M5M5178AP,J,FP-20,-25, -20L,-25L

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

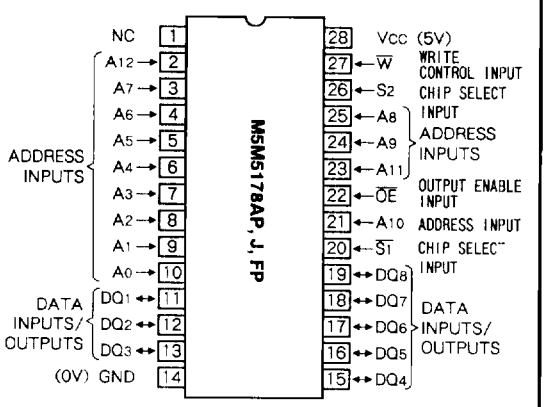
FEATURES

- Fast access time M5M5178AP,J,FP-20,-20L····· 20ns(max)
  M5M5178AP,J,FP-25,-25L····· 25ns(max)
- Low power dissipation Active ····· 300mW(typ)
  Stand-by(-20,-25) ····· 5mW(typ)
  Stand-by(-20L,-25L)····· 50μW(typ)
- Single +5V power supply
- Fully static operation : No clocks, no refresh
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S1}$, S2
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)

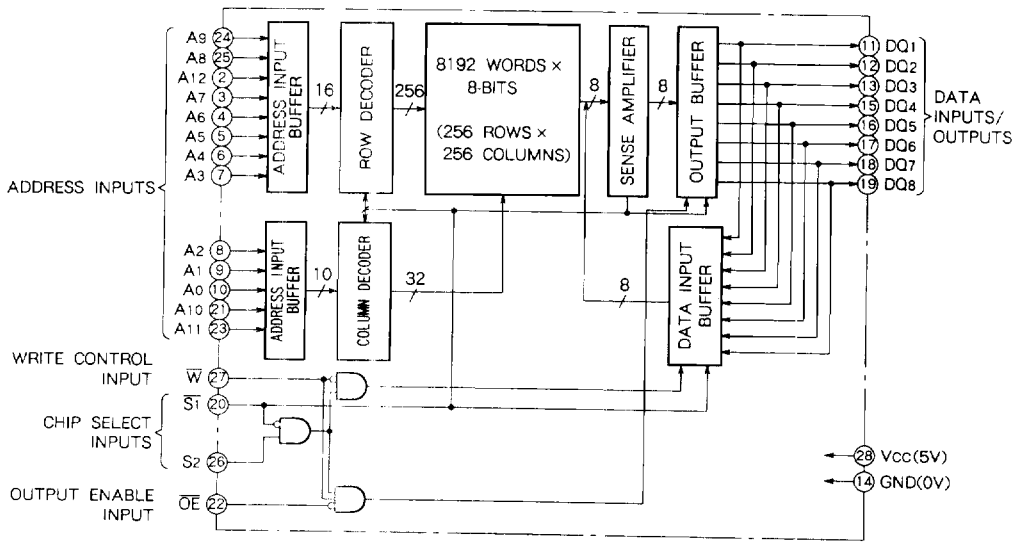
FUNCTION

The operation mode of the M5M5178A is determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.(see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and S2 are in an active state ($\overline{S1}$ = L, S2 = H)

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3}.

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
L	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H : V_{IH} L : V_{IL} X : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.5 * ~7	V
V_I	Input voltage		− 0.5 * ~V_{CC} + 0.3	V
V_O	Output voltage		0 ~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		− 10~85	℃
T_{stg}	Storage temperature		− 65~150	℃

* = − 3.5V in case of AC (pulse width ≦ 20ns), − 0.5V in case of DC

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage				2.4		V_{CC}+0.3	V
V_{IL}	Low input voltage				− 0.5*		0.6	V
V_{OH}	High output voltage		I_{OH} = − 4mA		2.4			V
V_{OL}	Low output voltage		I_{OL} = 8mA				0.4	V
I_I	Input current		V_I = 0~V_{CC}				± 10	μA
I_{OZH}	High level output current in off-state		$\overline{S_1}$ = V_{IH} or S_2 = V_{IL} or $\overline{OE}$ = V_{IH}				10	μA
I_{OZL}	Low level output current in off-state		$V_{I/O}$ = 0~V_{CC}				− 10	μA
I_{CC1}	Active supply current		$\overline{S_1}$ = V_{IL} or S_2 = V_{IH} Output open Other inputs = V_{IH}	AC(25MHz)			120	mA
				DC		60	70	
I_{CC2}	Stand by supply current		S_2 = V_{IL}, $\overline{S_1}$ = V_{IH} Other inputs=0~V_{CC}	AC(25MHz)			30	mA
				DC			20	
I_{CC3}	Stand by supply current		$\overline{S_1}$ = V_{CC} − 0.2V Other inputs ≦ 0.2V or V_{CC} − 0.2V	-20, -25			2	mA
				-20L, -25L		50	100	μA
C_I	Input capacitance	$\overline{S_1}$, S_2, $\overline{CE}$, $\overline{W}$	V_I = GND, V_I = 25mVrms, f = 1MHz				7	pF
		A_0~A_{12}					6	
C_O	Output capacitance		V_O = GND, V_O = 25mVrms, f = 1MHz				7	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).
2. CI, CO are periodically sampled and are not 100% tested.
* = − 3.0V in case of AC (pulse width ≦ 20ns), − 0.5V in case of DC

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing standard levels ····· V_{IH} = V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = V_{OL} = 1.5V
Output loads ····· Fig. 1, Fig. 2

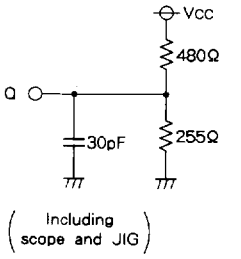


Fig. 1 Output load

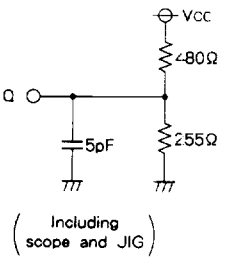


Fig. 2 Output load for t_{en}, t_{dis}

(2) Read cycle

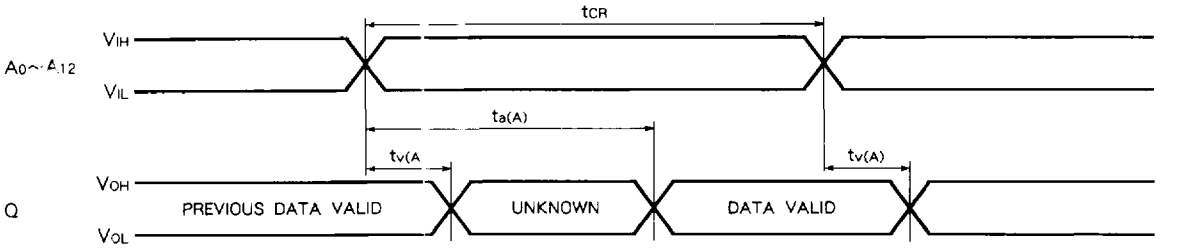
Symbol	Parameter	Limits				Unit
		M5M5178A-20, -20L		M5M5178A-25, -25L		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	20		25		ns
$t_{a(A)}$	Address access time		20		25	ns
$t_{a(S1)}$	Chip select 1 access time		20		25	ns
$t_{a(S2)}$	Chip select 2 access time		15		18	ns
$t_{a(OE)}$	Output enable access time		10		12	ns
$t_{v(A)}$	Data valid time after address change	3		3		ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	3		3		ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		10		15	ns
$t_{en(S2)}$	Output enable time after S_2 high	2		2		ns
$t_{dis(S2)}$	Output disable time after S_2 low		10		15	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	2		2		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		10		15	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip selection		20		25	ns

(3) Write cycle

Symbol	Parameter	Limits				Unit
		M5M5178A-20, -20L		M5M5178A-25, -25L		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	20		25		ns
$t_{su(S1)}$	Chip select 1 set up time	16		20		ns
$t_{su(S2)}$	Chip select 2 set up time	12		15		ns
$t_{su(A)1}$	Address set up time 1 ($\overline{W}$ control)	0		0		ns
$t_{su(A)2}$	Address set up time 2 ($\overline{S_1}$ control)	0		0		ns
$t_{su(A)3}$	Address set up time 3 (S_2 control)	0		0		ns
$t_{w(W)}$	Write pulse width	15		18		ns
$t_{rec(W)}$	Write recovery time	3		3		ns
$t_{su(D)}$	Data set up time	10		12		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		10		12	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		10		15	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	2		2		ns
$t_{su(A-\overline{WH})}$	Address to $\overline{W}$ high	15		18		ns

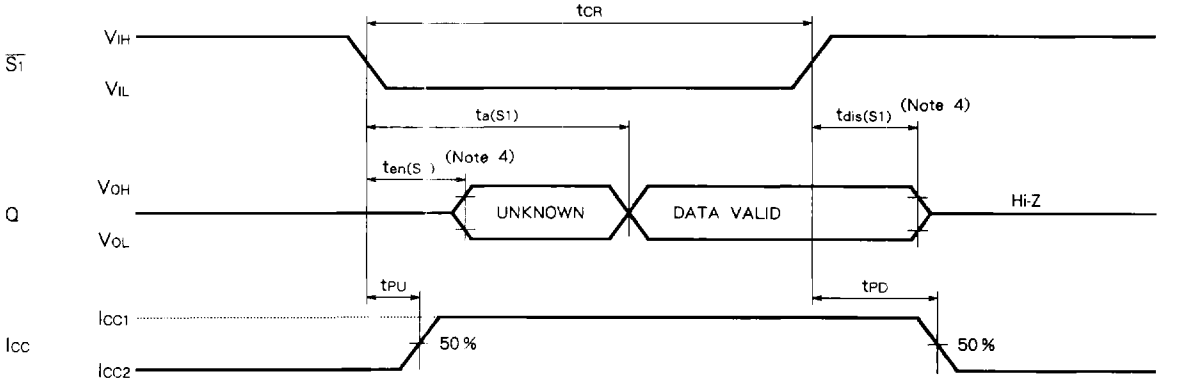
(4) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$S_2 = \overline{W} = H$
$\overline{S_1} = \overline{OE} = L$

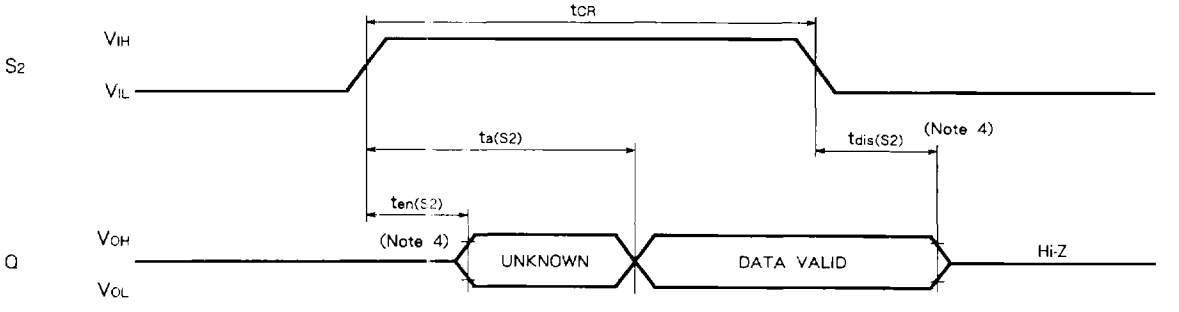
Read cycle 2 (Note 3)



$S_2 = \overline{W} = H$
$\overline{OE} = L$

Note 3. Addresses valid prior to or coincident with $\overline{S_1}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

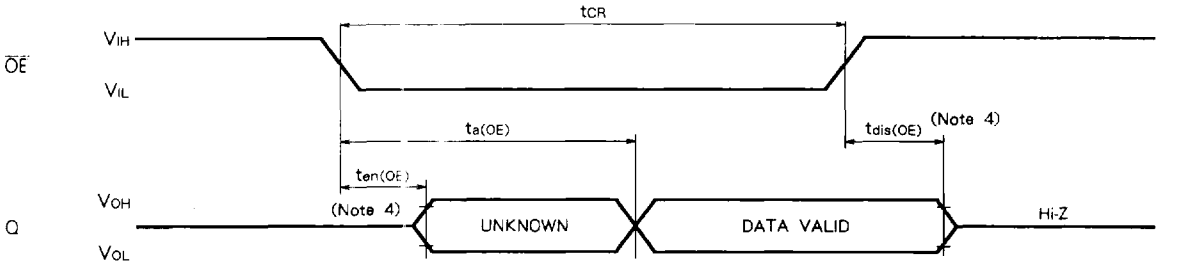
Read cycle 3 (Note 5)



$\overline{W} = H$
$\overline{S_1} = \overline{OE} = L$

Note 5. Addresses and $\overline{S_1}$ valid prior to S2 transition high by [ta(A) − ta(S2), ta(S1) − ta(S2)].

Read cycle 4 (Note 6)

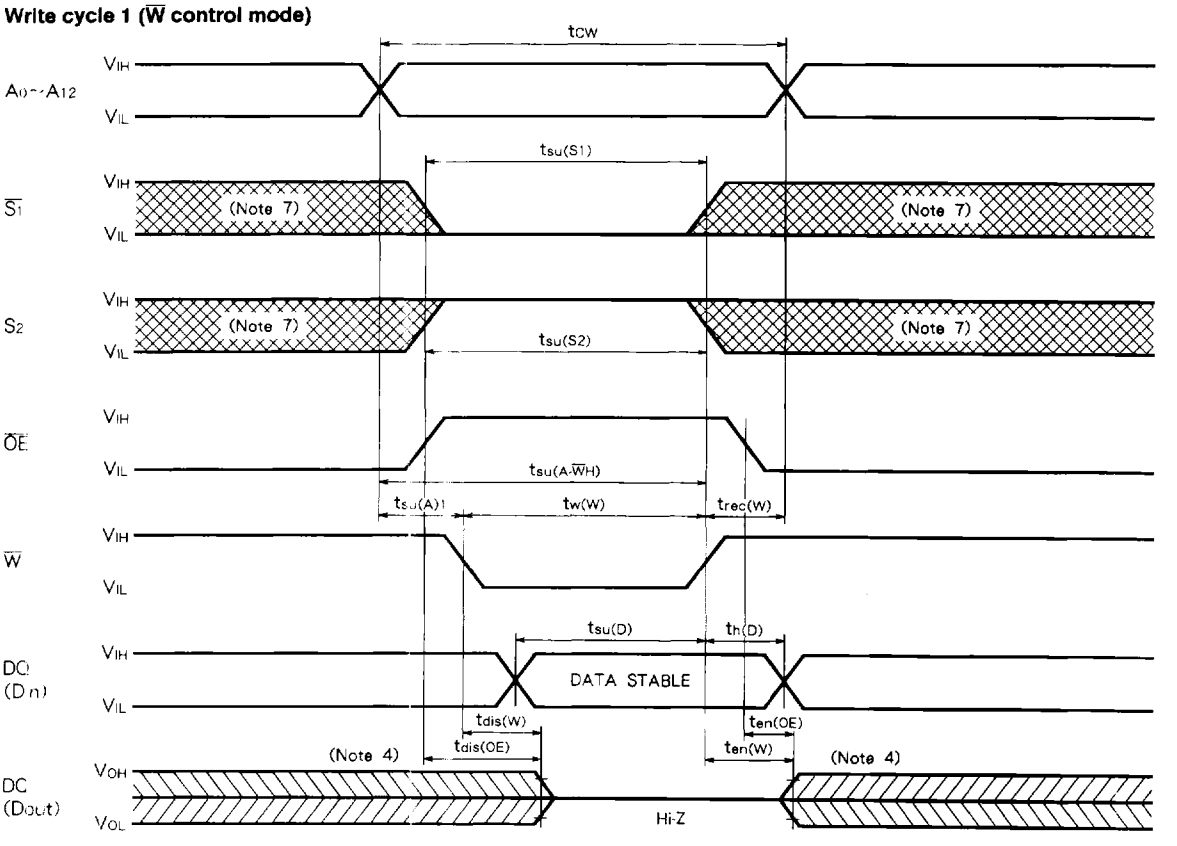


S_2 = $\overline{W}$ = H
$\overline{S1}$ = L

Note 6. Addresses and $\overline{S1}$ valid prior to $\overline{OE}$ transition low by [ta(A) − ta(OE), ta(S1) − ta(OE)].

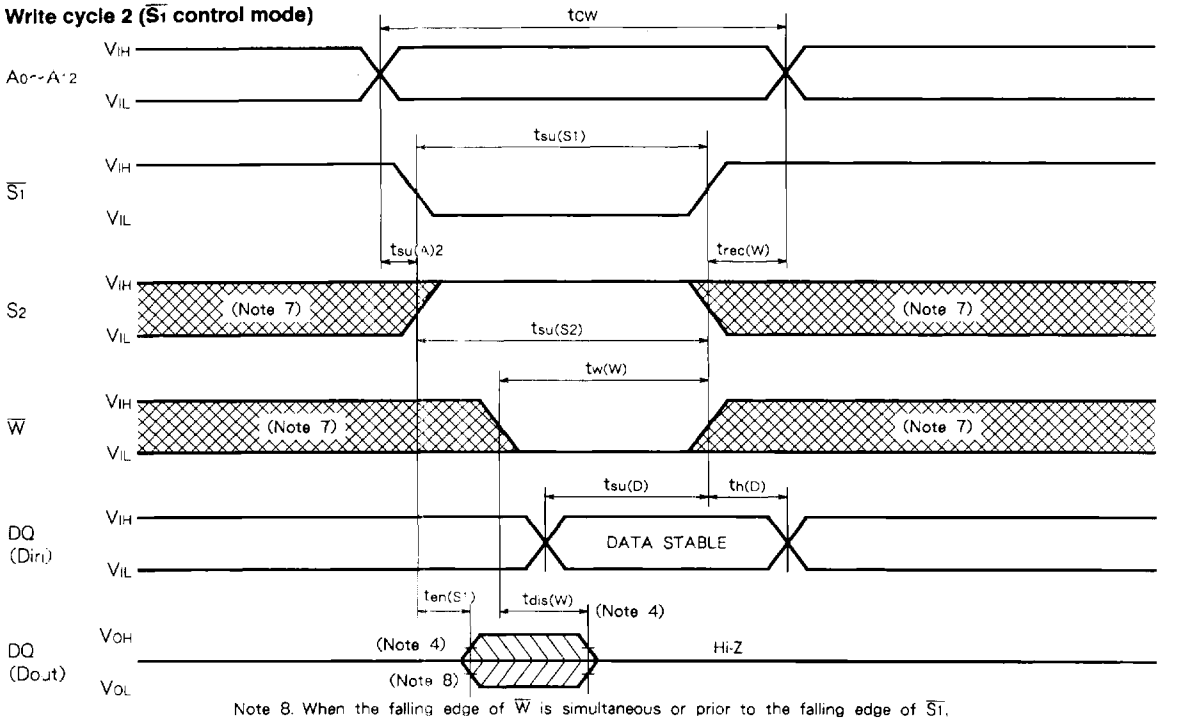
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



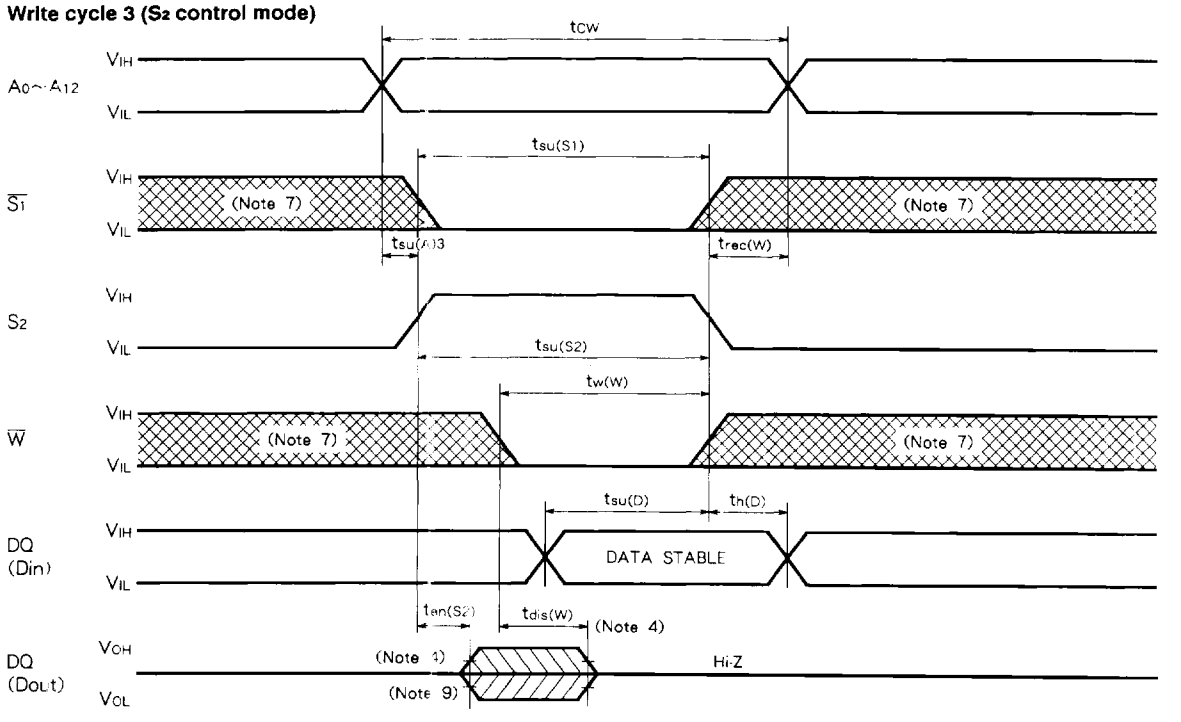
Note 7. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S_1}$ control mode)



Note 8. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S_1}$, the output is maintained in the high impedance.

Write cycle 3 (S_2 control mode)



Note 9. When the falling edge of $\overline{W}$ is simultaneous or prior to the rising edge of S_2, the output is maintained in the high impedance.

10. ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip select input voltage	$V_{I(\overline{ST})} \geqq V_{CC} - 0.2V$		$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time	$V_I \geqq V_{CC} - 0.2V$ or $0V \leqq V_I \leqq 0.2V$		0			ns
$t_{rec(PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3.0V$				50	μA
		$V_{CC} = 5.5V$				100	

Note 11. This is only M5M5178AP, J, FP-20L, -25L.

TIMING WAVEFORM FOR POWER DOWN