普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
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DESCRIPTION

PT6547 is a high performance Liquid Crystal Display (LCD) Driver IC utilizing CMOS Technology specially designed with Key Input Function. It can drive up to a maximum of 300 segments and control up to 8 general purpose output ports. It includes a Key Scan Circuit that can support up to 30 key inputs and provides On-Chip Voltage Detection Type Reset Circuit which prevents incorrect display. Display Data can be directly displayed without using any decoder. PT6547 also supports 1/3 to 1/4 duty-1/2 bias and 1/3 to 1/4 duty-1/3 bias drive techniques. Pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS Technology
- 1/3 duty and 1/4 duty Drive Techniques
- 1/2 bias and 1/3 bias Drive Techniques
- Up to 228 segments using 1/3 duty and up to 300 segments using 1/4 duty
- Up to 8 General Purpose Output Ports
- Key input function for up to 30 keys [6(O) x 5(I)]
- Serial interface for Clock, Data Input, Data Output, Strobe pins
- Sleep Mode & All segment OFF function
- On-Chip voltage detection type Reset circuit
- Power Supply: 4.5V ~ 6.0V
- /RES pin provided forcibly initializing the internal circuit
- RC Oscillation Circuit
- Available in 100 pins, LQFP Package

APPLICATION

- Electronic Equipment with LCD Display

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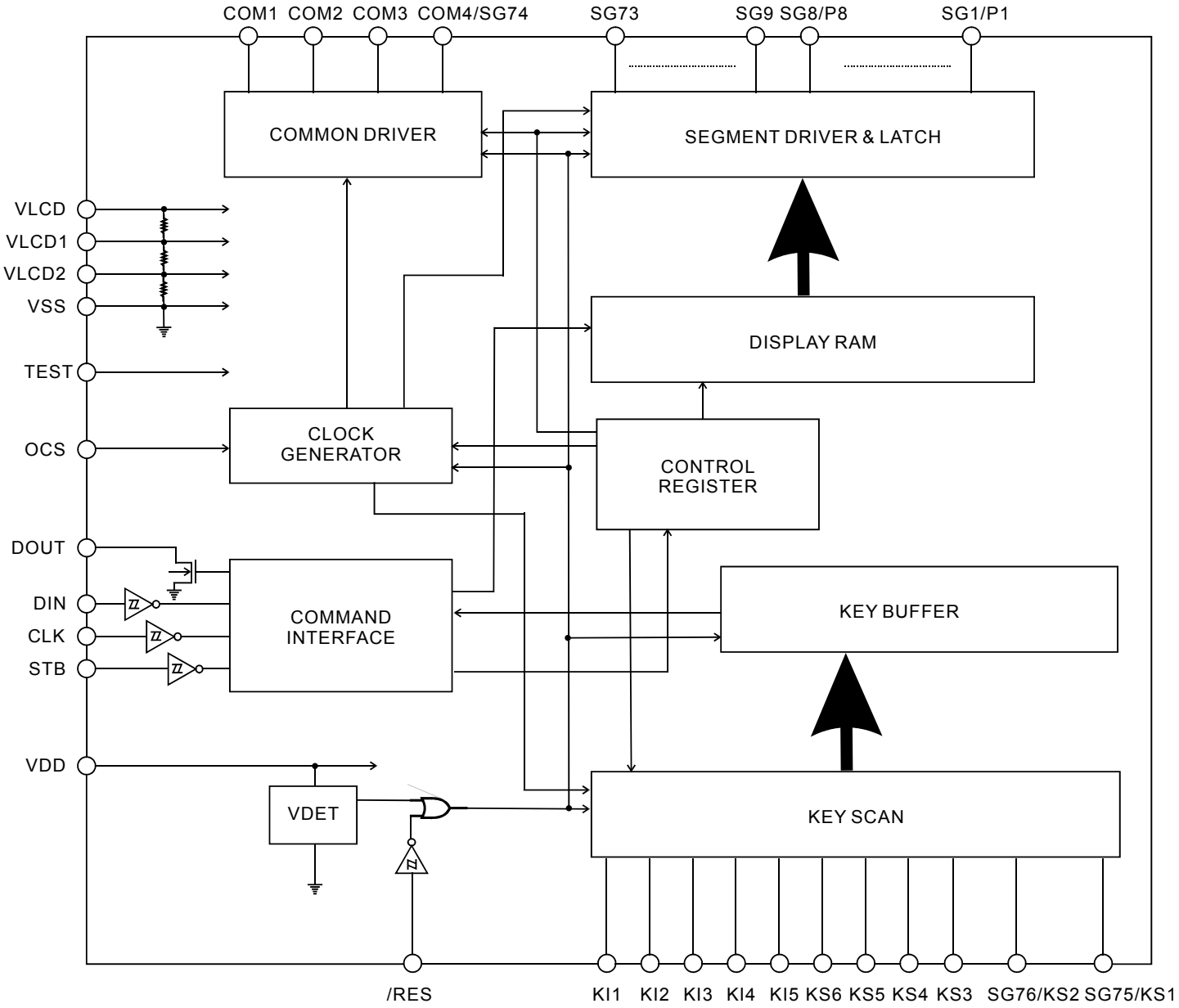
BLOCK DIAGRAM



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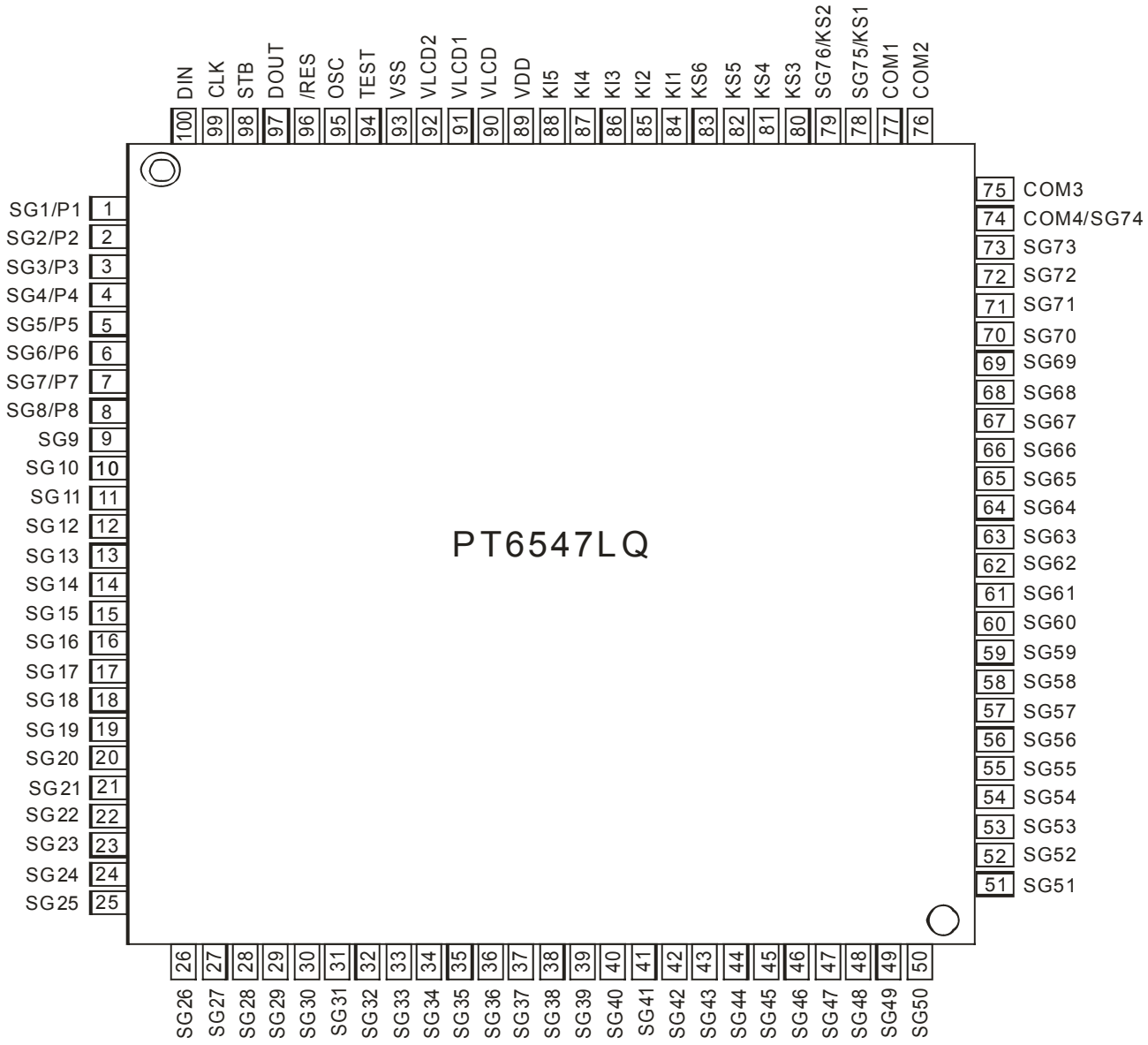
PIN CONFIGURATION

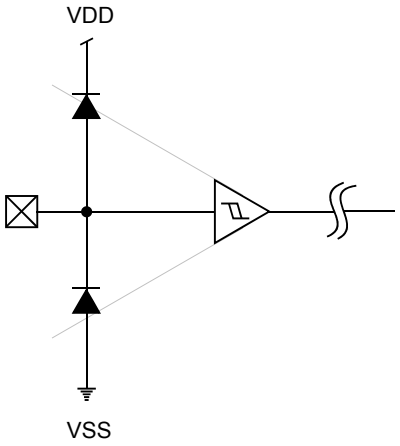
100PINS, LQFP



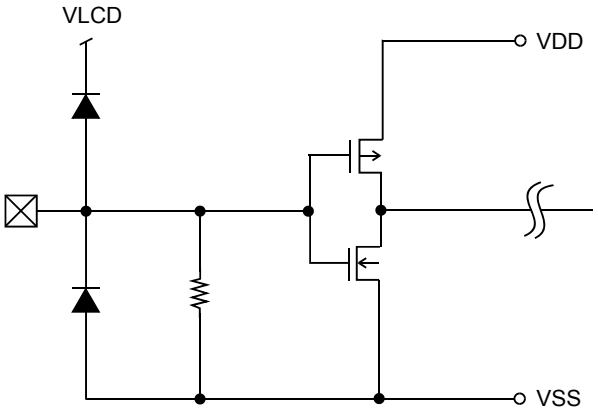
INPUT/OUPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

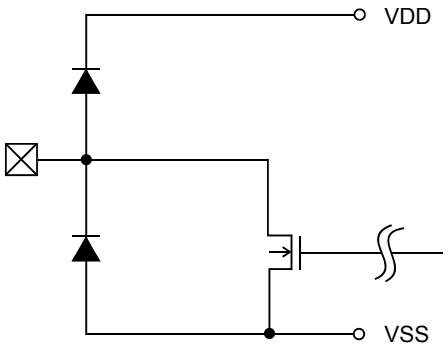
INPUT PIN: CLK, STB, DIN



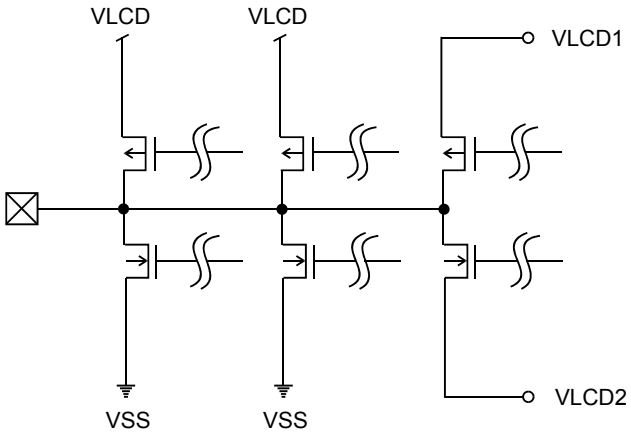
INPUT PIN: KI1 TO KI5



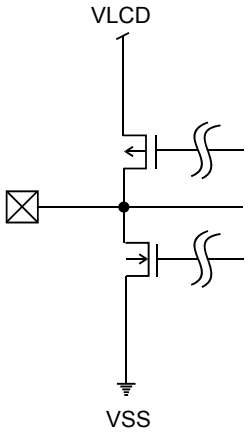
OUTPUT PIN: DOUT



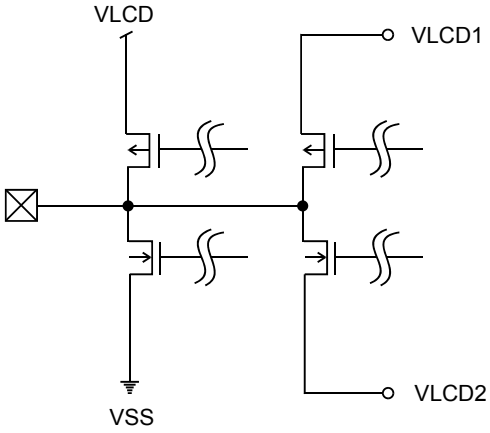
OUTPUT PIN: SG1/P1 TO SG8/P8, SG9 TO SG73, SG75/KS1, SG76/KS2



OUTPUT PIN: KS3 TO KS6



OUTPUT PIN: COM1 TO COM3, COM4/SG74



PIN DESCRIPTON

Pin Name	I/O	Description	Pin No.
SG1/P1 to SG8/P8	O	Segment Driver/General Purpose Output Pins	1 to 8
SG9 to SG73	O	Segment Driver Output Pins	9 to 73
SG74/COM4	O	Common/Segment Driver Output Pins This pin can used as segment output pin in 1/3 duty.	74
COM1 to COM3	O	Common Driver Output Pins	77 to 75
SG75/KS1, SG76/KS2	O	Key Scan/Segment Driver Output Pins	78, 79
KS3 to KS6	O	Key Scan Output Pins	80 to 83
KI1 to KI5	I	Key Scan Input Pins	84 to 88
VDD	-	Power Supply	89
VLCD	-	LCD Driver Power Supply	90
VLCD1	-	LCD Drive 2/3 Bias Voltage Power Supply Must be connected to VLCD2 when a 1/2 bias drive scheme is used.	91
VLCD2	-	LCD Drive 1/3 Bias Voltage Power Supply Must be connected to VLCD1 when a 1/2 bias drive scheme is used.	92
VSS	-	Ground Pin	93
TEST	I	This pin must be connected to ground.	94
OSC	I/O	Oscillator Input/Output Pin An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	95
/RES	I	Reset Input Pin When this pin is set to “Low”, reset to initial state.	96
DOUT	O	Data Output Pin (see Note) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	97
STB	I	Chip Enable Input Pin The data input after the STB has fallen is processed as a command. When this pin is “High”, CLK is ignored.	98
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	99
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	100

Note: This pin is open-drain output, a pull-up resistor of between 1K and 10KΩ is required.

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FUNCTION DESCRIPTION

COMMANDS

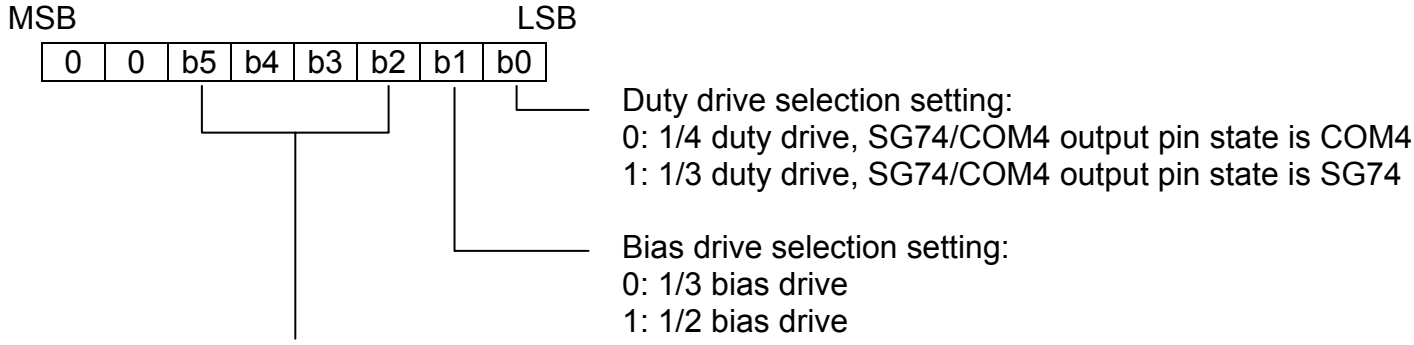
Commands determine the display mode and status of PT6547. A command is the first byte (b0 to b7) inputted to PT6547 via the DIN pin after STB pin has changed from "High" to "Low" State. If for some reason the STB Pin is set to "High" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE/OUTPUT-1 STATE SETTING COMMANDS

PT6547 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6547 via the DIN pin when STB is "Low". However, for these commands, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number, the bits 1 and 2 (b0 and b1) of duty drive and bias drive to be used (1/3 to 1/4 duty – 1/2 bias and 1/3 to 1/4 duty – 1/3 bias), the bits 3 to 6 (b2 to b5) are control which may be used for segment output port or general purpose output port.

When Power is turned on, the bit 6 to bit 1 (b5 to b0) are given the value of "0".

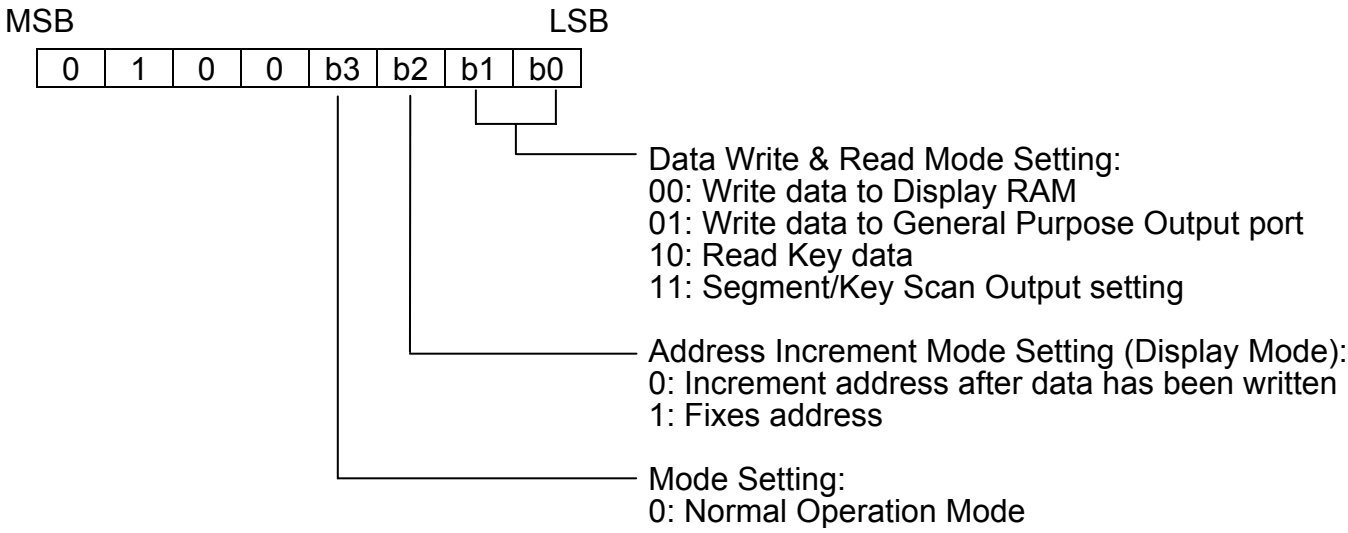


Control Bit				Output pin State							
b5	b4	b3	b2	SG1/P1	SG2/P2	SG3/P3	SG4/P4	SG5/P5	SG6/P6	SG7/P7	SG8/P8
0	0	0	0	SG1	SG2	SG3	SG4	SG5	SG6	SG7	SG8
0	0	0	1	P1	SG2	SG3	SG4	SG5	SG6	SG7	SG8
0	0	1	0	P1	P2	SG3	SG4	SG5	SG6	SG7	SG8
0	0	1	1	P1	P2	P3	SG4	SG5	SG6	SG7	SG8
0	1	0	0	P1	P2	P3	P4	SG5	SG6	SG7	SG8
0	1	0	1	P1	P2	P3	P4	P5	SG6	SG7	SG8
0	1	1	0	P1	P2	P3	P4	P5	P6	SG7	SG8
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	SG8
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8

COMMAND 2: DATA/OUTPUT-2 STATE SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6547. The data Setting Command, the bit 7 (b6) is given the value of "1" while bit 8 (b7) and bit 6 to bit 5 (b5 to b4) is given the value of "0". Please refer to the diagram below.

When power is turned on, the bit 4 to bit 1 (b3 to b0) are given the value of "0".



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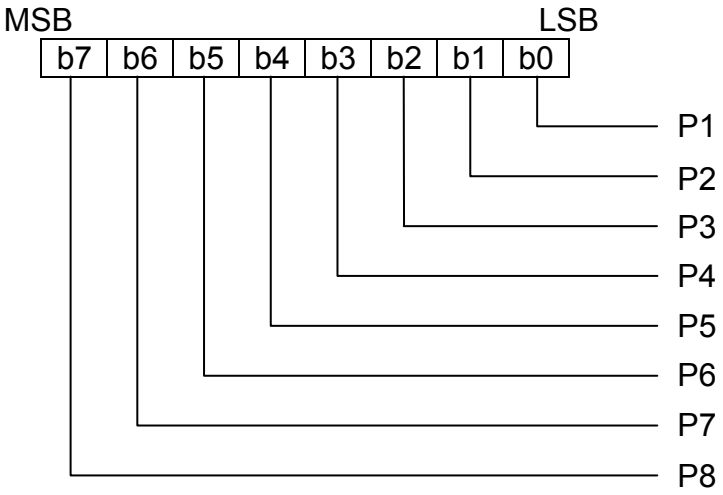
GENERAL PURPOSE OUTPUT PORT DATA

PT6547 provides 8 General Purpose Output Port namely P1 to P8. Data is written to the General Purpose Output Port starting from the least significant bit (b0) of the port using a Write Command.

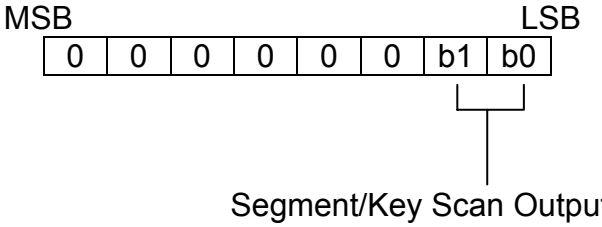
When power is turned on, the bit 8 to bit 1 (b7 to b0) are given the value of “0”.



SEGMENT/KEY SCAN OUTPUT SETTING

The Output State Setting Commands: Segment/Key Scan Output selection setting determine the number, the b0 to b1 are control which may be used for segment output port or key scan output port. Please refer to the diagram below.

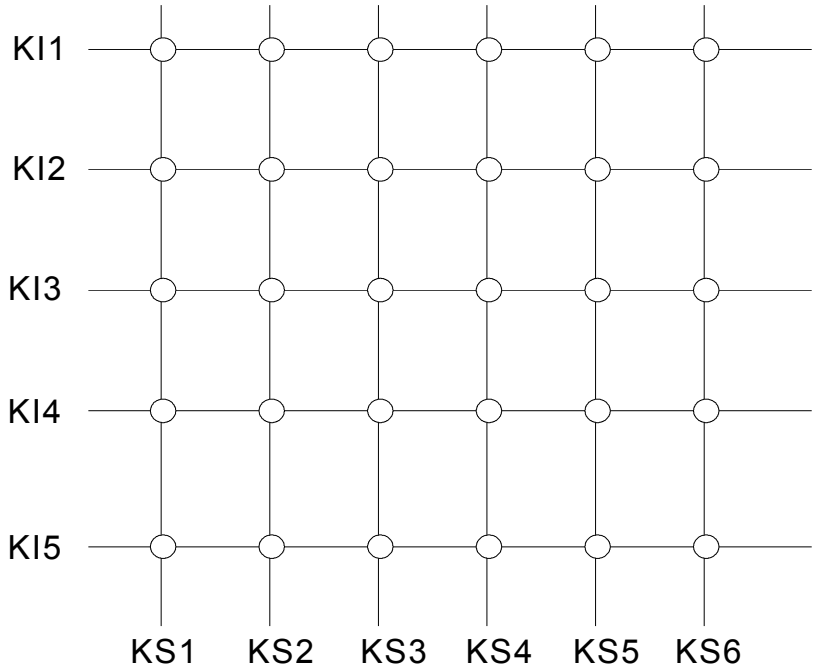
When power is turned on, the bit 2 to bit 1 (b1 to b0) are given the value of “1”.



Control Bit		Output pin State		Maximum number of input keys
b1	b0	SG75/KS1	SG76/KS2	
0	0	KS1	KS2	30
0	1	SG75	KS2	25
1	1	SG75	SG76	20

PT6547 KEY MATRIX

PT6547 Key Matrix consists of 6 x 5 arrays as shown below:



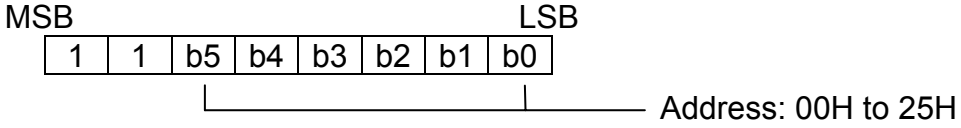
Each data inputted by each key are stored as follows. They are read by a Read Command, starting from the least significant bit.

KI1……KI5	KI1……KI5	KI1……KI5	KI1……KI5	KI1……KI5	KI1……KI5
KS1	KS2	KS3	KS4	KS5	KS6

Reading Sequence

COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is consider valid if it has a value of “00H” to “25H”. If the address is set to 26H or higher, the data is ignored until a valid address is set. When power is turned on, the address is set at “00H”. Please refer to the diagram below.



DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6547 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Address of PT6547 are given below in 8 bits unit.

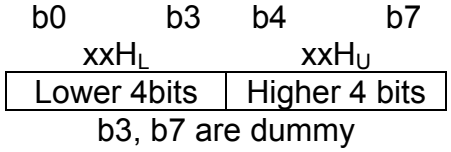
1/3 duty

	COM1 COM3
SG1	$00H_L$
SG2	$00H_U$
SG3	$01H_L$
SG4	$01H_U$
SG5	$02H_L$
SG6	$02H_U$
SG7	$03H_L$
SG8	$03H_U$
SG9	$04H_L$
SG10	$04H_U$
SG11	$05H_L$
SG12	$05H_U$
SG13	$06H_L$
SG14	$06H_U$
SG15	$07H_L$
SG16	$07H_U$
SG17	$08H_L$
SG18	$08H_U$
SG19	$09H_L$
SG20	$09H_U$

	COM1 COM3
SG21	$0AH_L$
SG22	$0AH_U$
SG23	$0BH_L$
SG24	$0BH_U$
SG25	$0CH_L$
SG26	$0CH_U$
SG27	$0DH_L$
SG28	$0DH_U$
SG29	$0EH_L$
SG30	$0EH_U$
SG31	$0FH_L$
SG32	$0FH_U$
SG33	$10H_L$
SG34	$10H_U$
SG35	$11H_L$
SG36	$11H_U$
SG37	$12H_L$
SG38	$12H_U$
SG39	$13H_L$
SG40	$13H_U$

	COM1 COM3
SG41	$14H_L$
SG42	$14H_U$
SG43	$15H_L$
SG44	$15H_U$
SG45	$16H_L$
SG46	$16H_U$
SG47	$17H_L$
SG48	$17H_U$
SG49	$18H_L$
SG50	$18H_U$
SG51	$19H_L$
SG52	$19H_U$
SG53	$1AH_L$
SG54	$1AH_U$
SG55	$1BH_L$
SG56	$1BH_U$
SG57	$1CH_L$
SG58	$1CH_U$
SG59	$1DH_L$
SG60	$1DH_U$

	COM1 COM3
SG61	$1EH_L$
SG62	$1EH_U$
SG63	$1FH_L$
SG64	$1FH_U$
SG65	$20H_L$
SG66	$20H_U$
SG67	$21H_L$
SG68	$21H_U$
SG69	$22H_L$
SG70	$22H_U$
SG71	$23H_L$
SG72	$23H_U$
SG73	$24H_L$
SG74	$24H_U$
SG75	$25H_L$
SG76	$25H_U$



1/4duty

	COM1 COM4
SG1	$00H_L$
SG2	$00H_U$
SG3	$01H_L$
SG4	$01H_U$
SG5	$02H_L$
SG6	$02H_U$
SG7	$03H_L$
SG8	$03H_U$
SG9	$04H_L$
SG10	$04H_U$
SG11	$05H_L$
SG12	$05H_U$
SG13	$06H_L$
SG14	$06H_U$
SG15	$07H_L$
SG16	$07H_U$
SG17	$08H_L$
SG18	$08H_U$
SG19	$09H_L$
SG20	$09H_U$

	COM1 COM4
SG21	$0AH_L$
SG22	$0AH_U$
SG23	$0BH_L$
SG24	$0BH_U$
SG25	$0CH_L$
SG26	$0CH_U$
SG27	$0DH_L$
SG28	$0DH_U$
SG29	$0EH_L$
SG30	$0EH_U$
SG31	$0FH_L$
SG32	$0FH_U$
SG33	$10H_L$
SG34	$10H_U$
SG35	$11H_L$
SG36	$11H_U$
SG37	$12H_L$
SG38	$12H_U$
SG39	$13H_L$
SG40	$13H_U$

	COM1 COM4
SG41	$14H_L$
SG42	$14H_U$
SG43	$15H_L$
SG44	$15H_U$
SG45	$16H_L$
SG46	$16H_U$
SG47	$17H_L$
SG48	$17H_U$
SG49	$18H_L$
SG50	$18H_U$
SG51	$19H_L$
SG52	$19H_U$
SG53	$1AH_L$
SG54	$1AH_U$
SG55	$1BH_L$
SG56	$1BH_U$
SG57	$1CH_L$
SG58	$1CH_U$
SG59	$1DH_L$
SG60	$1DH_U$

	COM1 COM4
SG61	$1EH_L$
SG62	$1EH_U$
SG63	$1FH_L$
SG64	$1FH_U$
SG65	$20H_L$
SG66	$20H_U$
SG67	$21H_L$
SG68	$21H_U$
SG69	$22H_L$
SG70	$22H_U$
SG71	$23H_L$
SG72	$23H_U$
SG73	$24H_L$
SG75	$24H_U$
SG76	$25H_L$

b0 b3	b4 b7
xxH_L	xxH_U
Lower 4bits	Higher 4 bits

COMMAND 4: DISPLAY CONTROL COMMANDS

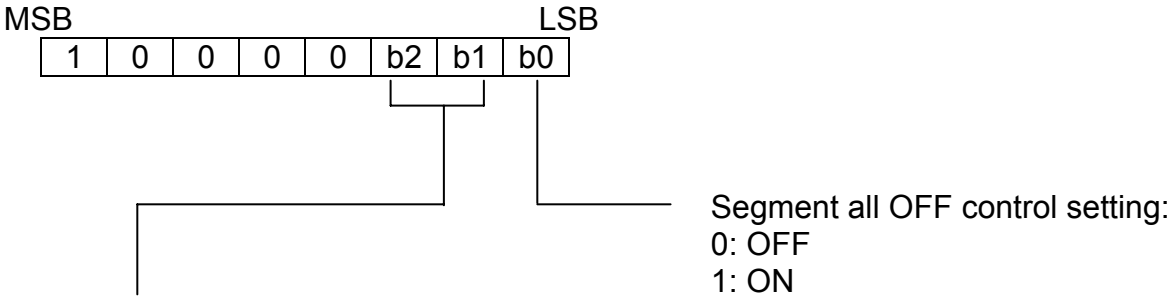
The Display Control Commands are used to Sleep Mode control and all segment off.

When bit 1 (b0) is set to "1", the segment display state is "ON"; When bit 1 (b0) is set to "0", the segment display state is "OFF". This "OFF" state is achieved by outputting segment "OFF" waveforms from the segment output pins.

Bit 2 to 3 (b1 to b2) are switch between Normal and Sleep Mode. Set the key states of the KS1 to KS6 key scan outputs during key scan standby.

Bit 8 (b7) is given the value of "1" while bit 7 to bit 4 (b6 to b3) is given the value of "0". Please refer to the diagram below.

When power is turned on, the bit 3 to bit 1 (b2 to b0) are given the value of "0".



Control Bit		Mode	OSC oscillator	Segment/Common Output state	Output pins state during key scan standby					
b2	b1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Operating	Operating	"H"	"H"	"H"	"H"	"H"	"H"
0	1	Sleep	Stopped	"L"	"L"	"L"	"L"	"L"	"L"	"H"
1	0				"L"	"L"	"L"	"L"	"H"	"H"
1	1				"H"	"H"	"H"	"H"	"H"	"H"

*Note: Assumes that SG75/KS1 and SG76/KS2 output pins are selected for key scan output.

SLEEP MODE

Sleep mode is set up by setting b2 or b1 in the control bit to "1". The segment and common outputs will all go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This mode could reduce power dissipation. This mode is cleared by sending control data with both b2 and b1 set to "0".

VOLTAGE DETECTION TYPE RESET (VDET)

The Voltage Detection Type reset Circuit (VDET) generates an output signal and resets the systems under the following conditions:

1. When power is initiated or first applied.
2. When the voltage drops (i.e. the Power Supply Voltages is less than or equal to the Power Down Detection Voltage, VDET).

To insure that this function will operate properly, then a capacitor must be connected to the power supply line so that the Power Supply Voltage VDD Rise Time when the power is first applied as well as the Power Supply Voltage VDD fall time when the voltage drops are both at least 1ms.

RESET OF OUTPUT PINS STATE

The states of the output pins during the reset period are given in the table below.

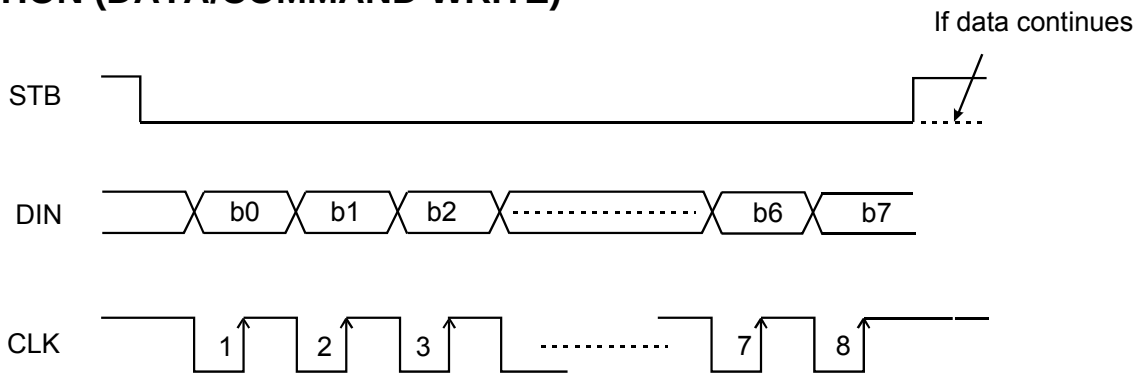
Output Pin	State during the Reset Period	Remarks
SG1/P1 to SG8/P8 SG75/KS1, SG76/KS2	L	These output pins are forcibly set to the segment output function and held low.
SG9 to SG73	L	-
COM4/SG74	L	This output pin is forcibly set to the common output function and held low. However, when the Command 1's b0 control bit is transferred, either the common output or the segment output function is selected.
COM1 to COM3	L	-
KS3 to KS5	x (see Note)	When the power is first applied, the states of these output pins are undefined until the command 4's b2 and b1 control bits have been transferred.
KS6	H	-
DOUT	H	This output pin is an open-drain output, thus a 1k to 10kΩ pull-up resistor is needed. This pin is kept at "HIGH" level during the reset period even if the key data read operation is performed.

Note: x=Not Relevant

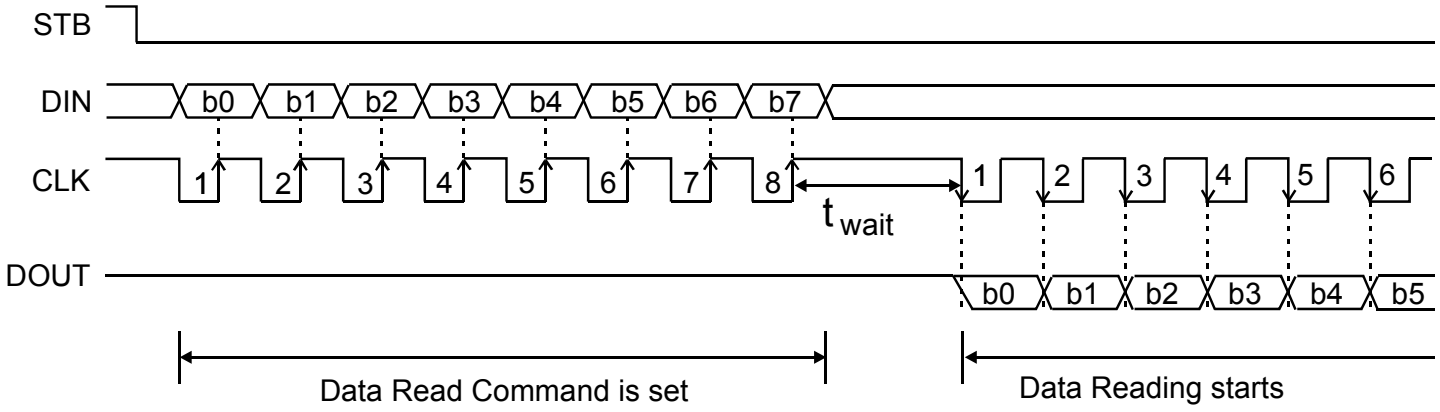
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6547 serial communication format. The DOUT pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)



TRANSMISSION (DATA READ)



where: twait (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

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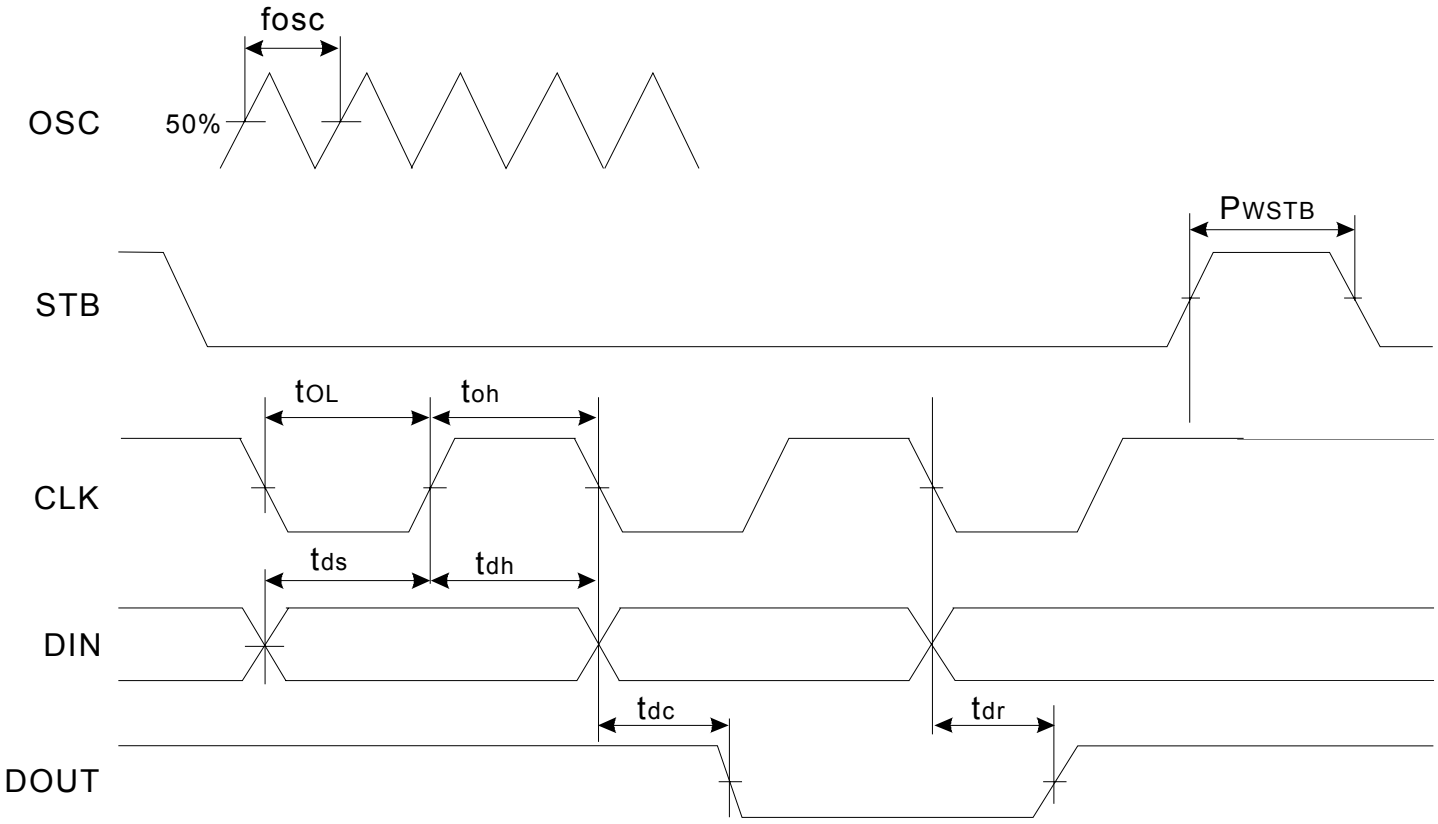
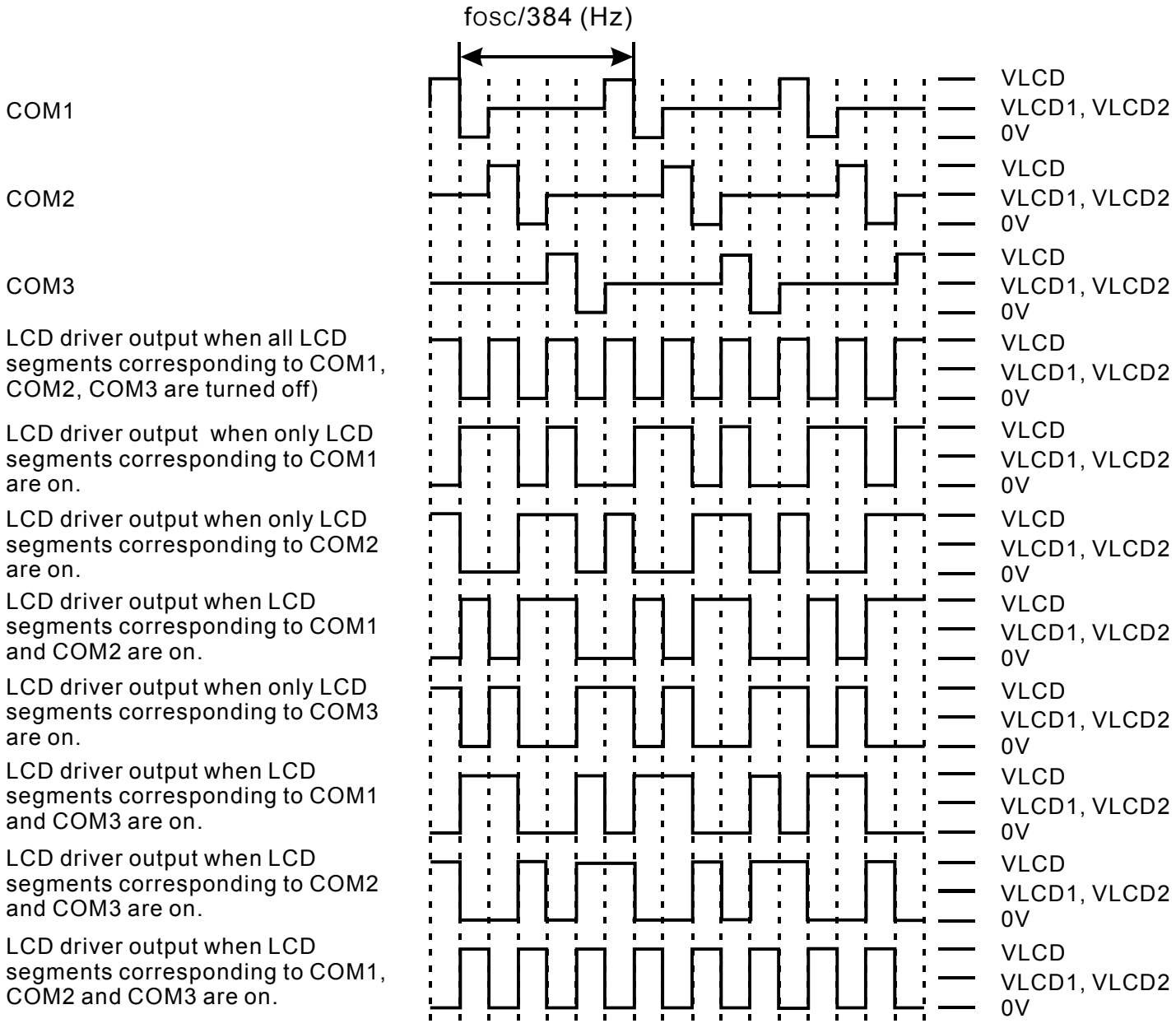
SWITCHING CHARACTERISTICS WAVEFORM

PT6547 switching characteristics waveform is given below.



1/3 DUTY, 1/2 BIAS DRIVE TECHNIQUE



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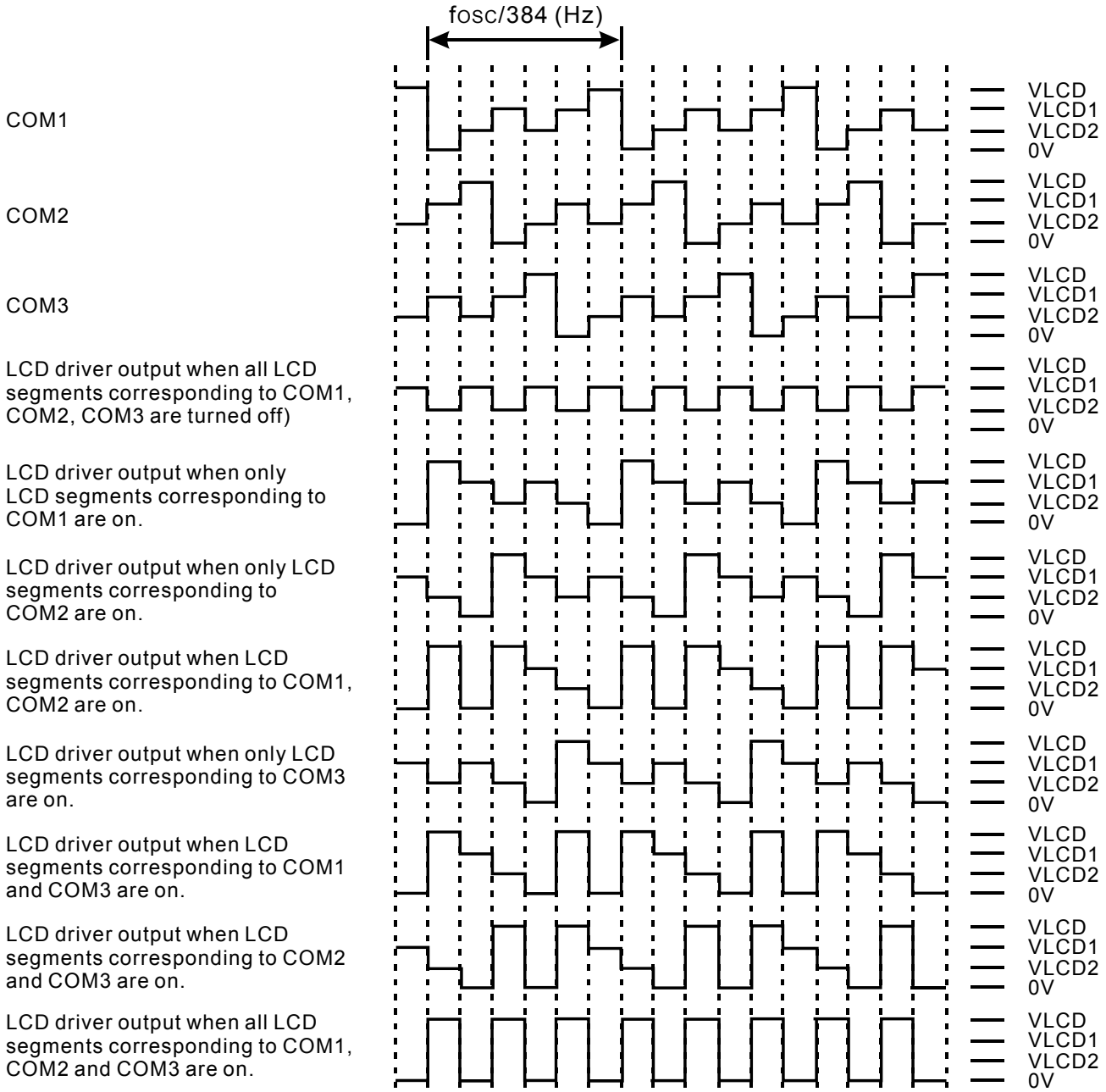
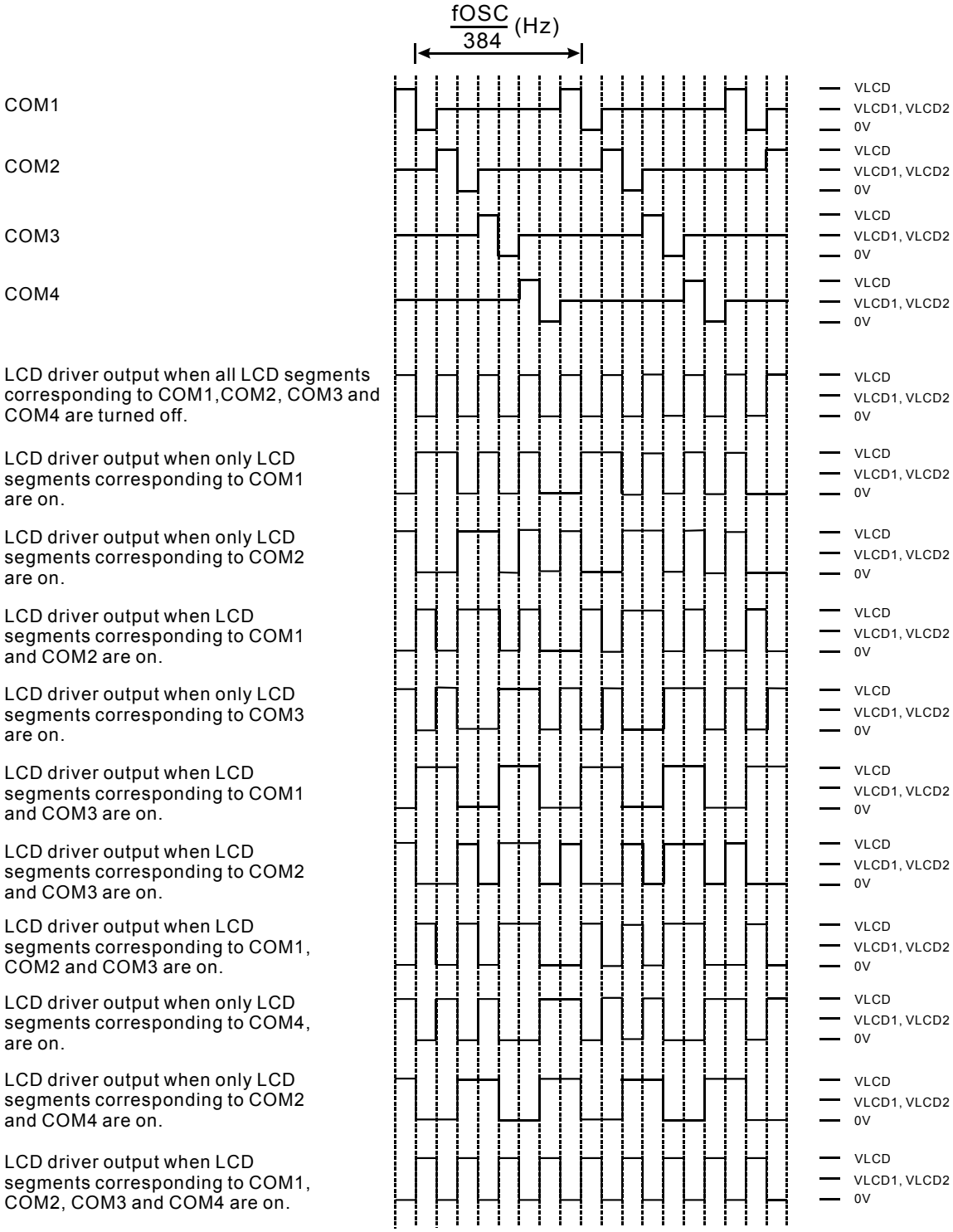
1/3 DUTY, 1/3 BIAS DRIVE TECHNIQUE



1/4 DUTY, 1/2 BIAS DRIVE TECHNIQUE



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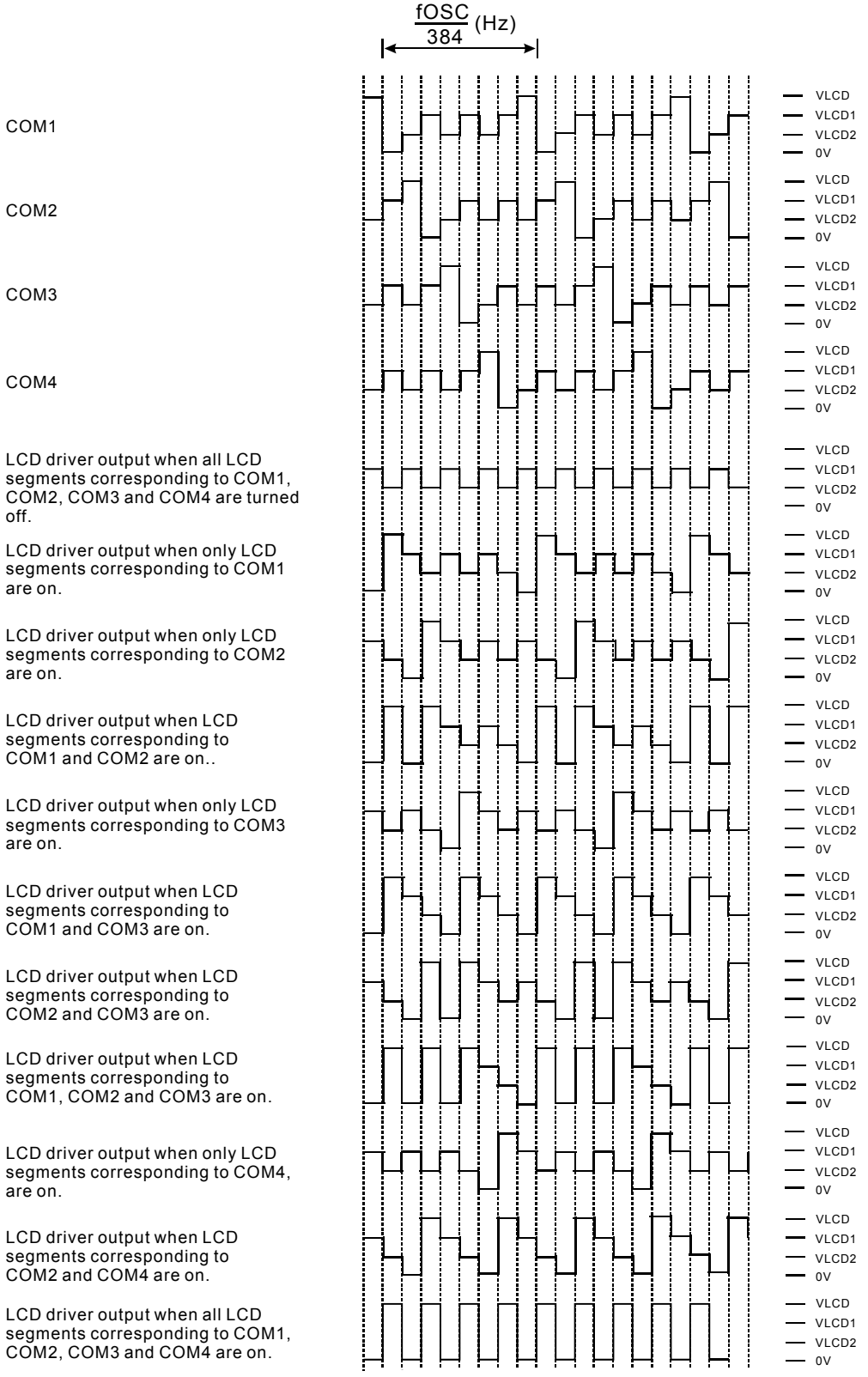
1/4 DUTY, 1/3 BIAS DRIVE TECHNIQUE



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25°C, Vss=0V)

Parameter	Symbol	Conditions	Rating	Unit
Maximum supply voltage	VDD max	VDD	-0.3 to +7.0	V
Maximum supply voltage	VLCD max	VLCD	-0.3 to +7.0	V
Input voltage	VIN1	DIN, CLK, STB, /RES	-0.3 to VDD+0.3	V
	VIN2	OSC, TEST	-0.3 to VDD+0.3	V
	VIN3	VLCD1, VLCD2, KI1 to KI5	-0.3 to VLCD+0.3	V
Output voltage	VOUT1	DOUT	-0.3 to VDD+0.3	V
	VOUT2	OSC	-0.3 to VDD+0.3	V
	VOUT3	SG1 to SG76, COM1 to COM4, KS1 to KS6, P1 to P8	-0.3 to VLCD+0.3	V
Output current	IOUT1	SG1 to SG76	300	μA
	IOUT2	COM1 to COM4	3	mA
	IOUT3	KS1 to KS6	1	mA
	IOUT4	P1 to P8	5	mA
Allowable power dissipation	Pd max	Ta=85°C	200	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-65 to +150	°C

ALLOWABLE OPERATING CONDITIONS

(Unless otherwise specified, Ta=-40 to +85°C, Vss=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDD	VDD	4.5	-	6.0	V
	VLCD	VLCD	VDD-0.5	-	6.0	
Input voltage	VLCD1	VLCD 1	-	2/3VLCD	VLCD	V
	VLCD2	VLCD 2	-	1/3VLCD	VLCD	
Input high level voltage	VIH1	DIN, CLK, STB, /RES	0.8VDD	-	VDD	V
	VIH2	KI1 to KI5	0.6VLCD	-	VLCD	
Input low level voltage	VIL	DIN, CLK, STB, /RES, (KI1 to KI5)	0	-	0.2VDD (0.2VLCD)	V
Recommended external resistance	ROSC	OSC	-	39	-	KΩ
Recommended external capacitance	COSC	OSC	-	1000	-	pF
Data setup time	tds	CLK, DIN	160	-	-	ns
Data hold time	tdh	CLK, DIN	160	-	-	ns
High level clock pulse width	tOH	CLK	160	-	-	ns
Low level clock pulse width	tOL	CLK	160	-	-	ns
Rise time	tr	STB, CLK, DIN	-	160	-	ns
Fall time	tf	STB, CLK, DIN	-	160	-	ns
DO output delay time	tdc	DOUT	-	-	1.5	μs
DO rise time	tdr	DOUT	-	-	1.5	μs

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25°C, VDD=5.0V, Vss=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Hysteresis	VH	DIN, CLK, STB, /RES, KI1 to KI5	-	0.1VDD	-	V
Power-down detection voltage	VDET		3.5	-	-	V
Input high level voltage	IIH	DIN, CLK, STB, /RES: VI=VDD	-	-	5.0	μA
Input high level current	IIL	DIN, CLK, STB, /RES: VI=0V	5.0	-	-	μA
Input floating voltage	VIF	KI1 to KI5	-	-	0.05VLCD	V
Pull-down resistance	RPD	KI1 to KI5: VLCD=5.0V	50	100	250	KΩ
Output off leakage current	IOFFH	DOUT: VO=6.0V	-	-	6.0	μA
Output high level voltage	VOH1	KS1 to KS6: IO=-500μA	VLCD-1.0	VLCD-0.5	VLCD-0.2	V
	VOH2	P1 to P8: IO=-1mA	VLCD-1.0	-	-	
	VOH3	SG1 to SG76: IO=-20μA	VLCD-1.0	-	-	
	VOH4	COM1 to COM4: IO=-100μA	VLCD-1.0	-	-	
Output low level voltage	VOL1	KS1 to KS6: IO=25μA	0.2	0.5	1.5	V
	VOL2	P1 to P8: IO=1mA	-	-	1.0	
	VOL3	SG1 to SG76: IO=20μA	-	-	1.0	
	VOL4	COM1 to COM4: IO=100μA	-	-	1.0	
	VOL5	DOUT: IO=1mA	-	0.1	0.5	
Output middle level voltage (see Note.)	VMID1	COM1 to COM4: 1/2 bias, IO=±100μA	1/2VLCD-1.0	-	1/2VLCD+1.0	V
	VMID2	SG1 to SG76:1/3 bias, IO=±20μA	2/3VLCD-1.0	-	2/3VLCD+1.0	
	VMID3	SG1 to SG76: 1/3 bias, IO=±20μA	1/3VLCD-1.0	-	1/3VLCD+1.0	
	VMID4	COM1 to COM4: 1/3 bias, IO=±100μA	2/3VLCD-1.0	-	2/3VLCD+ 1.0	
	VMID5	COM1 to COM4: 1/3 bias, IO=±100μA	1/3VLCD-1.0	-	1/3VLCD+ 1.0	
Oscillator frequency	fOSC	OSC: ROSC=39 kΩ, COSC=1000pF	30.4	38	45.6	KHz
Current drain	IDD1	VDD: Sleep mode	-	-	150	μA
	IDD2	VDD: VDD=6.0V, output open, fOSC=38KHz	-	405	810	
	IDD3	VLCD: Sleep mode	-	-	7.5	
	IDD4	VLCD: VLCD=6.0V, output open,1/2 bias, fOSC=38KHz	-	300	600	
	IDD5	VLCD: VLCD=6.0V, output open, 1/3 bias, fOSC=38KHz	-	180	360	

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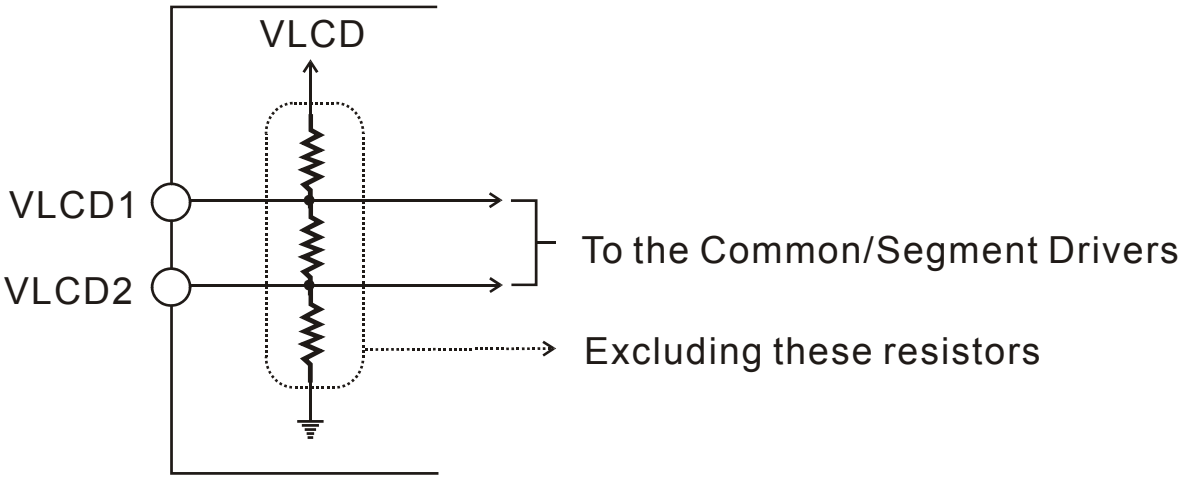
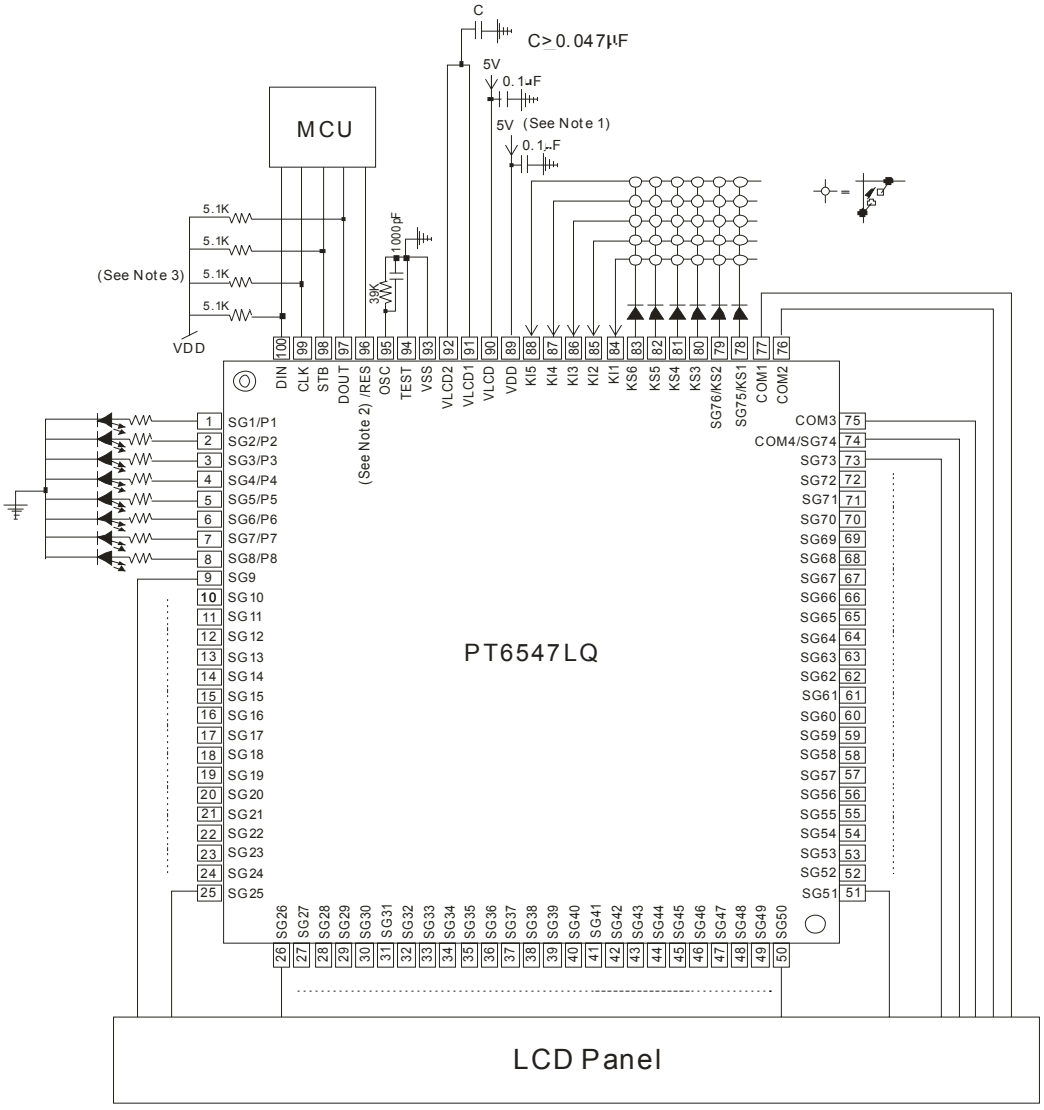
Note: The Bias Voltage Generation Driver built-into VLCD1 and VLCD2 are not included. Please refer to the diagram below.



APPLICATION CIRCUIT 1

1/3 DUTY 1/2 BIAS (FOR NORMAL PANEL USE)



Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

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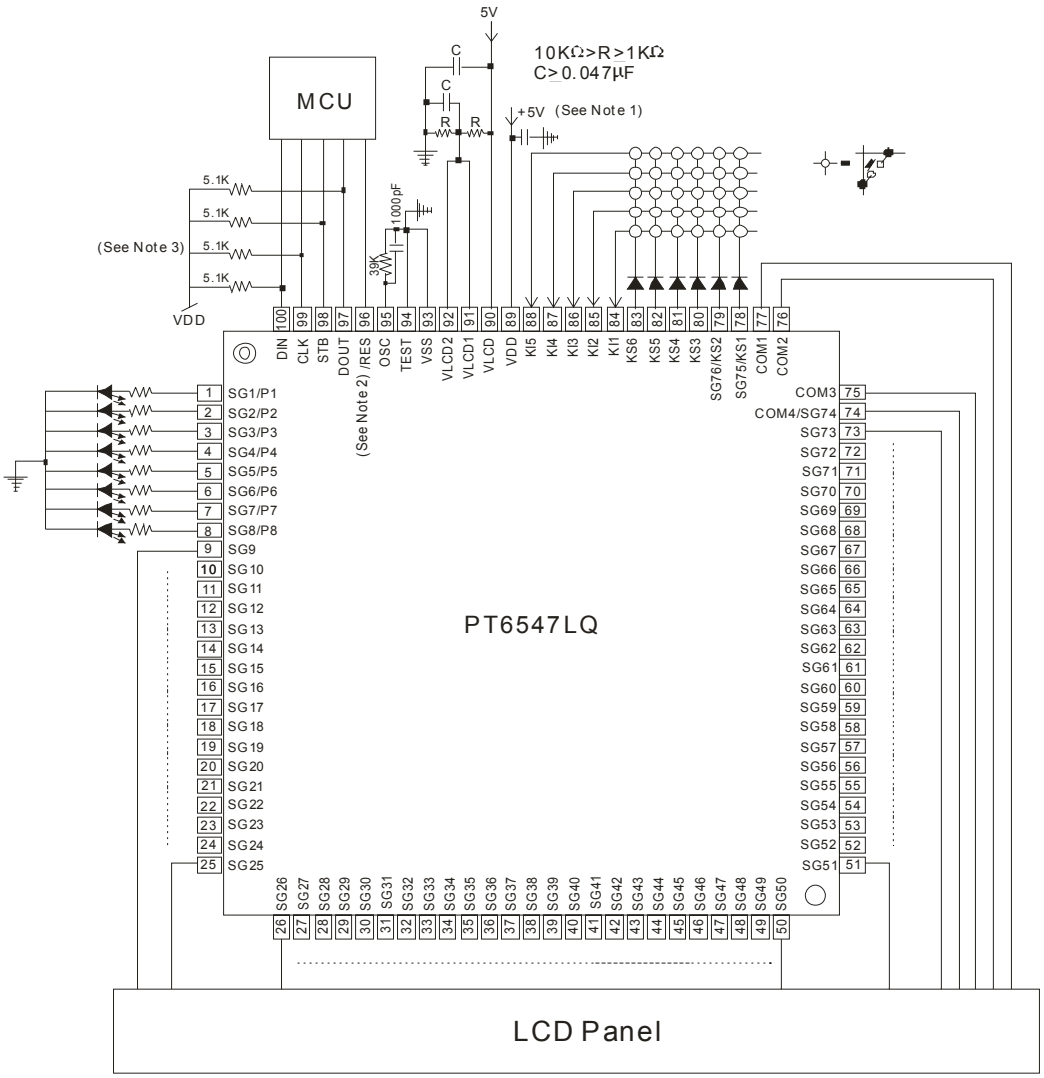
APPLICATION CIRCUIT 2

1/3 DUTY 1/2 BIAS (FOR LARGE PANEL USE)

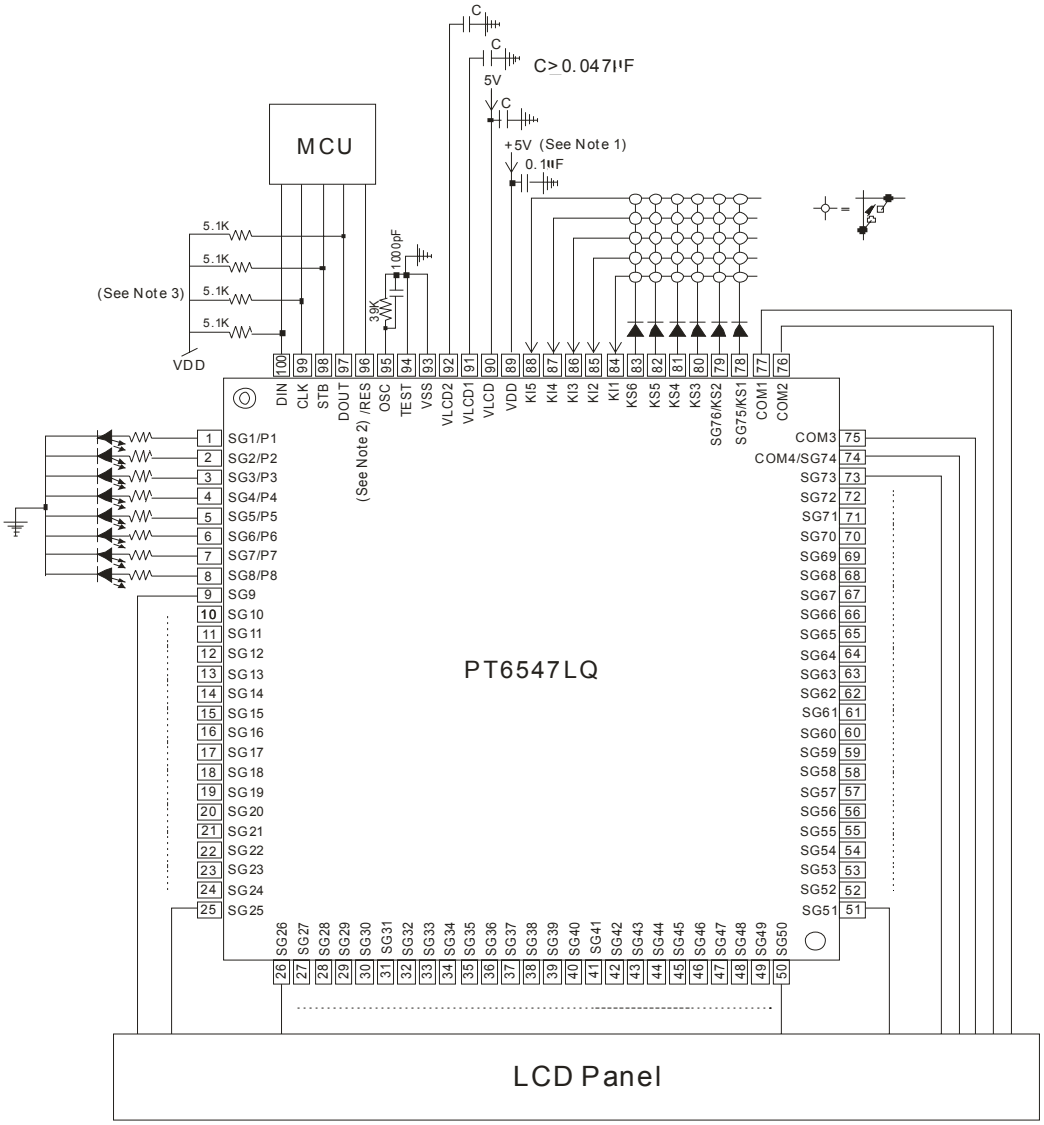


Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

APPLICATION CIRCUIT 3

1/3 DUTY 1/3 BIAS (FOR NORMAL PANEL USE)

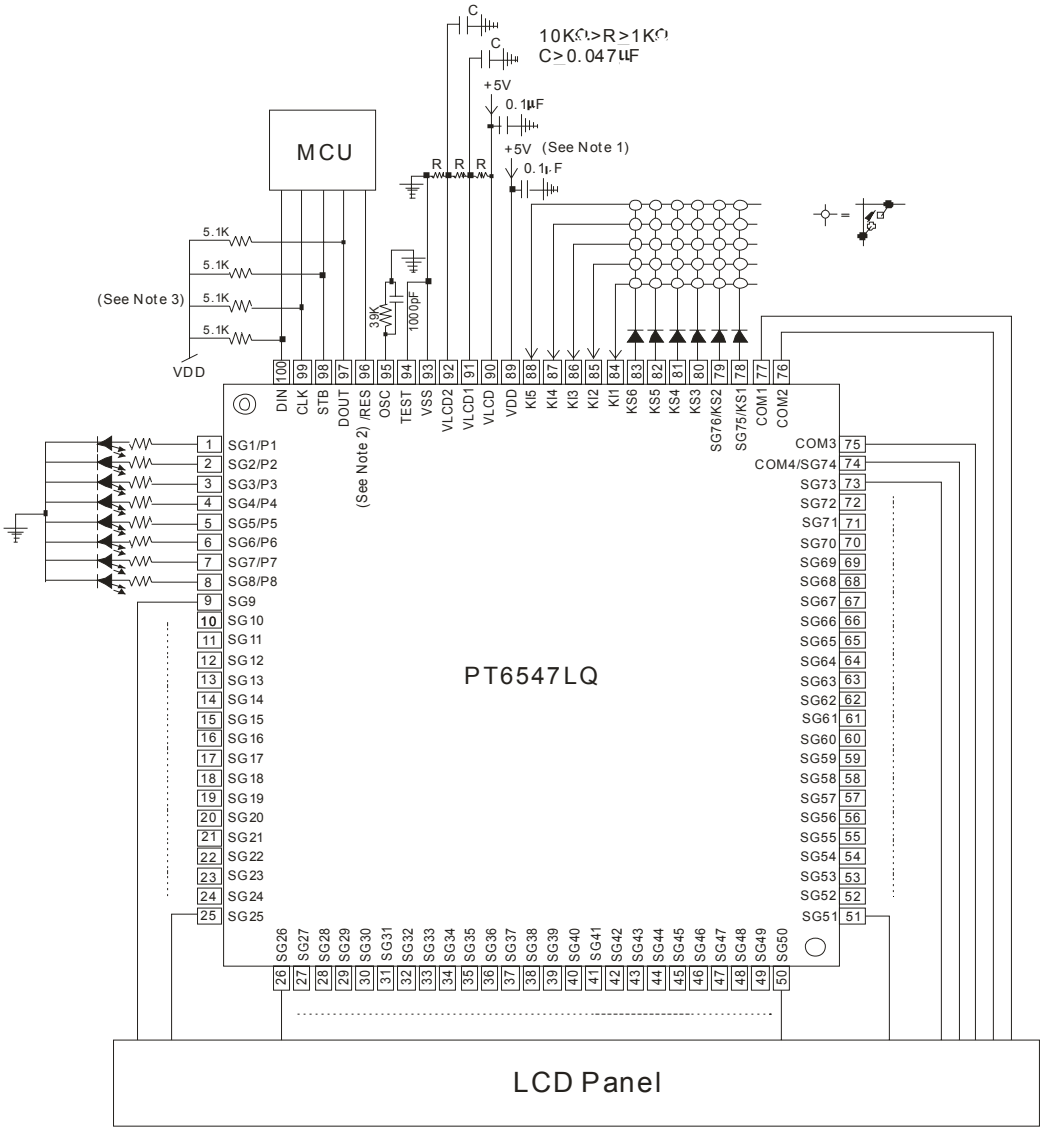


Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

APPLICATION CIRCUIT 4

1/3 DUTY 1/3 BIAS (FOR LARGE PANEL USE)

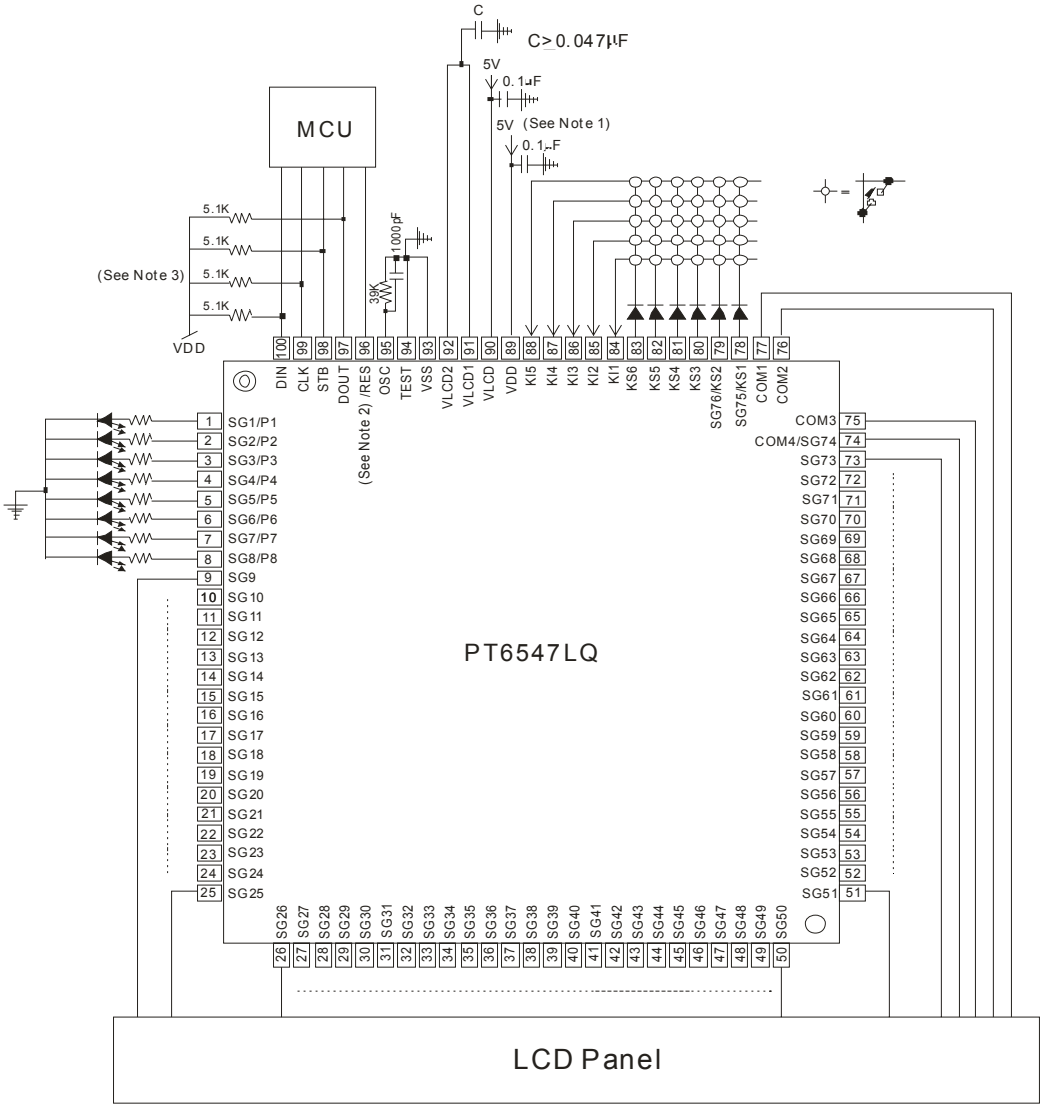


Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

APPLICATION CIRCUIT 5

1/4 DUTY 1/2 BIAS (FOR NORMAL PANEL USE)



Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

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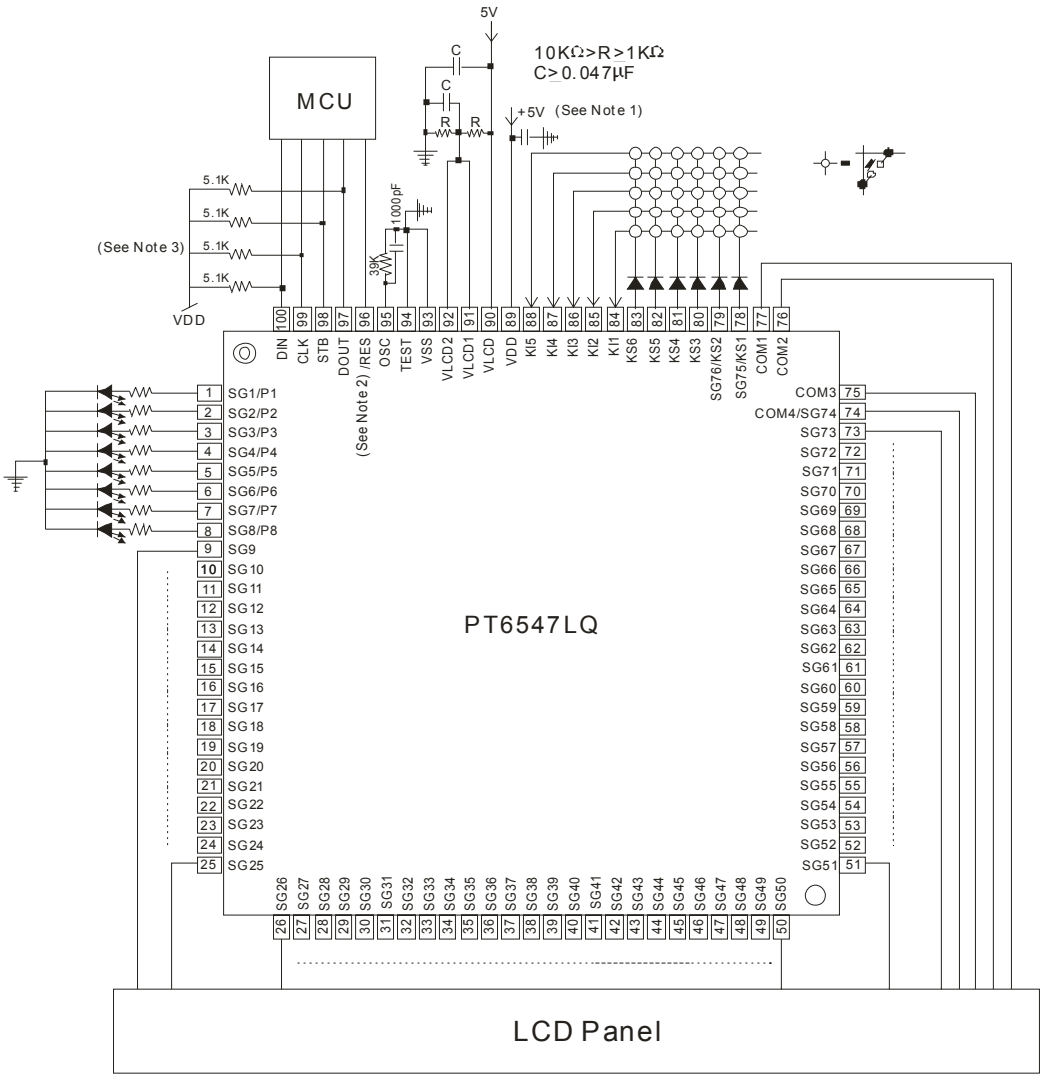
APPLICATION CIRCUIT 6

1/4 DUTY 1/2 BIAS (FOR LARGE PANEL USE)

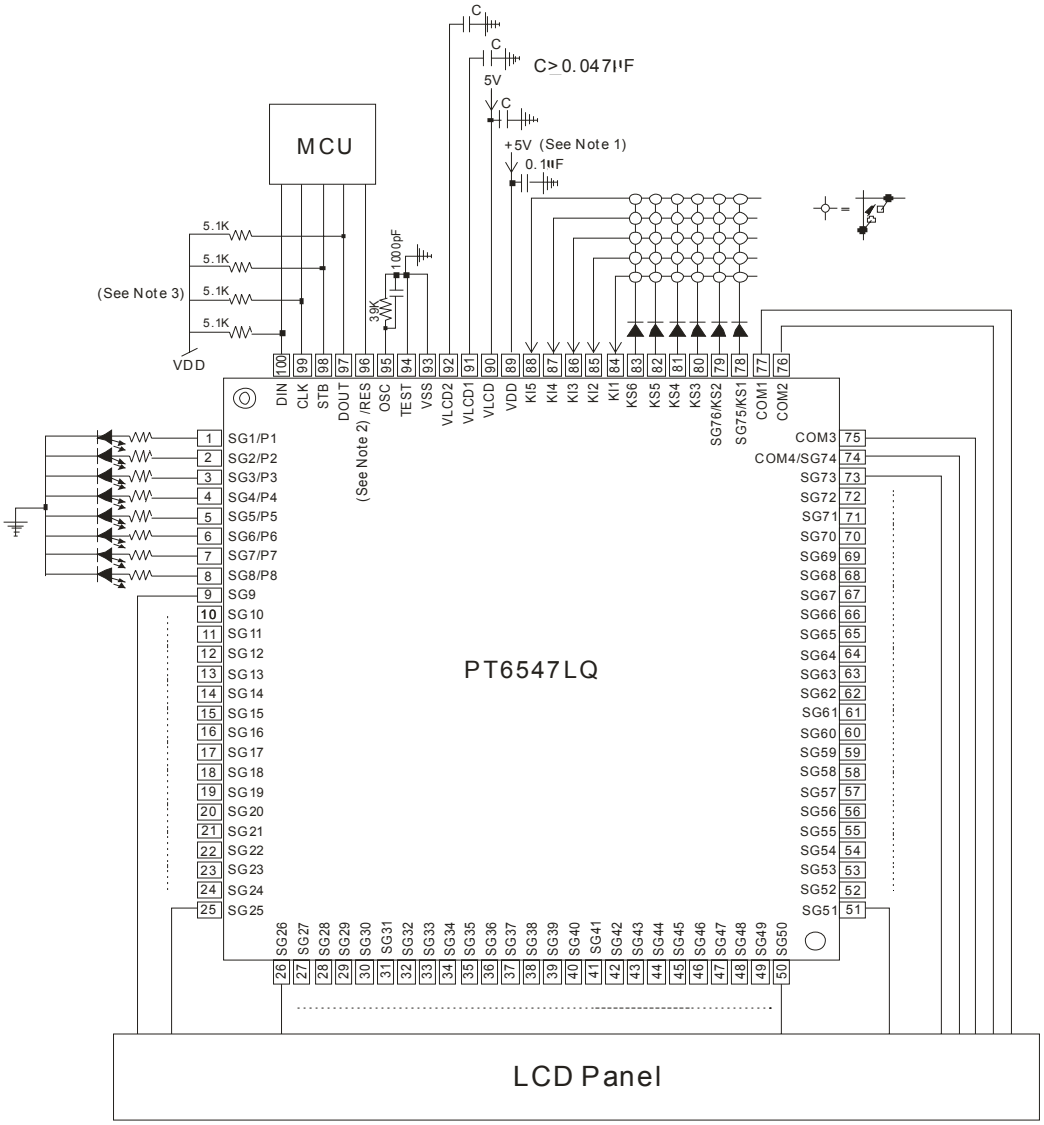


Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

APPLICATION CIRCUIT 7

1/4 DUTY 1/3 BIAS (FOR NORMAL PANEL USE)

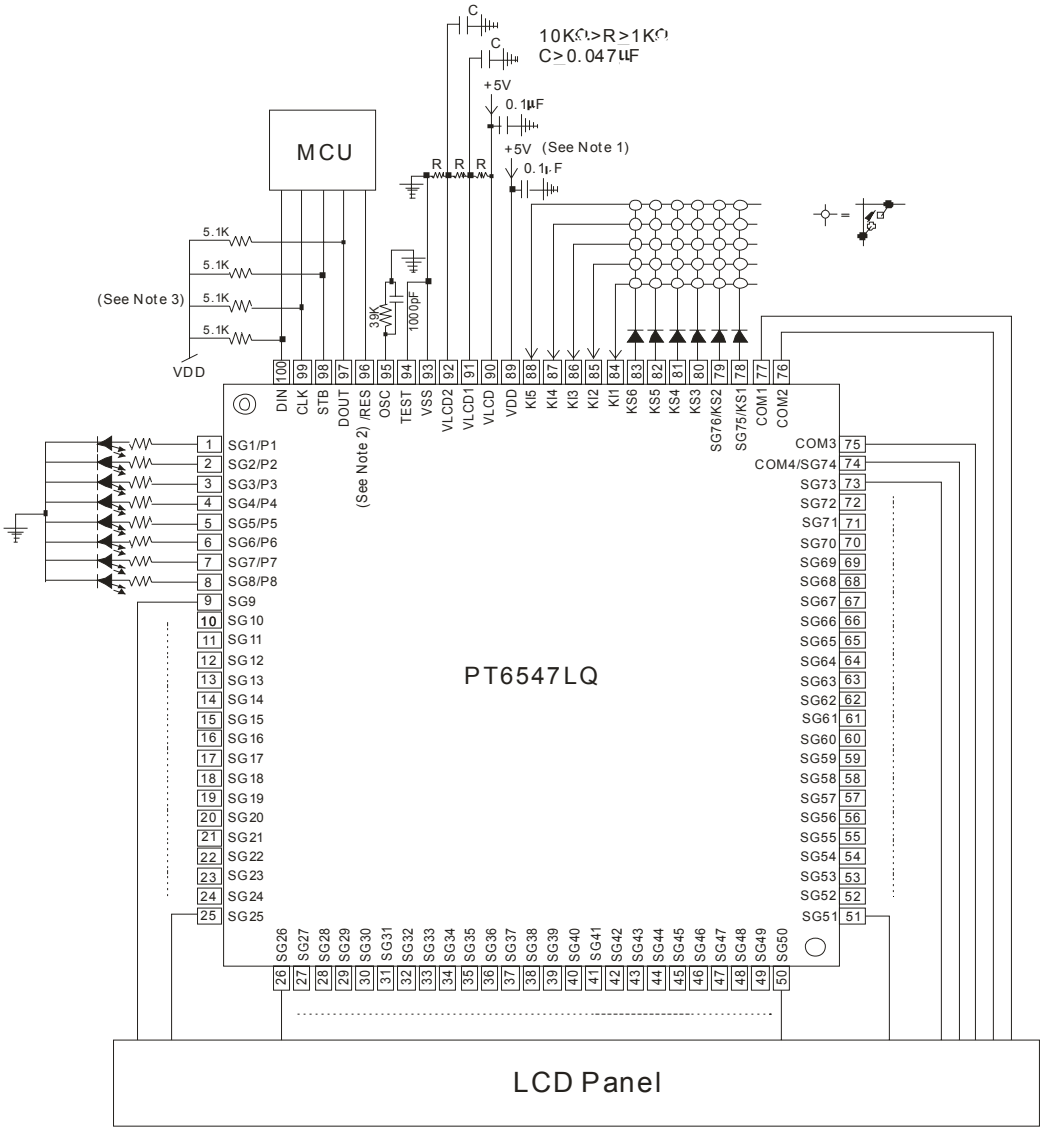


Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

APPLICATION CIRCUIT 8

1/4 DUTY 1/3 BIAS (FOR LARGE PANEL USE)



Notes:

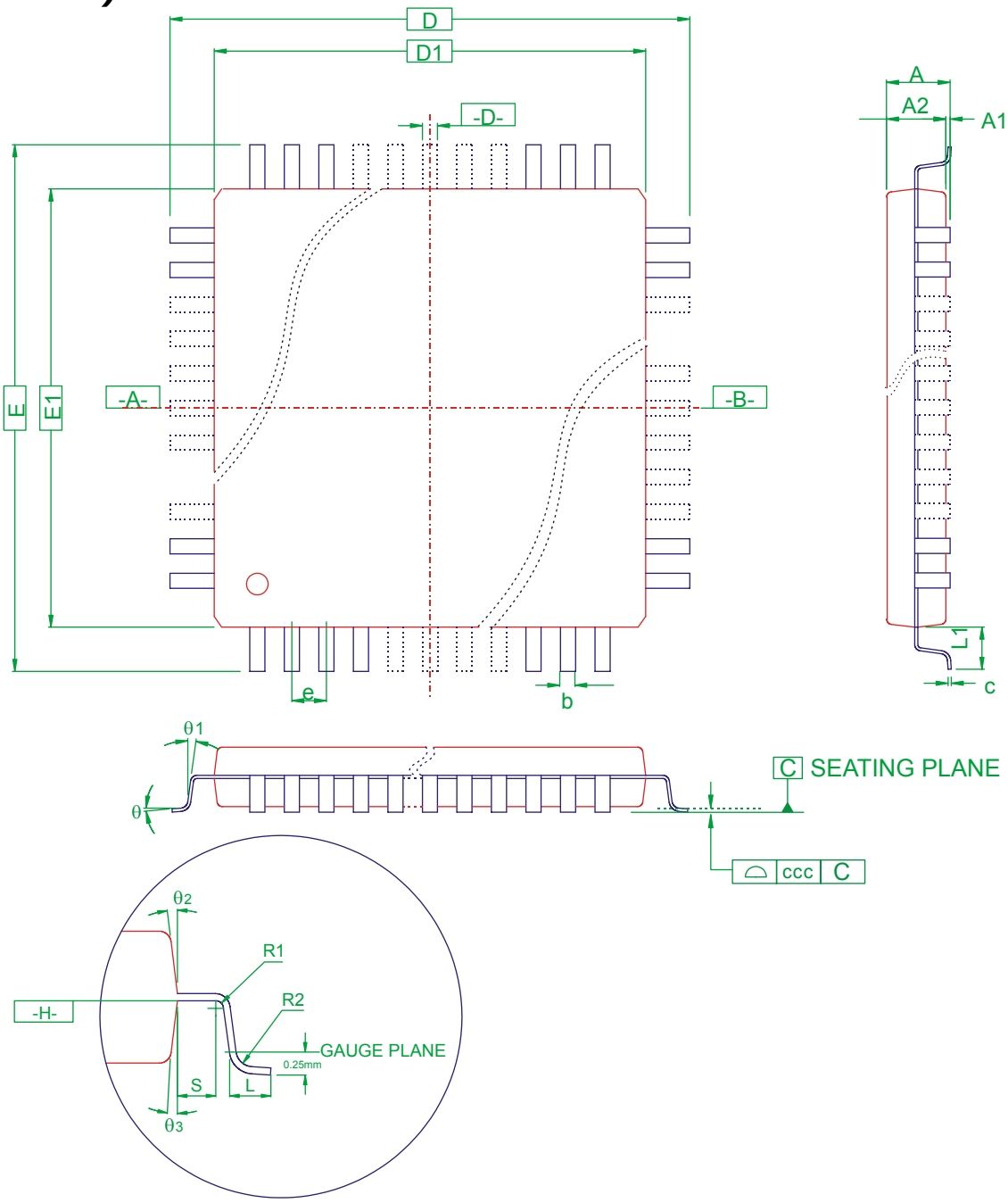
1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6547 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DOUT pin is an open-drain output and therefore needs a pull-up resistor. This resistor be between 1K to 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6547LQ	100 Pins, LQFP	PT6547LQ

PACKAGE INFORMATION

100 PINS, LQFP PACKAGE (BODY SIZE: 14MM X 14MM, PITCH:0.50MM, THK: 1.40MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	.027
D		16.00 BSC.	
D1		14.00 BSC.	
e		0.50 BSC.	
E		16.00 BSC.	
E1		14.00 BSC.	
θ	0º	3.5º	7º
θ1	0º	-	-
θ2	11º	12º	13º
θ3	11º	12º	13º
C	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
ccc		0.08	

Notes:
1. Dimensioning and tolerancing per ASMEY14.5-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusions is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mismatch.
5. Details of Pin1 identifier are optional but must be located within the zone indicated.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
7. Exact shape of each corner is optional.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Controlling Dimension: Millimeters
10. Refer to JEDEC MS-026 Variation BED

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