NB3U23C

1.2 V Dual Channel CMOS Buffer / Translator

ON Semiconductor®

http://onsemi.com

Description

The NB3U23C is a 2−input, 2−output buffer/voltage translator for UFS (Universal Flash Storage) in portable consumer applications such as mobile phones, tablets, cameras, etc. This dual channel CMOS buffer accepts 1.8 V CMOS input and translates it to 1.2 V CMOS output. The device is powered using single supply of 1.2 V ±5%.

The NB3U23C is packaged in 2 ultra−small 6−pin packages: the 6 pin SC70 and a 6 pin thin DFN package.

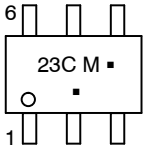
Features

- Operating Frequency: 52 MHz (Max)
- Propagation Delay: 5 ns (Max)
- Low Standby Current: < 10 μA at 1.2 V V_{DD}
- Low Phase Noise Floor: −150 dBc/Hz (Typ)
- Rise/Fall Times (tr/tf): 2 ns (Max)
- ESD Protection Exceeds JEDEC Standards
  - 2000 V Human−Body Model (JS−001−2012)
  - 200 V Machine Model (JESD22−A115C)
  - 1000 V Charged−Device Model (JESDC101E)
- Operating Supply Voltage Range (V_{DD}): 1.2 V ±5%
- Operating Temperature Range (Industrial): −40°C to 85°C
- This is a Pb−Free Device

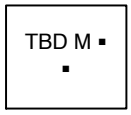
MARKING DIAGRAMS

1

SC−70
SQ SUFFIX
CASE 419B



UDFN−6
MN SUFFIX
PRELIMINARY



23C = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

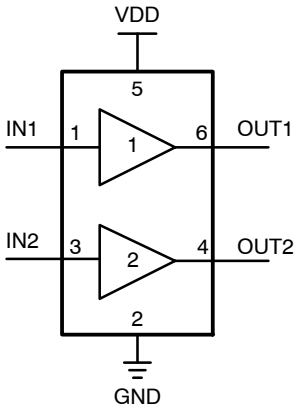


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

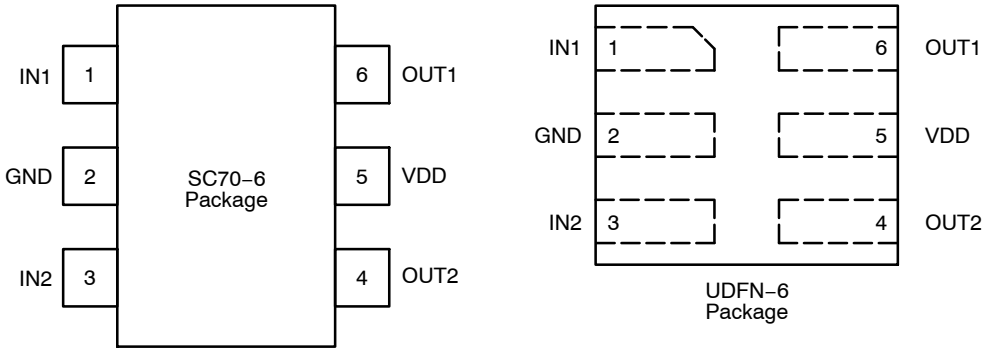


Figure 2. Pinout Diagram (Top Views)

Table 1. PIN DESCRIPTION

Number	Name	Description
1	IN1	Input Clock Signal − Channel 1
2	GND	Power Supply Ground (0 V)
3	IN2	Input Clock Signal − Channel 2
4	OUT2	Output − Channel 2
5	VDD	Power Supply Voltage
6	OUT1	Output − Channel 1

Table 2. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model Charge Device Model	2 kV min 200 V min 1 kV min
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		120
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test II		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Supply Voltage			3.6	V
V_{in}	Input Voltage			$-0.5 \le V_I \le 2.5$	V
I_D	Output Current			25	mA
T_A	Operating Temperature Range, Industrial			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm (Note 3)	SC70−6 UDFN−6	210 126 TBD	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	SC70−6 UDFN−6	100 TBD	°C/W
T_{sol}	Wave Solder			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 4. ELECTRICAL CHARACTERISTICS (VDD = 1.2 ±5% V, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DIDD	Power Supply Current (Single Channel Switching @ 52 MHz)	C_L = 20 pF C_L = 5 pF C_L = 1 pF		2.5 1.5 1		mA
	Power Supply Current (Both Channels Switching @ 52 MHz)	C_L = 20 pF C_L = 5 pF C_L = 1 pF		5 3 2		mA
I_{off}	Standby Current	Vi = V_{IH} Max or GND; V_{DD} = 1.2 V, No Output Load			10	μA
V_{IH}	Input High Voltage		0.65 * VDD		1.98	V
V_{IL}	Input Low Voltage		0		0.35 * VDD	V
V_{OH}	Output High Voltage	C_L = 20 pF R_L = 100 kΩ	0.75 * VDD		VDD	V
V_{OL}	Output Low Voltage	C_L = 20 pF R_L = 100 kΩ	0		0.25 * VDD	V
C_{in}	Input Capacitance				5	pF
F_{clk}	Operating Frequency Range		0		52	MHz
t_{PD}	Propagation Delay	INx to OUTx C_L = 20 pF, R_L = 100 kΩ			5	ns
	Phase Noise Floor Density (Notes 4 and 5)	C_L = 20 pF R_L = 100 kΩ		−150		dBc/Hz
	Additive RMS Phase Jitter (Notes 5 and 6)	C_L = 20 pF R_L = 100 kΩ Offset Frequency Range: 50 kHz to 10 MHz		0.15	0.25	ps
DC	Output Duty Cycle (Note 7)	Input Duty Cycle = 50%, Min Input Slew Rate = 1 V/ns	45		55	%
tr/tf	Output Rise/Fall Times	0.2 * V_{DD} to 0.8 * VDD C_L = 20 pF R_L = 100 kΩ			2	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. White noise floor.
5. This parameter refers to the random jitter only.
6. The output RMS phase jitter can be calculated using the following equation:
   $(\text{Output RMS Phase Jitter})^2 = (\text{Input RMS Phase Jitter})^2 + (\text{Additive RMS Phase Jitter})^2$
7. Measured with input voltage swing from 0 V to 1.8 V.

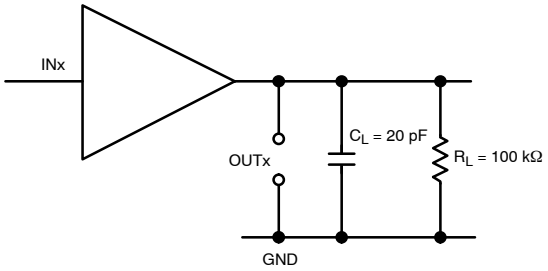


Figure 3. Typical Test Setup for Evaluation

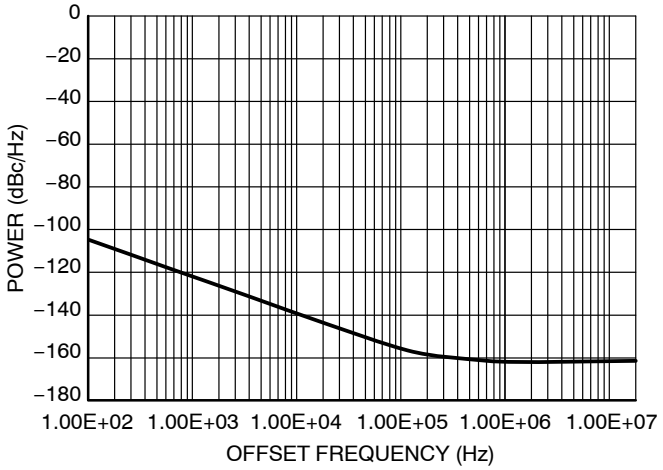


Figure 4. Typical Phase Noise Plot at 50 MHz Carrier Frequency

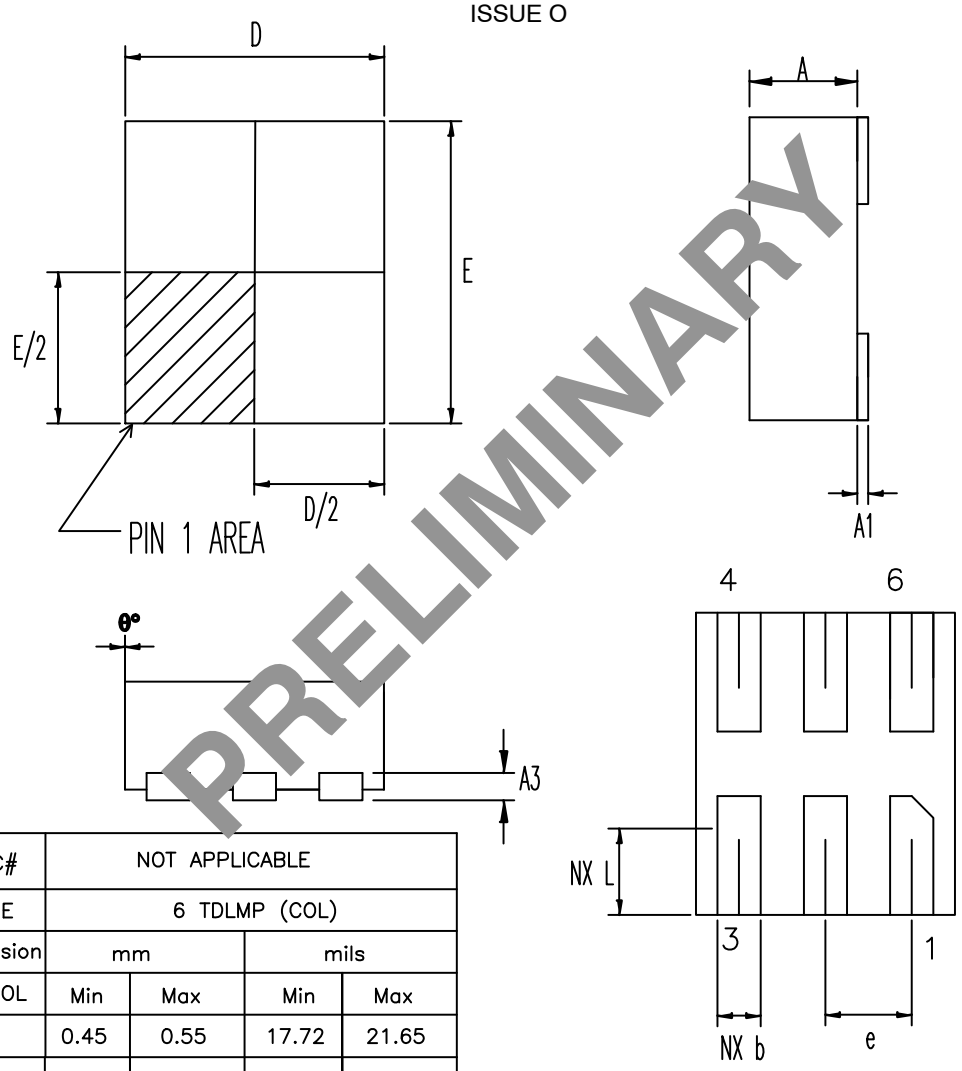
ORDERING INFORMATION

Device	Package	Shipping†
NB3U23CSQTCG	SC−70−6 (Pb−Free)	3000 / Tape & Reel
NB3U23CMNTBG	UDFN−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UDFN−6, 1.4 x 1.2, 0.5
CASE TBD
ISSUE O



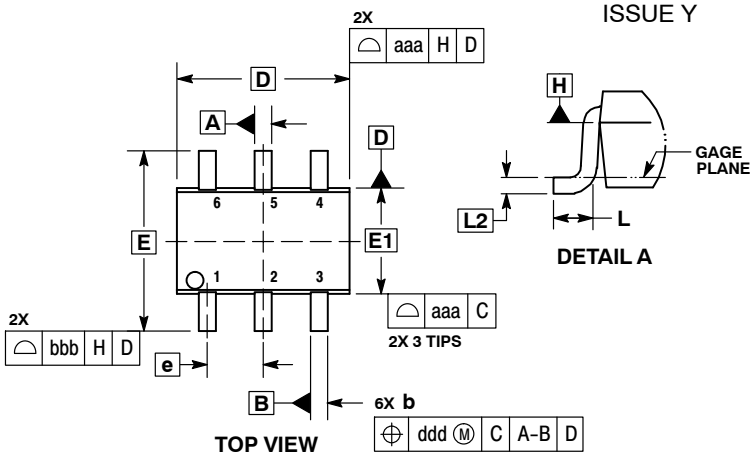
JEDEC#	NOT APPLICABLE			
TYPE	6 TDLMP (COL)			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.45	0.55	17.72	21.65
A1	0	0.05	0	1.97
A3	0.102	0.153	4.02	9.95
D	1.15	1.25	45.28	49.21
E	1.35	1.45	53.15	57.09
D2	−	−	−	−
E2	−	−	−	−
e	0.4 BSC		15.75 BSC	
NX b	0.15	0.25	5.91	9.84
NX L	0.5	0.6	19.69	23.62
θ°	0°	5°	0°	5°
ND	3			
NE	0			

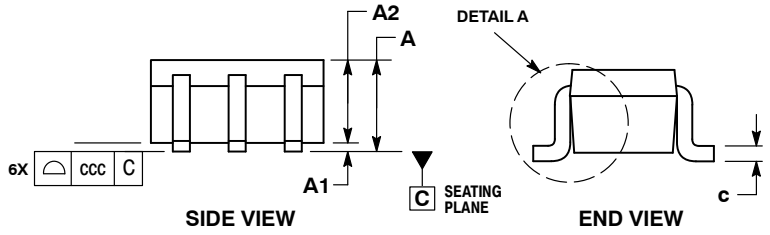
NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF PLATING MATERIAL
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95−1 SPP−012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

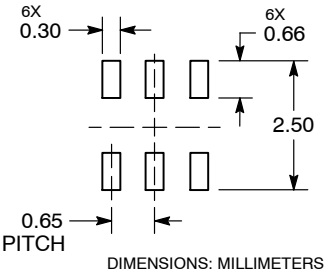




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative