256K × 16 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K × 16 bits RAM port
  512 × 16 bits SAM port
- **Performance range:**

Parameter \ Speed		-6	-70	-80
RAM access time (t_{RAC})		60ns	70ns	80ns
RAM access time (t_{CAC})		15ns	20ns	20ns
RAM cycle time (t_{RC})		110ns	130ns	150ns
RAM page cycle (t_{PC})	KM4216C257	40ns	45ns	50ns
	KM4216V257	40ns	45ns	50ns
SAM access time(t_{SCA})		15ns	17ns	20ns
SAM cycle time (t_{SCC})		18ns	20ns	25ns
RAM active current	KM4216C257	120mA	110mA	100mA
	KM4216V257	110mA	100mA	90mA
SAM active current	KM4216C257	50mA	45mA	40mA
	KM4216V257	40mA	35mA	30mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **2 $\overline{CAS}$ Byte/Word Read/Write Operation**
- **8 Column Block Write (BW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single + 5V ±10% Supply Voltage (KM4216C257)**
- **Single + 3.3V ±10% Supply Voltage (KM4216V257)**
- **Plastic 64-Pin 525 mil SSOP (0.8mm pin pitch)**
- **Plastic 70-pin 400mil TSOP II(0.65mm pin pitch) (Forward and Reverse Type)**

- **Device Options** • **Part Marking**
  -. **Low Power Dissipation**
  Extended CBR Refresh (64ms) **L**
  -. **Low Low Power Dissipation**
  Self Refresh (128ms) **F**
- **Low Vcc(3.3V) Part Name: KM4216V257**

GENERAL DESCRIPTION

The Samsung KM4216C/V257 is a CMOS 256K × 16 bit Dual Port DRAM. It consists of a 256K × 16 dynamic random access memory (RAM) port and 512 × 16 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 8192 bits. It operates like a conventional 256K × 16 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access, 2 $\overline{CAS}$ Byte/word Read/write operation and Block Write capabilities.

The SAM port consists of sixteen 512 bit high speed shift registers that are connected to the RAM array through a 8192 bit data transfer gate The SAM port has serial read capability.

Data may be internally transferred from the RAM to SAM ports using read, and programmable (Stop Register) Split Transfers.

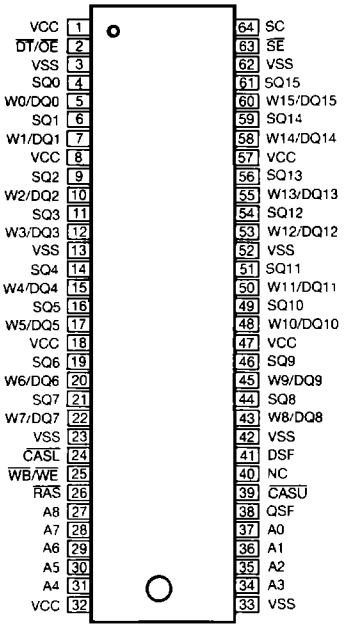
Refresh is accomplished by familiar DRAM refresh modes. The KM4216C/V257 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

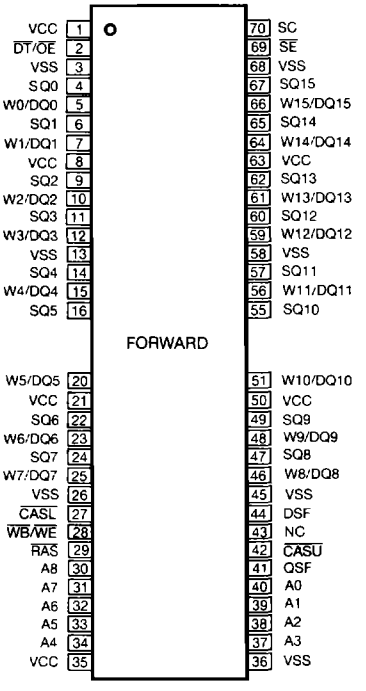
Pin Name		Pin Function
SC		Serial Clock
SQ_0-SQ_{15}		Serial Data Output
$\overline{DT}/\overline{OE}$		Data Transfer/Output Enable
$\overline{CASL}$, $\overline{CASU}$		Column Address Strobe (Lower /Upper)
$\overline{RAS}$		Row Address Strobe
$\overline{WB}/\overline{WE}$		Write Per Bit/Write Enable
W_0/DQ_0-W_{15}/DQ_{15}		Data Write Mask/Input/Output
$\overline{SE}$		Serial Enable
A_0-A_8		Address Inputs
DSF		Special Function Control
V_{CC}	KM4216C257	Power (+5V)
	KM4216V257	Power (+3.3V)
V_{SS}		Ground
QSF		Special Flag Out
N.C		No Connection

PIN CONFIGURATION (TOP VIEWS)

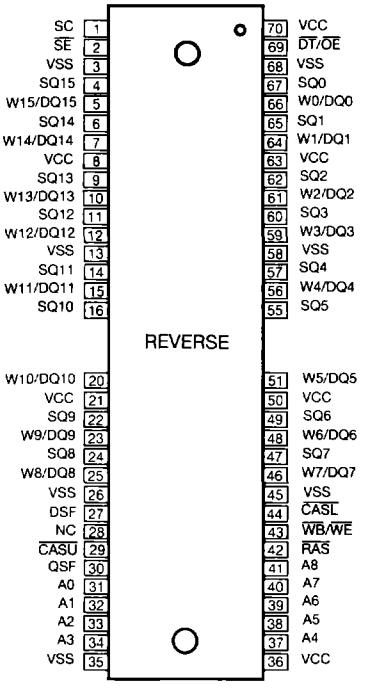
• **KM4216C/V257G/GL/GF**



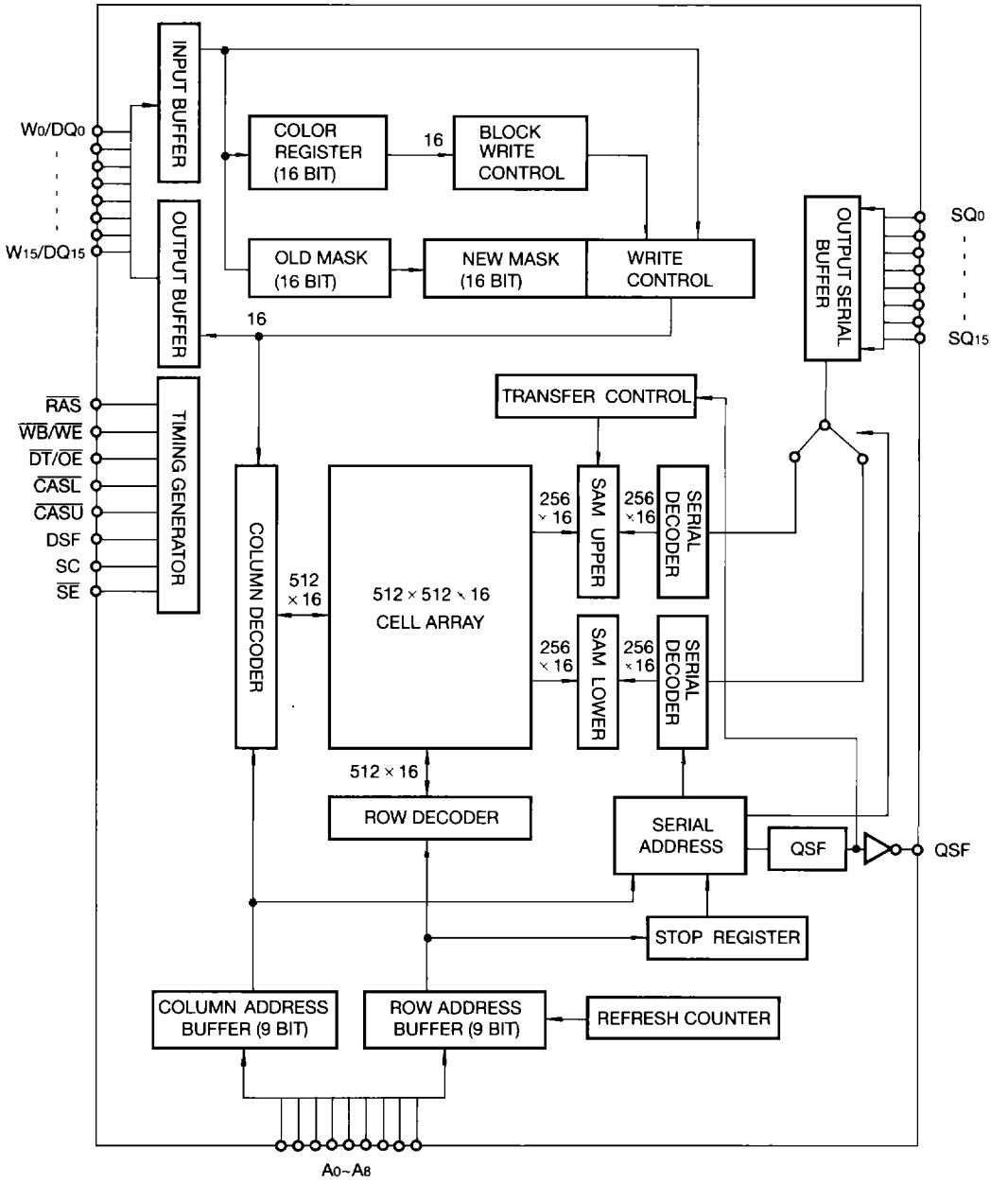
• **KM4216C/V257T/TL/TF**



• **KM4216C/V257R/RL/RF**



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic	RAS ↓				CAS ↓	Address		DQi Input		Register		Function
Code	CAS	DT/OE	WE	DSF	DSF	RAS	CAS	RAS	CAS/WE	Mask	Color	
CBRS (Note 1.3)	0	×	0	1	-	Stop (Note4)	-	×	-	-	-	CBR Refresh/ Stop (No reset)
CBRN (Note 1)	0	×	1	1	-	×	-	×	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	×	×	0	-	×	-	×	-	-	-	CBR Refresh (Option reset)
ROR	1	1	×	0	-	ROW	-	×	-	-	-	RAS-only Refresh
RT	1	0	1	0	×	ROW	Tap	×	×	-	-	Read Transfer
SRT	1	0	1	1	×	ROW	Tap	×	×	-	-	Split Read Transfer
RWM	1	1	0	0	0	ROW	Col.	WMi	Data	Use	-	Masked write (New/Old Mask)
BWM	1	1	0	0	1	ROW	Col.	WMi	Column Mask	Use	Use	Masked Block Write (New/Old Mask)
RW	1	1	1	0	0 (Note6)	ROW	Col.	×	Data	-	-	Read or Write
BW	1	1	1	0	1	ROW	Col.	×	Column Mask	-	Use	Block Write
LMR (Note 2)	1	1	1	1	0	ROW (Note7)	×	×	WMi	Load (Note5)	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	ROW (Note7)	×	×	Color		Load	Load Color Register

X: Don't Care, - : Not Applicable, Tap:SAM Start (Column) Address, WMi : Write Mask Data (i=0~15)
RAS only refresh does not reset Stop or LMR functions.

Notes:
(1) CBRS, CBRN and CBRR all perform CAS-before-RAS refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, RWM and BWM use old mask. (Use CBRR reset to new mask, CBRS or CBRN to perform CAS-before-RAS refresh while using Old mask)
(3) After CBRS Cycle, SRT use STOP Register as a boundary address.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, Mask Register is only changed by the another LMR or CBRR cycle.
(6) In the case of read cycle, DSF is don't care
(7) The ROW that is addressed will be refreshed, but a ROW address is not reguired.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating		Unit
		KM4216C257	KM4216V257	
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	-0.5 to V_{CC}+0.5	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to + 150	55 to +150	°C
Power Dissipation	P_D	1	0.6	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	KM4216C257			KM4216V257			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1V	2.0		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	-0.3		0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq V_{CC}$+0.5(0.3*1) all other pins not under test=0 volts).	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

Note) *1 : KM4216V257

CAPACITANCE (V_{CC}=5V, f=1MHz, T_A=25° C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_{15}/DQ_{15})	C_{DQ}	2	7	pF
Output Capacitance (SQ_0~SQ_{15}, QSF)	C_{SQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless other wise noted)

Parameter (RAM Port)	SAM port	Symbol	KM4216C257			KM4216V257			Unit
			-6	-7	-8	-6	-7	-8	
Operating Current*1	Standby*4	I_{CC1}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)	Active	I_{CC1A}	160	145	130	140	125	110	mA
Standby Current	Standby*4	I_{CC2}	10	10	10	10	10	10	mA
($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$=$V_{IH}$	Active	I_{CC2A}	50	45	40	40	35	30	mA
DSF=V_{IL})	Standby*4	I_{CC2C}*2	200	200	200	200	200	200	μA
	Standby*4	I_{CC2C}*3	150	150	150	150	150	150	μA
$\overline{RAS}$ Only Refresh Current*1	Standby*4	I_{CC3}	120	110	100	110	100	90	mA
($\overline{CAS}$-V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min	Active	I_{CC3A}	160	145	130	140	125	110	mA
Fast Page Mode Current*1	Standby*4	I_{CC4}	110	100	90	100	90	80	mA
($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cyciing @t_{PC}=min	Active	I_{CC4A}	150	135	120	130	115	110	mA
CAS Before-RAS Refresh Current*1	Standby*4	I_{CC5}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min	Active	I_{CC5A}	160	145	130	140	125	110	mA
Data Transfer Current *1	Standby*4	I_{CC6}	140	130	120	130	120	110	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC6A}	180	165	150	160	145	130	mA
Block Write Cycle Current *1	Standby*4	I_{CC7}	120	110	100	110	100	90	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC7A}	160	145	130	140	125	110	mA
Color Register Load Current *1	Standby*4	I_{CC8}	110	90	80	90	80	70	mA
($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min)	Active	I_{CC8A}	140	125	110	120	105	90	mA
Battery Back Up Current *2 $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycling or $\leq V_{IL}$ $\overline{RAS}$=t_{RAS}(min) to 1μs t_{RC}=125 μs (64ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, DSF$\geq V_{IH}$ or$\leq V_{IL}$	Standby*4	I_{CC9}	300	300	300	300	300	300	μA
Self Refresh Current *3 $\overline{RAS}$,$\overline{CAS}\leq$0.2V(128ms for 512 rows) $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, A_0~A_8, DSF$\geq V_{CC}$ - 0.2v or$\leq$0.2V DQ0~15=V_{CC}-0.2V, 0.2V or OPEN	Standby*4	I_{CC10}	250	250	250	250	250	250	μA

Note *1 Real values dependent on output loading and cycle rates. Specified values are obtained with the output open, I_{CC} is specified as average current.

In I_{CC1}, I_{CC3}, I_{CC6}, I_{CC7}, I_{CC8}, adress transition should be changed only once while RAS=V_{IL}.

In I_{CC4}, Address transition should be changed only once while $\overline{CAS}$=V_{IH}

*2 KM4216C257L only : $V_{IH}\geq V_{CC}$-0.2V, $V_{IL}\leq$0.2V

*3 KM4216C257F only : $V_{IH}\geq V_{CC}$ -0.2V, $V_{IL}\leq$0.2V,

*4 SAM standby condition : $\overline{SE}\geq V_{IH}$, SC $\leq V_{IL}$ or $\geq V_{IL}$

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, KM4216C257 : V_{CC}=5.0V±10%, KM4216V257 : 3.3V±10%,)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		200		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,5,11
Access time from column address	t_{AA}		30		35		40	ns	3,5,6
Access time from CAS precharge	t_{CPA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	3
Transition time(rise and fall)	t_T	2	50	2	50	2	50	ns	7
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	2
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	17
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	16
Column address hold time	t_{CAH}	10		12		15		ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		ns	
Write command pulse width	t_{WP}	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	19
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	10		12		15		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8,18
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		60		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	20
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		10		10		ns	21
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
Access time from output enable	t_{OEA}		15		20		20	ns	
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output Buffer turn-off delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	7
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period (512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF set-up time referenced to $\overline{RAS}$	t_{FSR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$	t_{RFH}	10		10		15		ns	
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	10		10		15		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	110		130		150		ns	15
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	0		0		0		ns	15
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ low set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold referenced to $\overline{RAS}$ (real time read transfer)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold referenced to $\overline{CAS}$ (real time read transfer)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold referenced to column address (real time read transfer)	t_{ATH}	20		25		30		ns	
$\overline{DT}$ precharge time	t_{TP}	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	t_{RSD}	60		70		80		ns	

AC CHARACTERISTICS (Continued)

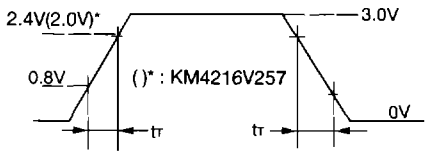
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to first SC delay (read transfer)	tCSD	25		30		40		ns	
Col. Address to first SC delay (read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	tTSD	10		10		15		ns	
LAST SC to $\overline{RAS}$ set-up time	tSRS	20		20		20		ns	
SC cycle time	tSCC	18		20		25		ns	14
SC pulse width (SC high time)	tSC	5		7		7		ns	
SC precharge (SC low time)	tSCP	5		7		7		ns	
Access time from SC	tSCA		15		17		20	ns	4
Serial output hold time from SC	tSOH	5		5		5		ns	
Access time from $\overline{SE}$	tSEA		15		17		20	ns	4
$\overline{SE}$ pulse width	tSE	20		20		25		ns	
$\overline{SE}$ precharge time	tSEP	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	7
Split transfer set-up time	tSTS	20		25		25		ns	
Split transfer hold time	tSTH	20		25		25		ns	
SC-QSF delay time	tSQD		20		25		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		25		25	ns	
$\overline{RAS}$-QSF delay time	tRQD		70		75		80	ns	
$\overline{CAS}$-QSF delay time	tCQD		35		35		40	ns	
$\overline{DT}$ to $\overline{RAS}$ Precharge time	tTRP	40		50		60		ns	

NOTES

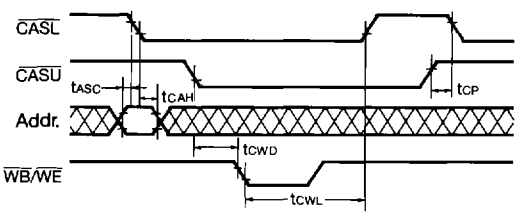
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ 8 SC cycles before proper device operation is achieved.($\overline{DT}/\overline{OE}$=High) if the intenal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required in stead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input siganl transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1TTL load and 50pF.
   D_{OUT} Comparator level : V_{OH}/V_{OL}=2.0V/0.8V.
4. SAM port outputs are measured with a load equivalent to 1TTL load and 30pF.
   D_{OUT} comparator level:V_{OH}/V_{OL}=2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. This parameters define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the first $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them high before or at the same time as the V_{CC} supply is turned on.
    After power-up, initial status of chip is described below

Pin or REGISTER	STATUS
QSF	Hi-Z
Color Registe	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Hi-Z
SDQi	Hi-Z

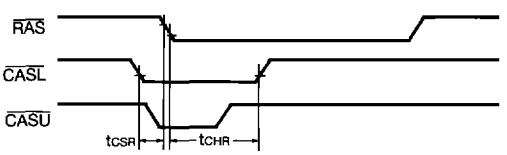
13. Recommended operating input condition.



    Input pulse levels are from 0.0V to 3.0Volts.
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time=5.0ns
14. Assume t_T=3ns.
15. Self refresh parameter (KM4216C/V257F)
    512K cycle of burst refresh must be executed within 8ms before and after self-refresh in order to meet refresh specification.
16. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
17. t_{CP} is specified from the last $\overline{CAS}$ rising edge in tne previous cycle to the first $\overline{CAS}$ falling edge in the next cycle
18. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
19. t_{CWL} is specified from $\overline{WB}/\overline{WE}$ faliing edge to the earlier $\overline{CAS}$ rising edge.



20. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
21. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



DEVICE OPERATION

The KM4216C/V257 contains 4,194,304 memory locations. Eighteen address bits are required to address a particular 16 bit word in the memory array. Since the KM4216C/V257 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$). the column address strobe($\overline{CAS}$) and the valid row and coumn address inputs.

Operation of the KM4216C/V257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This the beginning of any KM4216C/V257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum RAS precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM4216C/V257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then tne access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}

The KM4216C/V257 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

DEVICE OPERATION (continued)

2$\overline{CAS}$ Byte/Word Read/Write Operation

The KM4216C/V257 has 2 $\overline{CAS}$ control pin, $\overline{CASL}$ and $\overline{CASU}$, and offers asynchronous Read/Write operation with lower byte (W_0/DQ_0~W_7/DQ_7) and upper bybe (W_8/DQ_8~W_{15}/DQ_{15}). This is called 2$\overline{CAS}$ Byte/Word Read/Write operation. This operation can be performed RAM Read in RAM write, Block write, Load Mask register, and Load Color register.

New Masked Write Per Bit

The New Masked Write Per Bit cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ and DSF low at the falling edge of $\overline{RAS}$. The mask data on the W_0/DQ_0~W_{15}/DQ_{15} pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM.

The mask data is valid for only one cycle. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ low after $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~W_{15}/DQ_{15} must keep the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.

If $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$, no masking operation is performed (see Figure2, 3). And If $\overline{CASL}$ is high during $\overline{WB}/\overline{WE}$ low, write operation of lower byte do not perform and if $\overline{CASU}$ is high, write operation of upper byte do not execute.

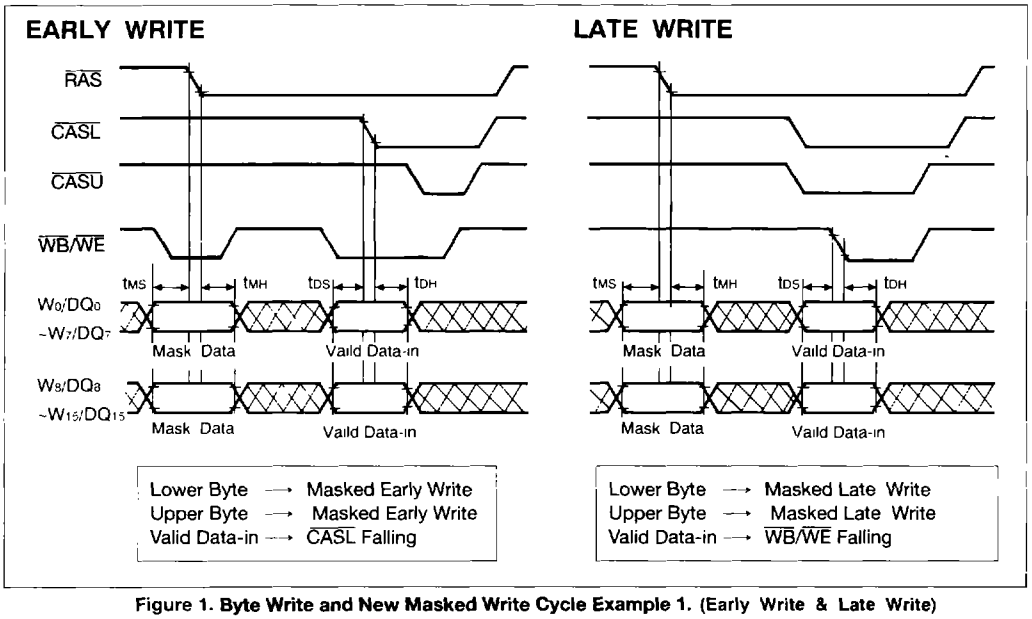


Figure 1. Byte Write and New Masked Write Cycle Example 1. (Early Write & Late Write)

DEVICE OPERATION (continued)

Load Mask Register(LMR)

The Load Mask Register operation loads the data present on the Wi/DQi pins into the Mask Data Register at the falling edge of $\overline{CAS}$ or $\overline{WB/WE}$.

The LMR cycle is performed if DSF high, $\overline{WB/WE}$ high at the $\overline{RAS}$ falling edge. And DSF low at the $\overline{CAS}$ falling edge. If an LMR is done, the KM4216C/V257 are set to old masked write mode.

Old Masked Write Per Bit

This mode is enabled through the Load Mask Register (LMR) cycle. If an LMR is done, all Masked write are Old Masked Write Per Bit and the I/O mask data wil be provided by the Mask Data Register (See Figure 4.)

The mask data is applied in the same manner as in New Masked write Per Bit mode.

Mask Data Register's content is changed by the another LMR. To reset the device back to the New Masked write mode, CBRR (CBR refresh with option reset) cycle must be performed. After power-up, the KM4216C/V257 Initializes in the New Masked write mode.

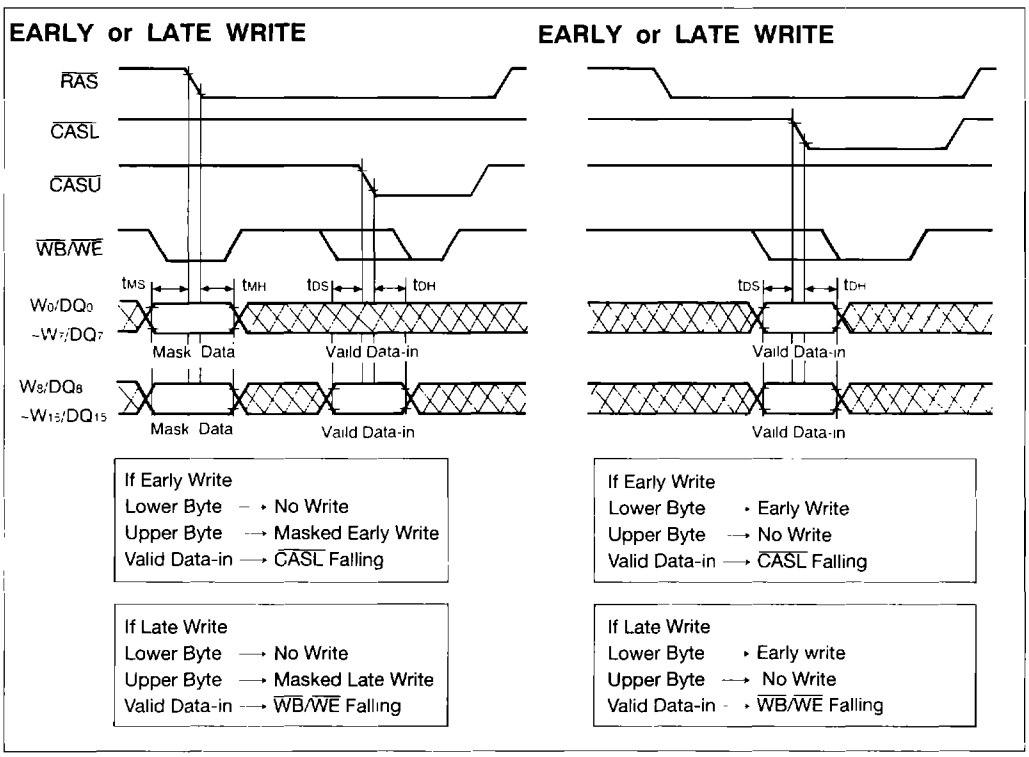


Figure 2. Byte Write and New Masked Write Cycle Example 2.

DEVICE OPERATION (continued)

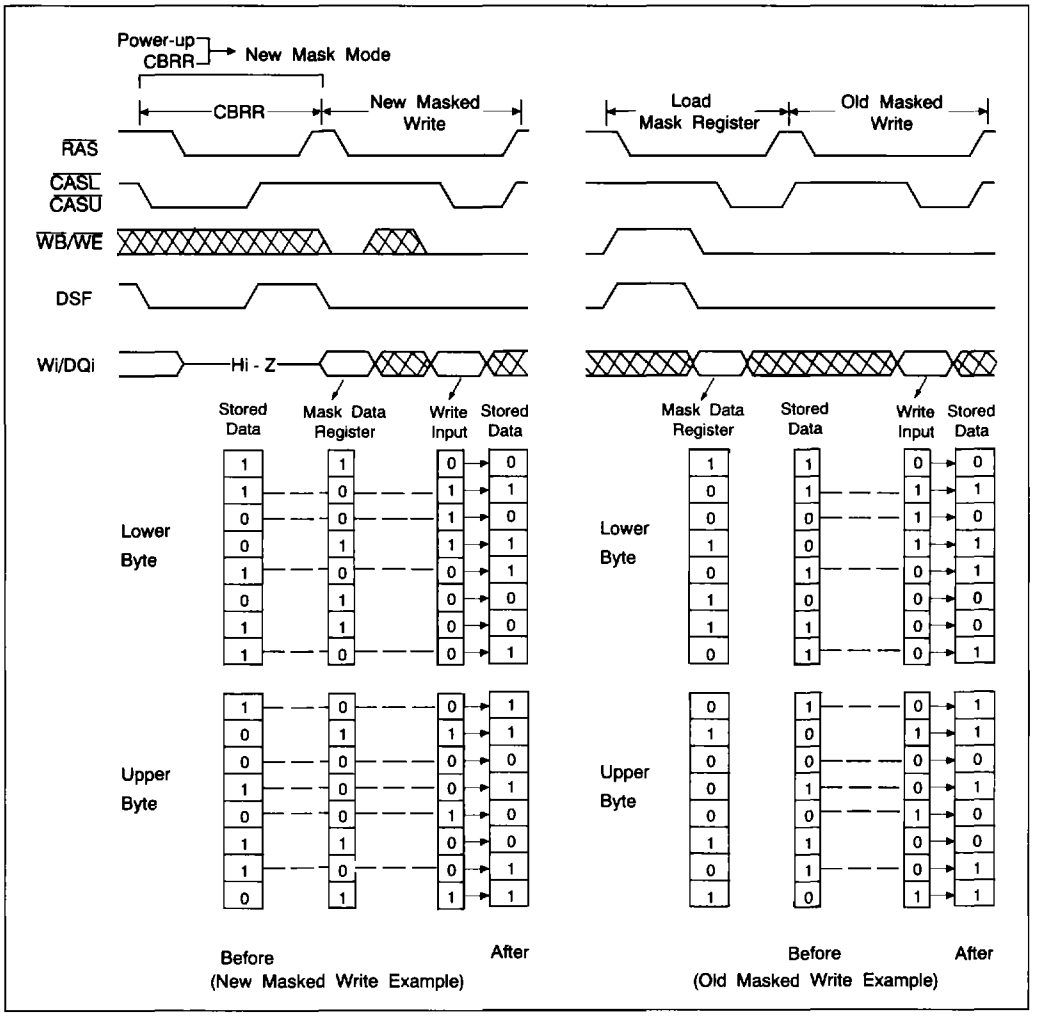


Figure 3. New Masked Write Cycle and Old Masked Write Cycle Example

Fast Page Mode

The KM4216C/V257 has Fast Page mode capability provides high speed read, write or read-modify-write access to all memory locations Within a selected row. In this cycle, read, write, read-modify write, and block write cycles can be mixed in any order.

In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

DEVICE OPERATION (continued)

Load Color Register(LCR)

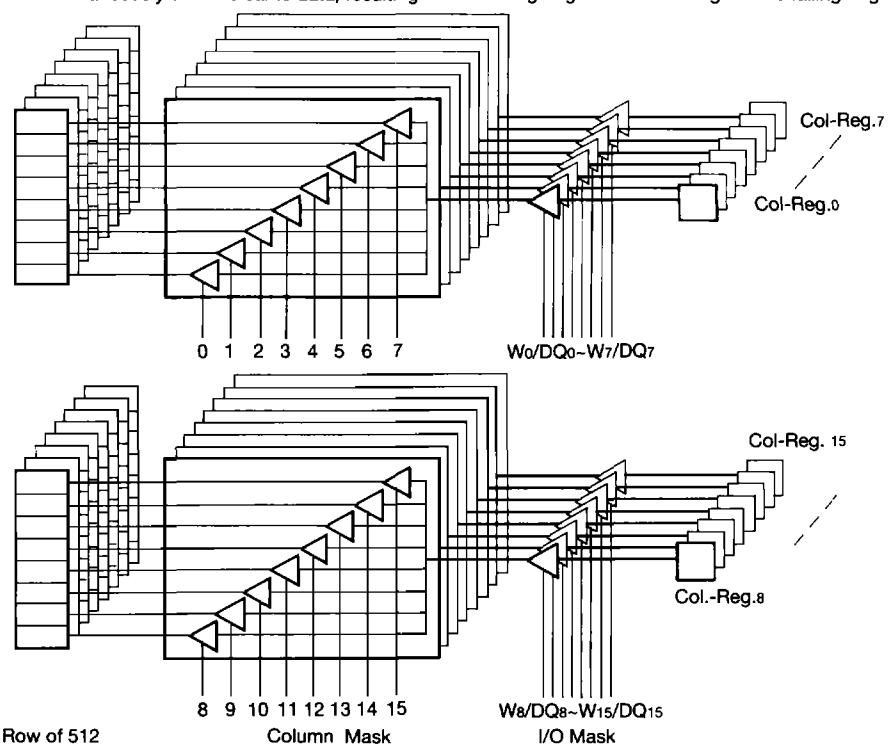
A Load Color register cycle is performed by keeping DSF high on the both falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded in the falling edge of $\overline{CAS}$(early write) or $\overline{WE}$(late write) via the W_0/DQ_0~w_7/DQ_7(Lower Byte), W_8/DQ_8~W_{15}/DQ_{15} (Upper Byte) pins. This data is used in Block Write cycles and remains unchanged until the next Load Color Register Cycle.

Block Write

In a Block write cycle 8 adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 16-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into 8 adjacent locations of the same row of each correspeonding bit plane(16). This result in a total of 128-bits Written in a single Block write cycle compared to 16-bit in a normal write cycle.

The Block write cycle is performed if DSF is low at the falling edge of $\overline{RAS}$ and high at the falling edge of $\overline{CAS}$.



	$\overline{RAS}$
W_0/DQ_0~7	Lower Block I/O Mask
W_8/DQ_8~15	Upper Block I/O Mask

	$\overline{CAS}$
A_0~A_2	Don't Care
W_0/DQ_0~7	Lower Block Column Select
W_8/DQ_8~15	Upper Block Column Select

A_2~A_0	Lower	Upper	Column Mask	
0 0 0	W_0/DQ_0	W_8/DQ_8	DQi=1	Column Enable
0 0 1	W_1/DQ_1	W_9/DQ_9		
0 1 0	W_2/DQ_2	W_{10}/DQ_{10}		
0 1 1	W_3/DQ_3	W_{11}/DQ_{11}		
1 0 0	W_4/DQ_4	W_{12}/DQ_{12}	DQi=0	Column Disable
1 0 1	W_5/DQ_5	W_{13}/DQ_{13}		
1 1 0	W_6/DQ_6	W_{14}/DQ_{14}		
1 1 1	W_7/DQ_7	W_{15}/DQ_{15}		

Figure 4. Block Write Scheme

DEVICE OPERATION (continued)

Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.
Since 8 columns are being written at a time, the minimum increment required for the column address is latched on the falling edge of $\overline{CAS}$, the 3 LSBs, A_0, A_1, and A_2 are ignored and only bits (A_3~A_8) are used to define the location of the first bit out of the eight to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_{15}/DQ_{15} pins provide column mask data. That is, for each of the eight bits in all 16 -bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_1/DQ_1=0, then the Color Register contents will be written into the first bit out of the eight, but the second remains unchanged. Fig. 4 shows the correspondence of each data line to the column mask bits.
A Masked Block Write cycle is identical to a New/old Masked Write-Per-bit cycle except that each of the 16-bit planes being masked is operating on 8 column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB/WE}$ must be low at the falling edge of $\overline{RAS}$. And DSF must be high on the falling edge of $\overline{CAS}$. In new mask mode, Mask data is latched into the device via the W_0/DQ_0~W_{15}/DQ_{15} pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle. In Old mask mode, I/O mask data will be provided by the Mask Data Register.

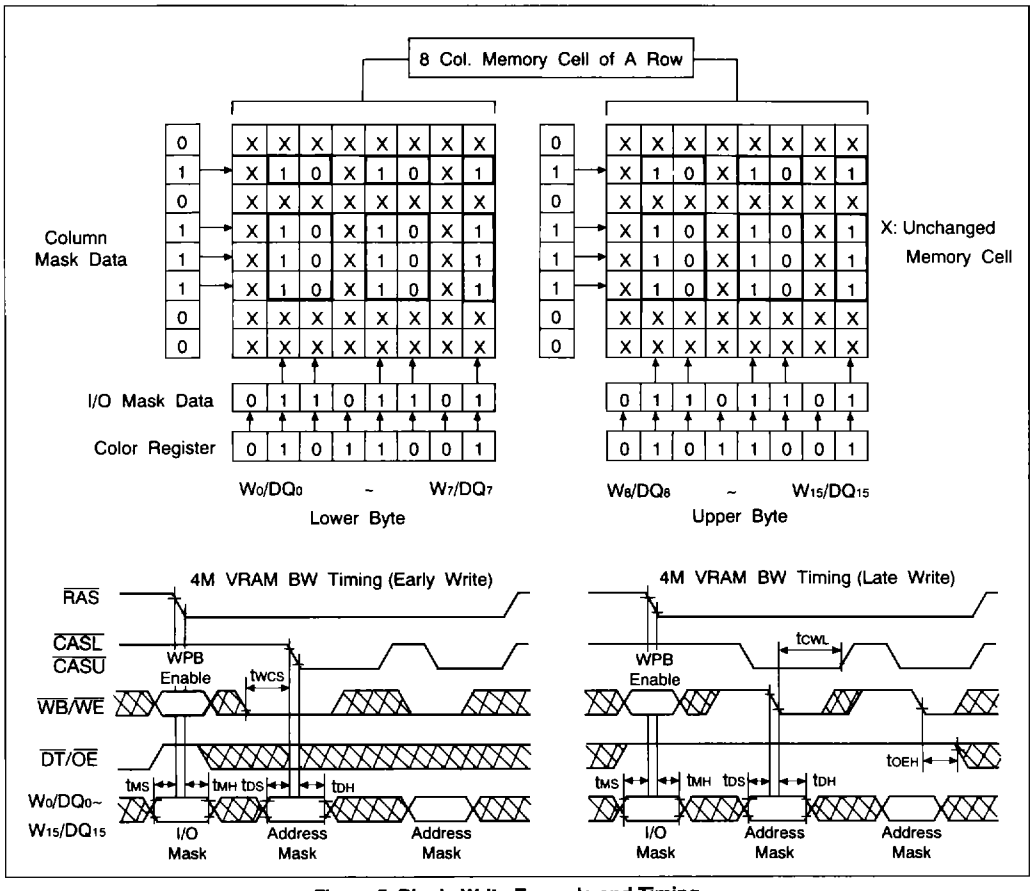


Figure 5. Block Write Example and Timing

DEVICE OPERATIONS (Continued)

Data Output

The KM4216C/V257 has three state output buffer Controlled by $\overline{DT}/\overline{OE}$ and $\overline{CAS}$,$\overline{RAS}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ low, the output state is in high impedance (High-z). In any cycle, the output goes low impedance state after t_{CLZ} of the first $\overline{CAS}$ falling edge. Invalid data may be present at the output duing the time after t_{CLZ} and the valid data appears at the output. The timing parameter t_{RAC}, t_{CAC} and t_{AA} specify when the valid data will be present at the output.

Refresh

The data in the KM4216C/V257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM refreshes the 8192 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0~A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM4216C/V257 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) befor $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operatian occurs automatically. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

The KM4216C/V257 has 3 type $\overline{CAS}$-before-$\overline{RAS}$ refresh operation ; CBRR, CBRN, CBRS

CBRR (CBR Refresh with option reset) is set if DSF low at the $\overline{RAS}$ falling edge. This mode initiates to change from old masked write to new masked write cycle, and reset stop register to default values.

CBRN (CBR refresh without reset) is set if DSF high when $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$ and simply do only refresh operation.

CRRS(CBR Refresh with stop register set) cycle is set if DSF high when $\overline{WB}/\overline{WE}$ is low and this mode is to set stop register's value.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM4216C/V257 hidden refresh cycle is actually a $\overline{CAS}$-beford-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh *(Only KM4216C/V257F)*: The Self Refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for longer periods of standby, such as a battery back-up. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If $\overline{RAS}$ is low more than 100μs at the condition of CBR, Self Refresh function is accomplished. In this state, the external refresh address do not need to supply additionally on-chip because the refresh counter on-chip gives that addresses needed to refresh. Please note that the ending point of Self Refresh is when $\overline{RAS}$ and $\overline{CAS}$ is high and t_{RPS} of Self Refresh is the time reguiring to complete the last refresh of Self Refresh.

Other Refresh Methods : It is also possible to refresh the KM4216C/V257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

DEVICE OPERATIONS (Continued)

Table 1. Truth Table for Transfer Operation *: Don't care

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bit
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$			
H	L	H	L	*	Read Transfer	RAM→SAM	512 × 16
H	L	H	H	*	Split Read Transfer	RAM→SAM	256 × 16

Transfer Operation

Transfer operation is initiated when $\overline{DT}/\overline{OE}$ is low at the falling edge of $\overline{RAS}$. The state of DSF when $\overline{RAS}$ goes low is used to select between normal transfer and split transfer cycle. Each of the transfer cycle is described in the truth table for transfer operation. (Table 1).

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT}/\overline{OE}$ is low, $\overline{WB}/\overline{WE}$ is high, and DSF is low at the falling edge of $\overline{RAS}$. The row address bits in the read transfer cycle indicate which sixteen 512 bit DRAM row portions are transferred to the sixteen SAM data register portions. The column address bits indicate the start address of the SAM Registers when SAM data read operation is performed. If MSB of column address is low during Read transfer operation, the QSF state will be set low level and this indicates the start address of SAM register is present at lower half of SAM port. (If A8 is high, QSF will be high and means the start address is in upper half). Read Transfer may be accomplished in two ways. If the transfer is to be synchronized with the SC, $\overline{DT}/\overline{OE}$ is taken high after $\overline{CAS}$ goes low. This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT}/\overline{OE}$ must be Synchronized with the rising edge of SC (t_{TSL}/t_{TSD}) to retain the continuity of Sevial read data output. If the transfer does not have to be synchronized with SC, $\overline{DT}/\overline{OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first rising edge of $\overline{DT}/\overline{OE}$.

The Split Read Transfer cycle elinimates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

DEVICE OPERATIONS (Continued)

A normal Read Transfer cycle must be executed before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is initiated by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched in the falling edge of $\overline{RAS}$. The column address defined by (A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. column addrress pin A_8 is a "Don't care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1= Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when the SAM address counter reaches a split SAM boundary (e.g.255th or 511th bit).
Example of SRT applications are shown in Fig.6 through Fig. 9

The normal usage of Split Read Transfer cycle is described in Fig.6. When Read Transfer is executed, data from X_1 row address is fully transferred to the SAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X_2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC. Note that in this case "256+Y_0" Tap address instead of "Y_0" is loaded.
The another example of SRT cycle is described in Fig.7 When Serial Read is performed after executing RT and SRT in succession, the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 8 and 10 are the exanple of abnormal SRT cycle.

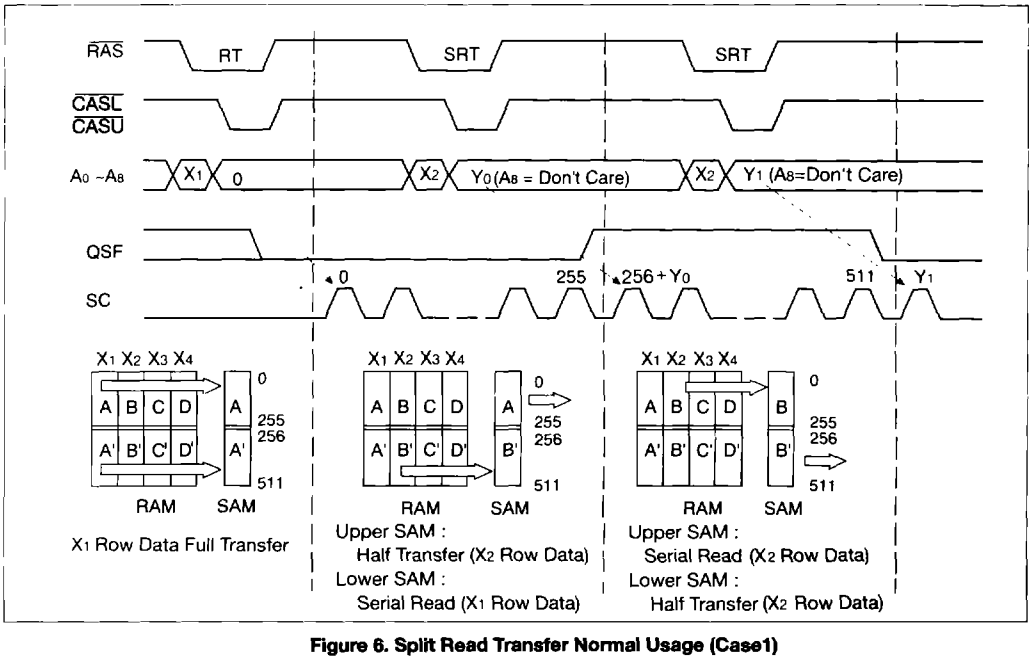


Figure 6. Split Read Transfer Normal Usage (Case1)

DEVICE OPERATIONS (Continued)

If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig.8, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig. 9 indicates that SRT cycle is not performed until Serial Read is completed to the boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during t_{STH}+ t_{STS}(See Figure 10)

A split Read Transfer does not change the direction of the SAM I/O port.

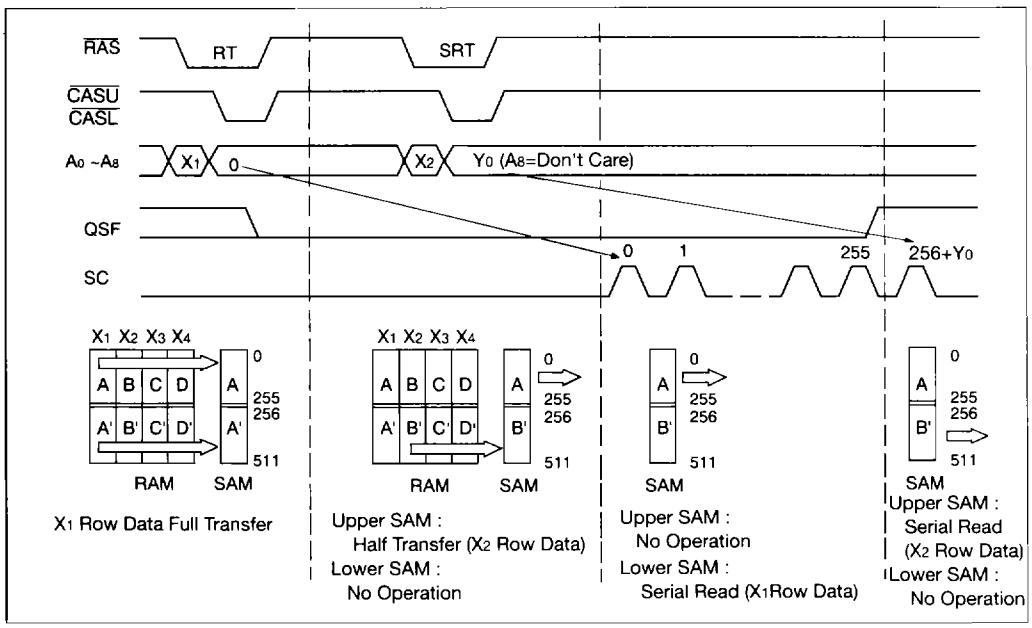


Figure 7. Split Read Transfer Normal Usage (Case 2)

DEVICE OPERATIONS (Continued)

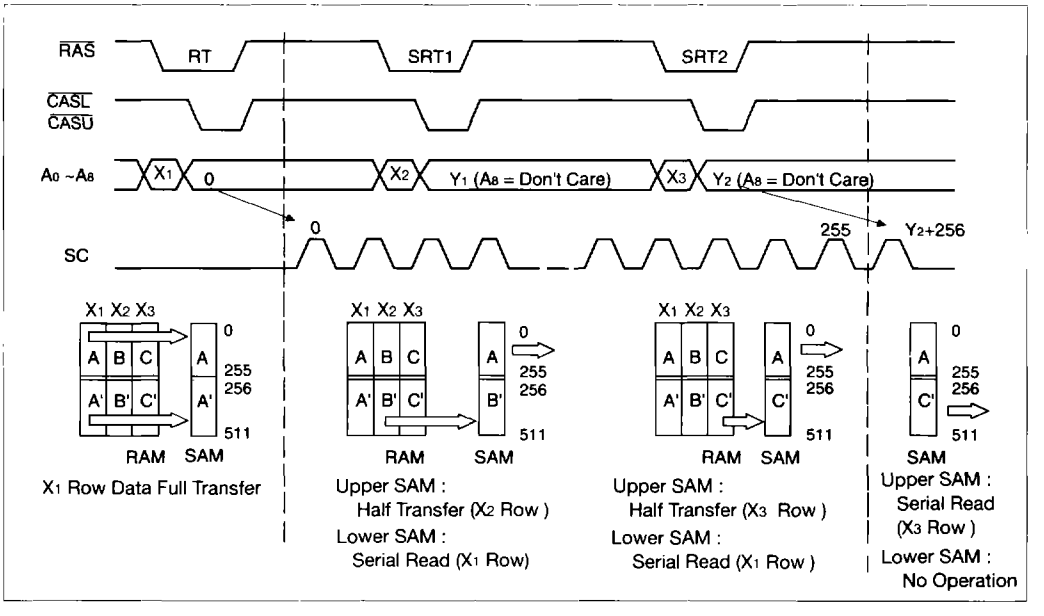


Figure 8. Split Read Transfer Abnormal Usage (Case 1)

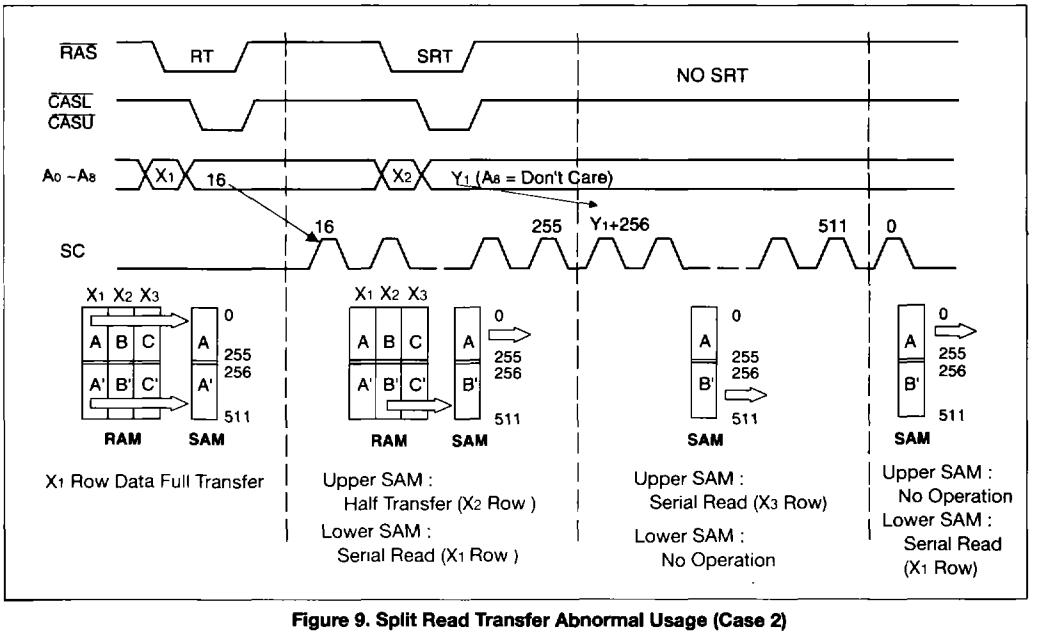


Figure 9. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATIONS (Continued)

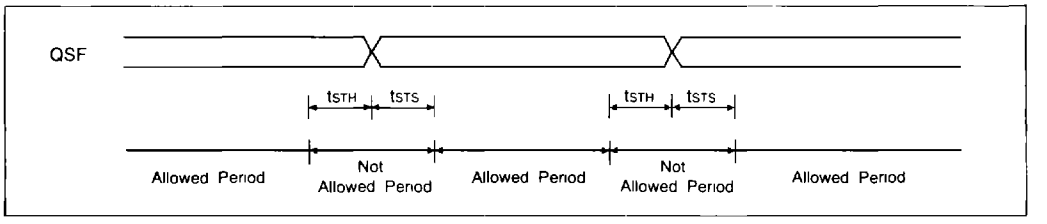


Figure 10. Split Transfer Cycle Limitation Period

Programmable Split SAM

In split SAM mode, SAM is divided into the lower half and the upper half.

After the last address of each half SAM(255 or 511) is accessed, the access will be changed one half of the SAM to the other half (at the loaded TAP address).

This last address is called Stop Point.

The KM4216C/V257 offers user-programmable Stop Point. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points and size of the resulting partitions are shown in Table 2. The Stop Points are set by performing CBRS cycle. The CBRS cycle's condition is $\overline{WB}/\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$ in CBR cycle and the Stop Point is determined by row address entering at this time.

The Stop Point will not become valid until a SRT cycle is done. The Stop Point do not effect to SAM in normal RT, RRT cycle.

In Figure 11. programmable split SAM operation is shown. If a SRT cycle was done before the partition boundary (383), the access will jump to the TAP address(70) of the next half. Otherwise, the axxess will continue in the same half until a SRT occurs or the SAM half boundary (255, 511).

Note that the Stop Point may be changed at any time by performing another CBRS, and new Stop Point will not be valid until a SRT is performed. To reset Stop Point, CBRR cycle must be performed. DBRR is a CBR cycle with DSF low at the falling edge of $\overline{RAS}$. The CBRR wil take effect immediately; it does not require a SRT to become active valid.

Table 2. Stop Point Setting Address

Stop Register= Store Address of Serial Access
Use on the Split Transter Cycle
Stop Pointer Set → CBRS Cycle

Number of Stop Points/Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	A_3-A_0
1	(1×256)×2	x	1	1	1	1	x
2	(2×128)×2	x	0	1	1	1	x
4	(4×64)×2	x	0	0	1	1	x
8	(8×32)×2	x	0	0	0	1	x
16	(16×16)×2	x	0	0	0	0	x

*Other Case=Inhibit
X=Don't Care

DEVICE OPERATION (continued)

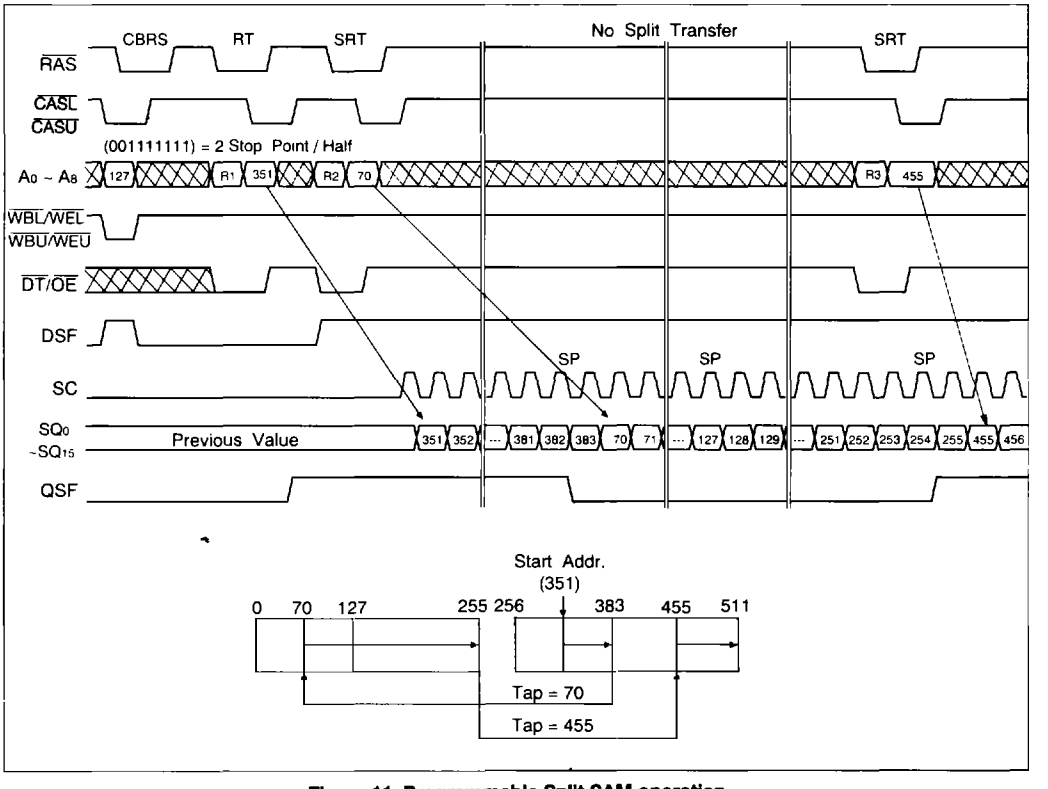
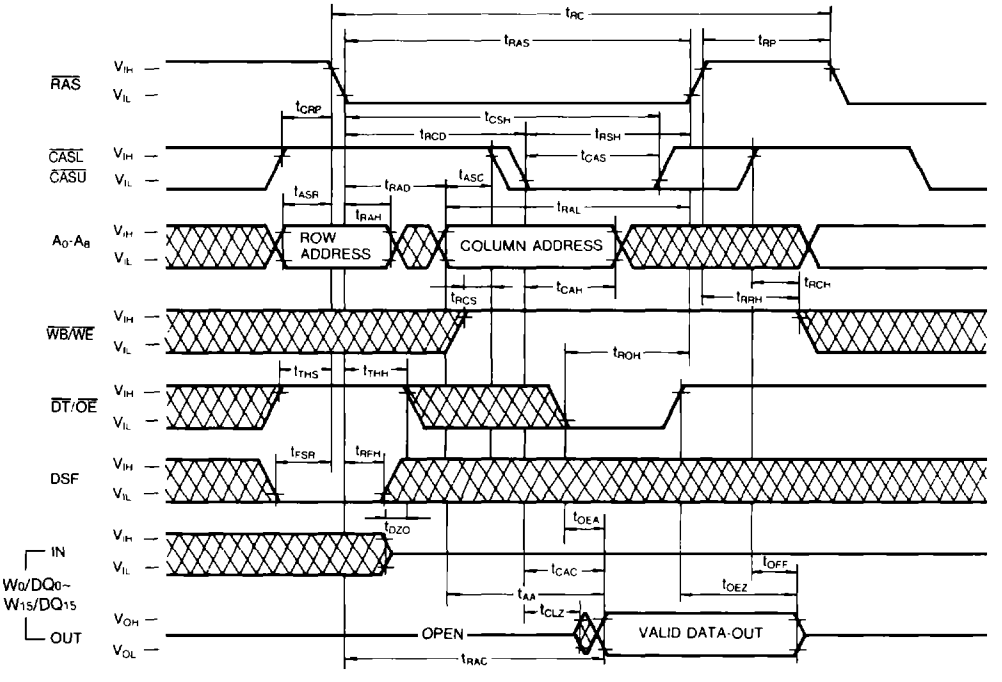


Figure 11. Programmable Split SAM operation

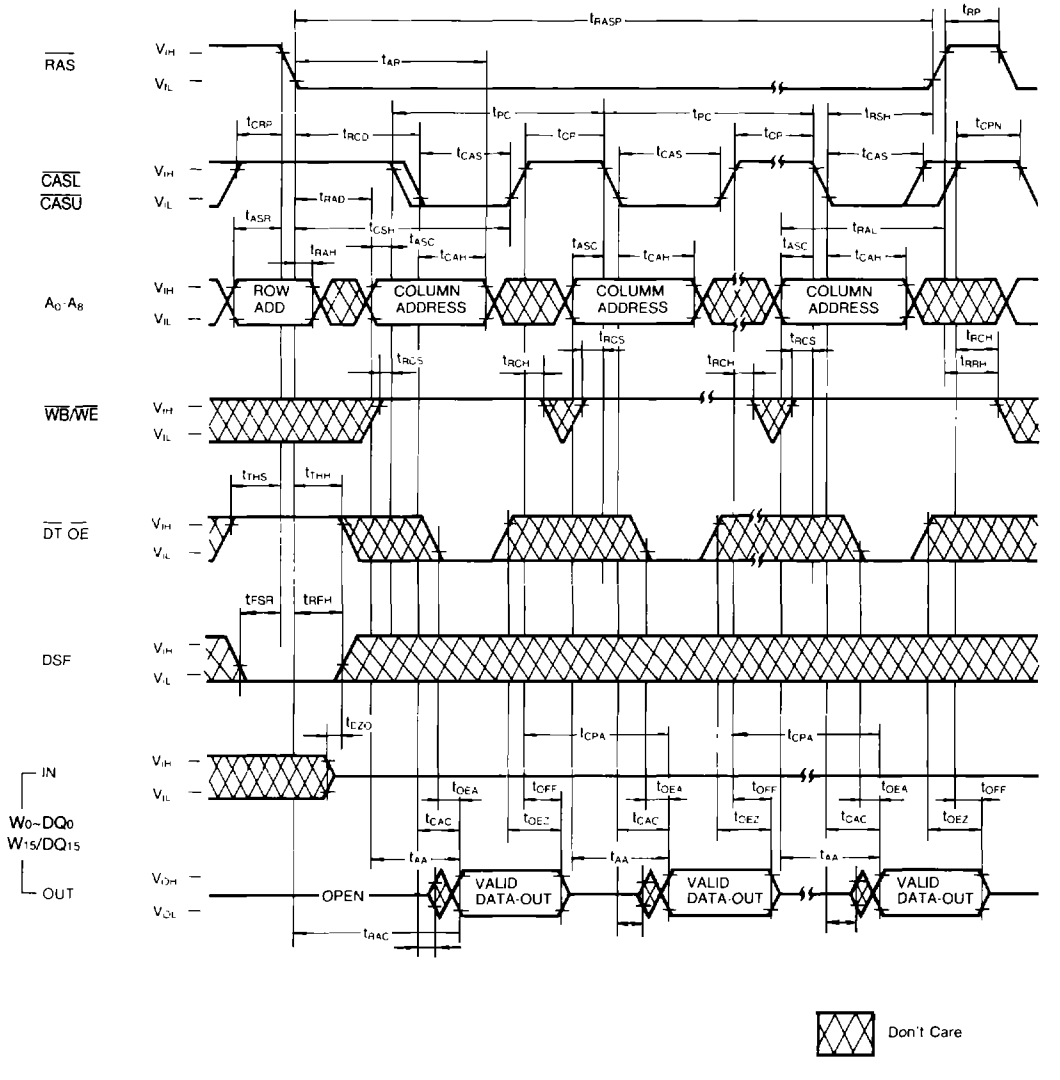
TIMING DIAGRAMS

READ CYCLE



Don't Care

FAST PAGE MODE READ CYCLE



Truth Table for Write Cycle(1)

FUNCTION	RAS			CAS	CAS↓ or WBL(U)/WEL(U)
	*1 WB/WE	*2 DSF	*3 Wi/DQi (3) (New Mask)	*4 DSF	*5 Wi/DQi
Normal write	1	0	×	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask) (4)	1	0	×	1	Column Mask
Masked Block Write (4)	0	0	Write Mask	1	Column Mask
Load Mask Data Register (2)	1	1	×	0	Write Mask Data
Load Color Register	1	1	×	1	Color Data

Note:
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram on the following pages
(2) Old Mask data load
(3) Function table for Old Mask and New Mask

IF		*1 WB/WE	*3 Wi/DQi	Note
LMR Cycle Executed	Yes	0	×	Write using mask register data (Old Mask Data)
		1	×	Non Masked Write
	No	0	Mask	Write using New Mask Data Wi/DQi=0 Write Disable Wi/DQi=1 Write Enable
		1	×	Non Masked Write

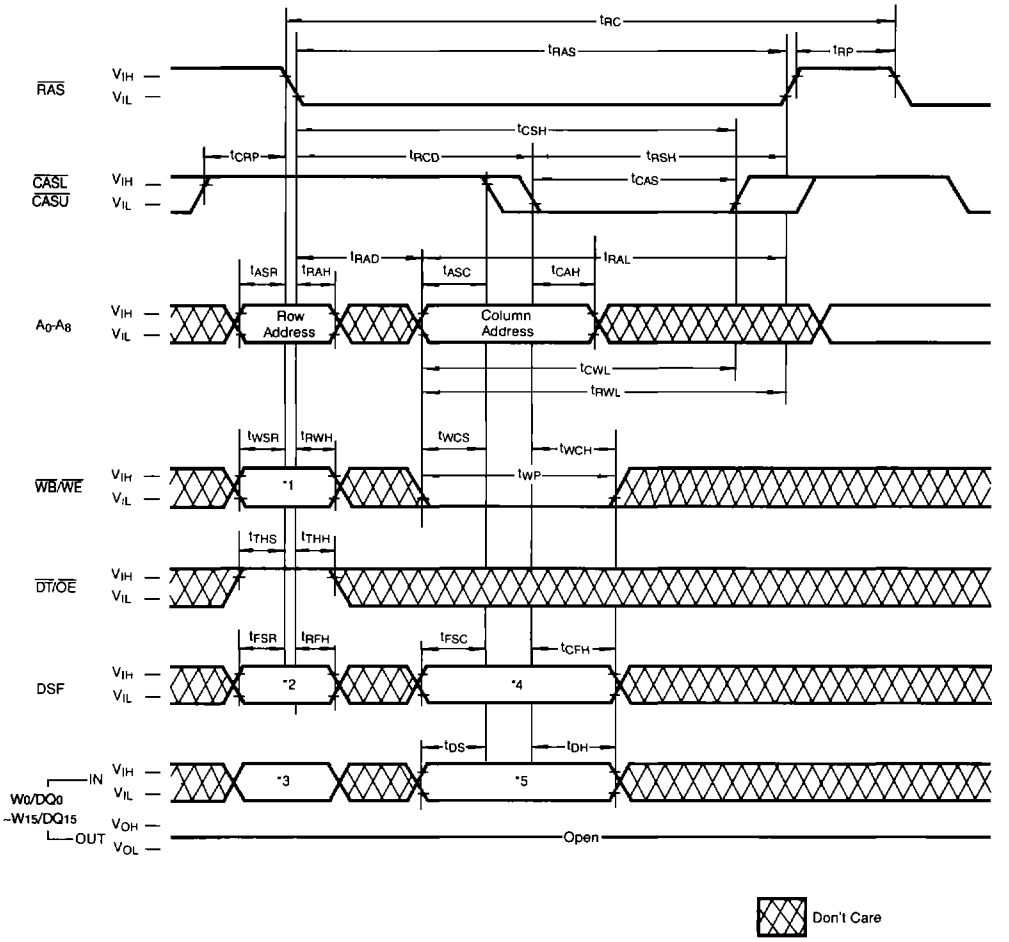
× : Don't Care

(4) Function Table for Block Write Column Mask

Column Address		
A2	A1	A0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

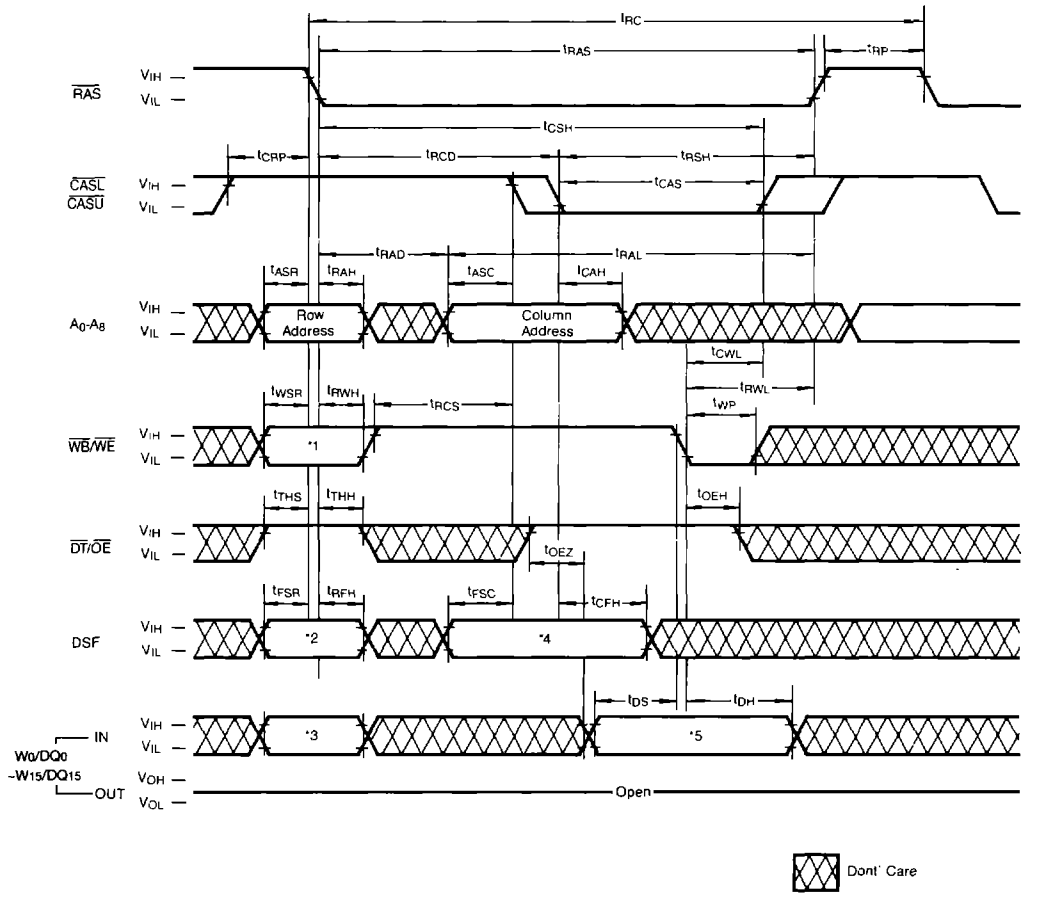
*5		IF	
Lower Byte	Upper Byte	Wi/DQi=0	Wi/DQi=1
W_0/DQ_0	W_8/DQ_8	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
W_1/DQ_1	W_9/DQ_9		
W_2/DQ_2	W_{10}/DQ_{10}		
W_3/DQ_3	W_{11}/DQ_{11}		
W_4/DQ_4	W_{12}/DQ_{12}		
W_5/DQ_5	W_{13}/DQ_{13}		
W_6/DQ_6	W_{14}/DQ_{14}		
W_7/DQ_7	W_{15}/DQ_{15}		

EARLY WRITE CYCLE



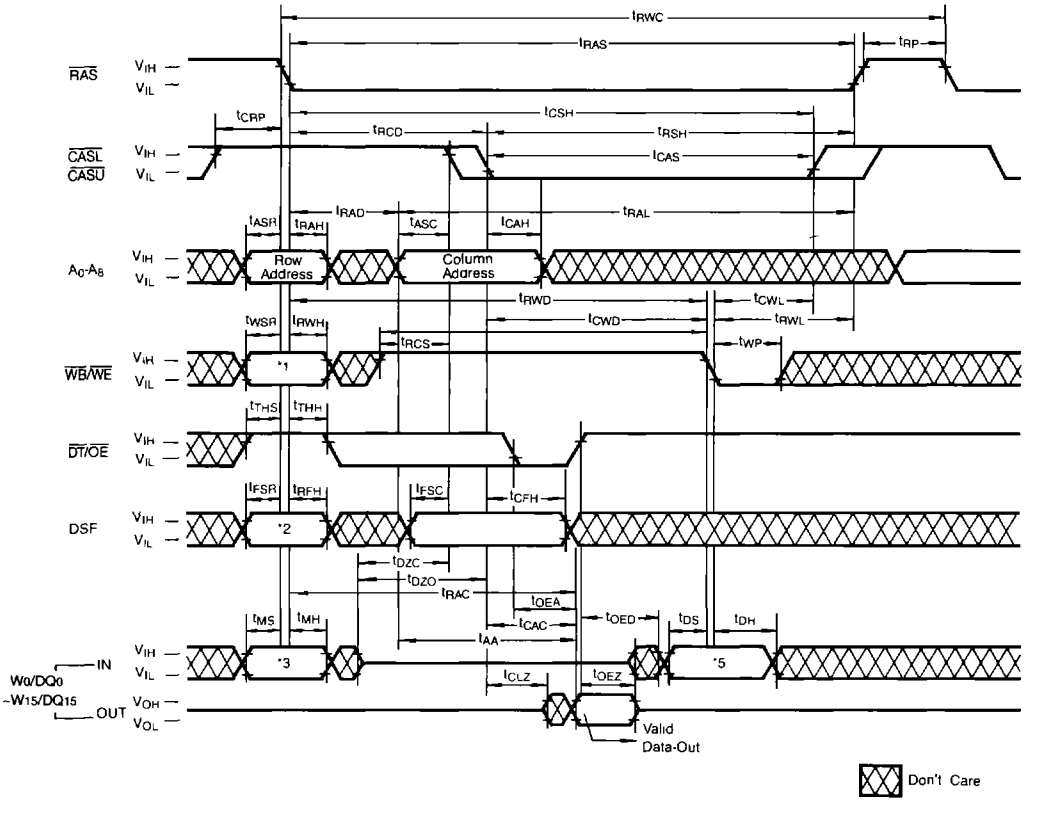
Note : In Block write cycle, only column address A3~A8 are used.

LATE WRITE CYCLE



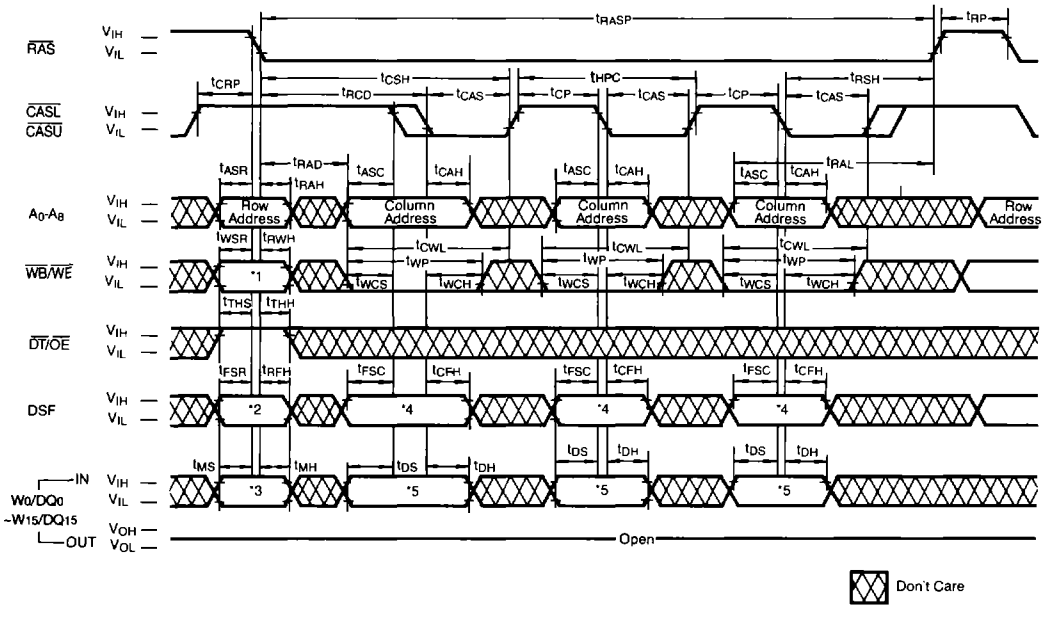
Note : In Block write cycle, only column address A_3~A_8 are used.

READ-WRITE/READ-MODIFY-WRITE CYCLE



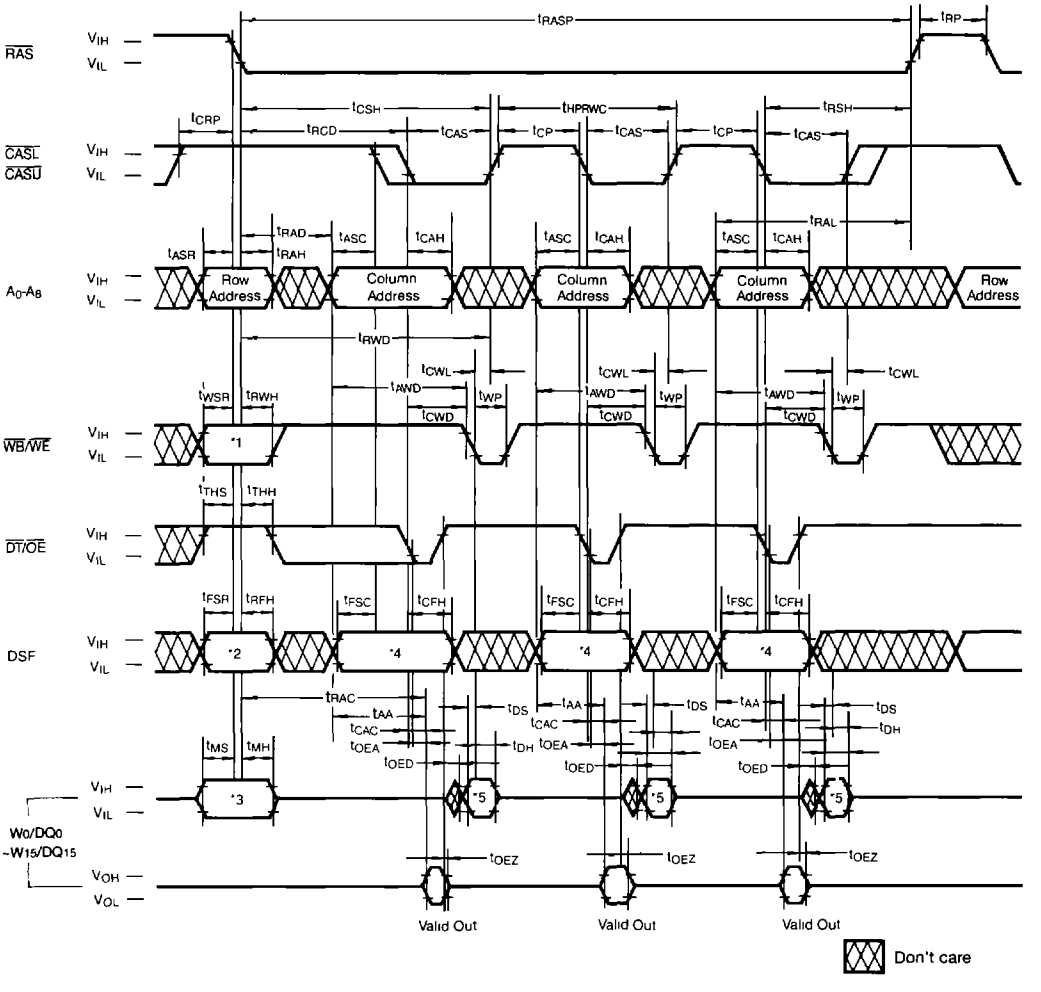
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE EARLY WRITE CYCLE



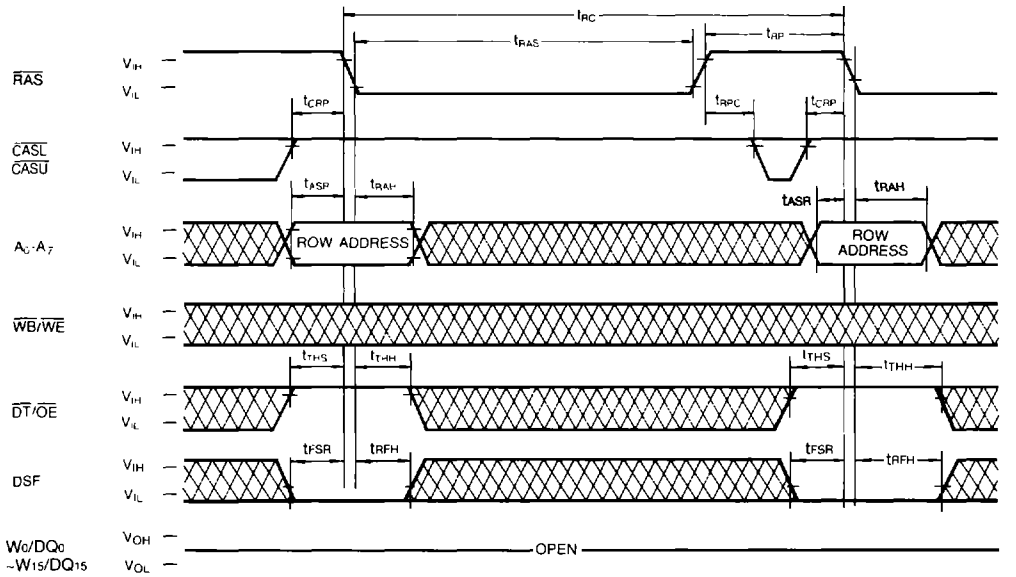
Note : In Block write cycle, only column address A_3~A_8 are used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



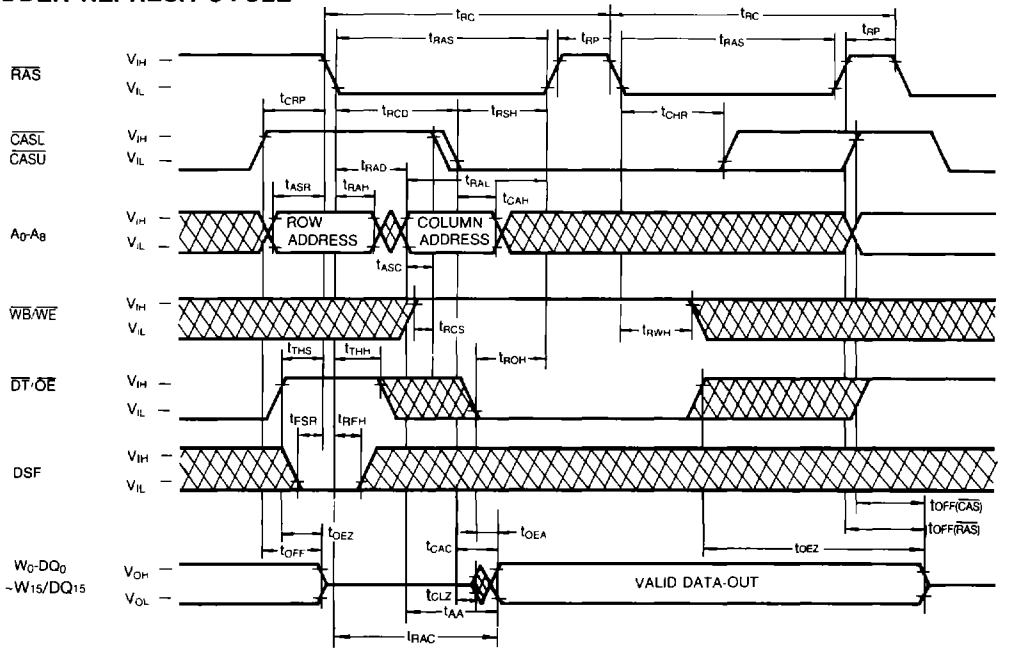
Note : In Block write cycle, only column address A_3~A_8 are used.

$\overline{RAS}$ ONLY REFRESH CYCLE

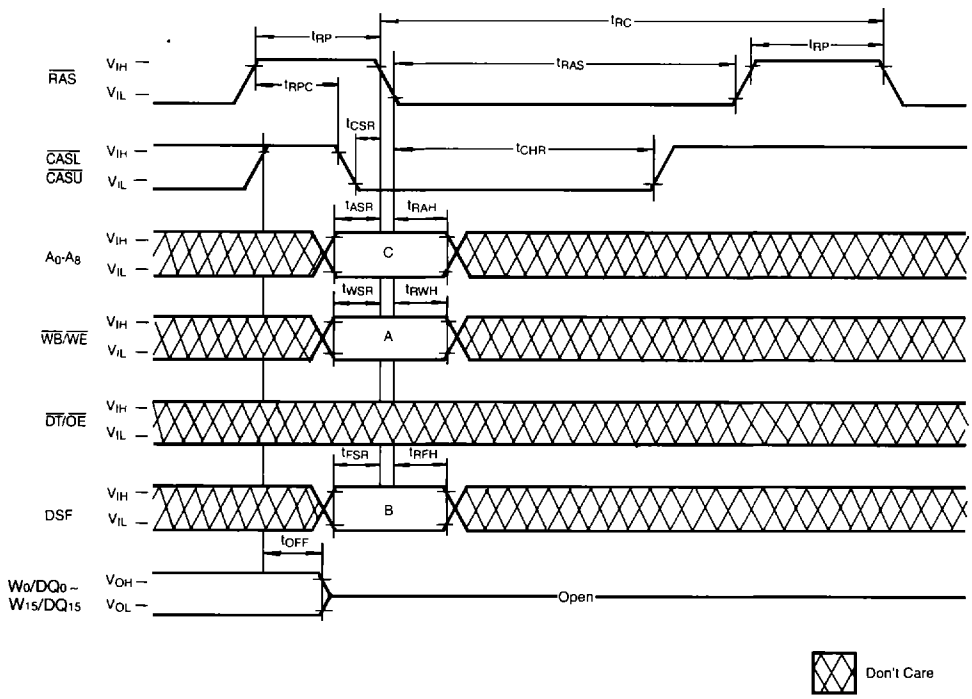


DON T CARE

HIDDEN REFRESH CYCLE



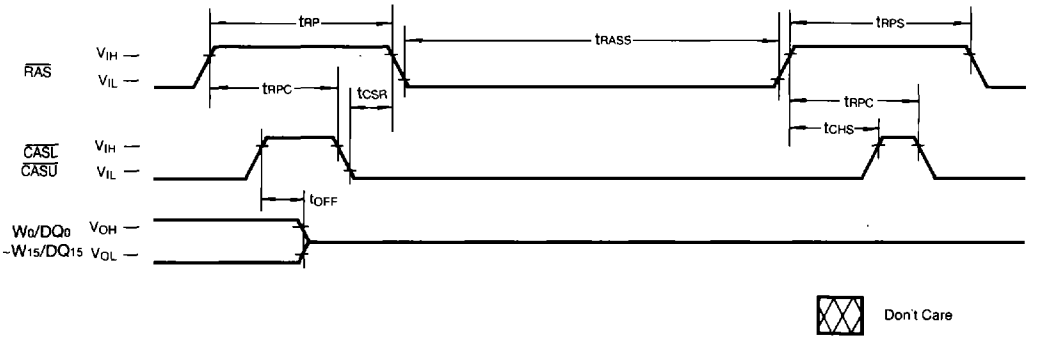
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE FUNCTION TABLE

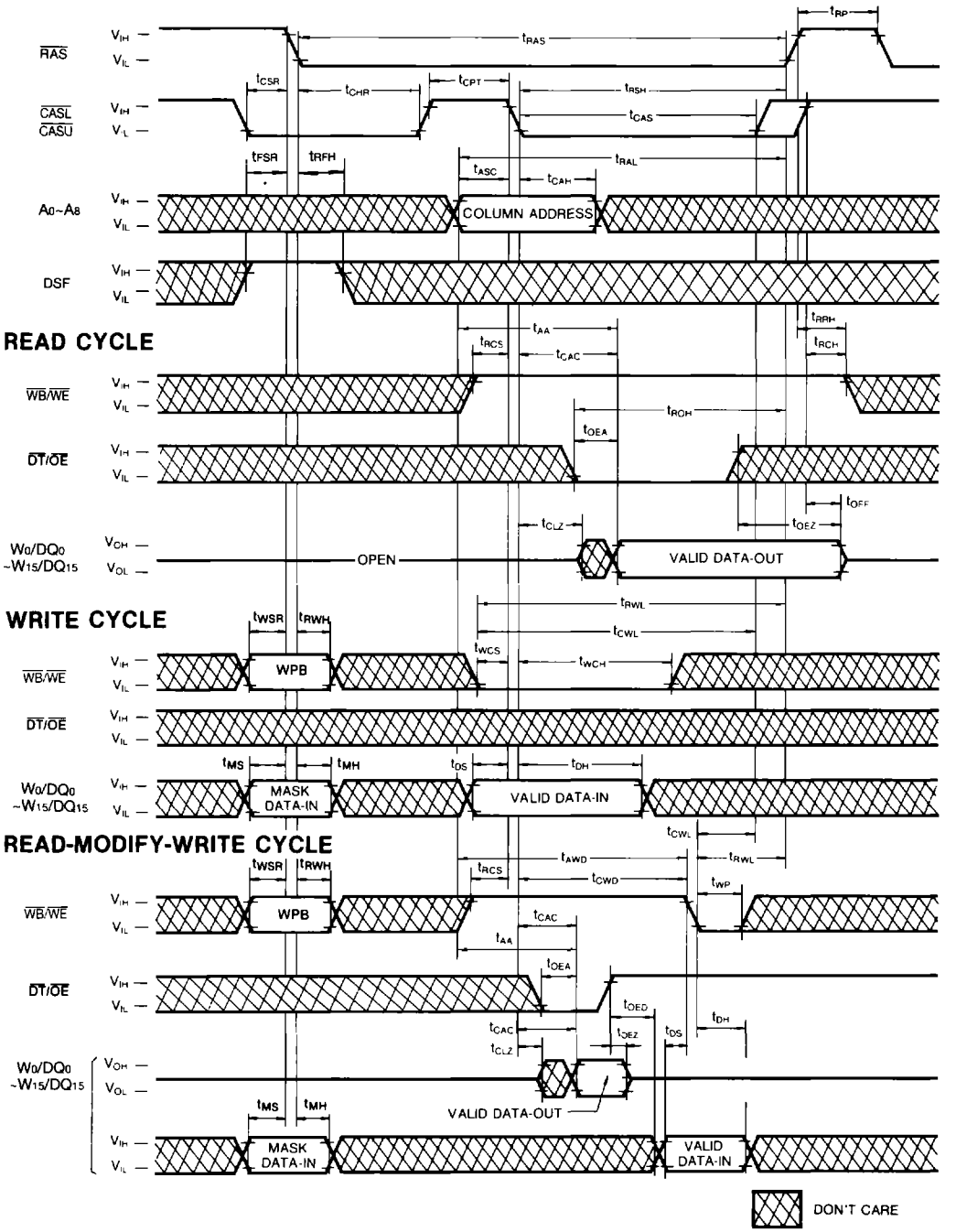
FUNCTION	CODE	LOGIC STATES		
		A	B	C
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (Stop Register Set)	CBRS	0	1	STOP Address
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (No Reset)	CBRN	1	1	X

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

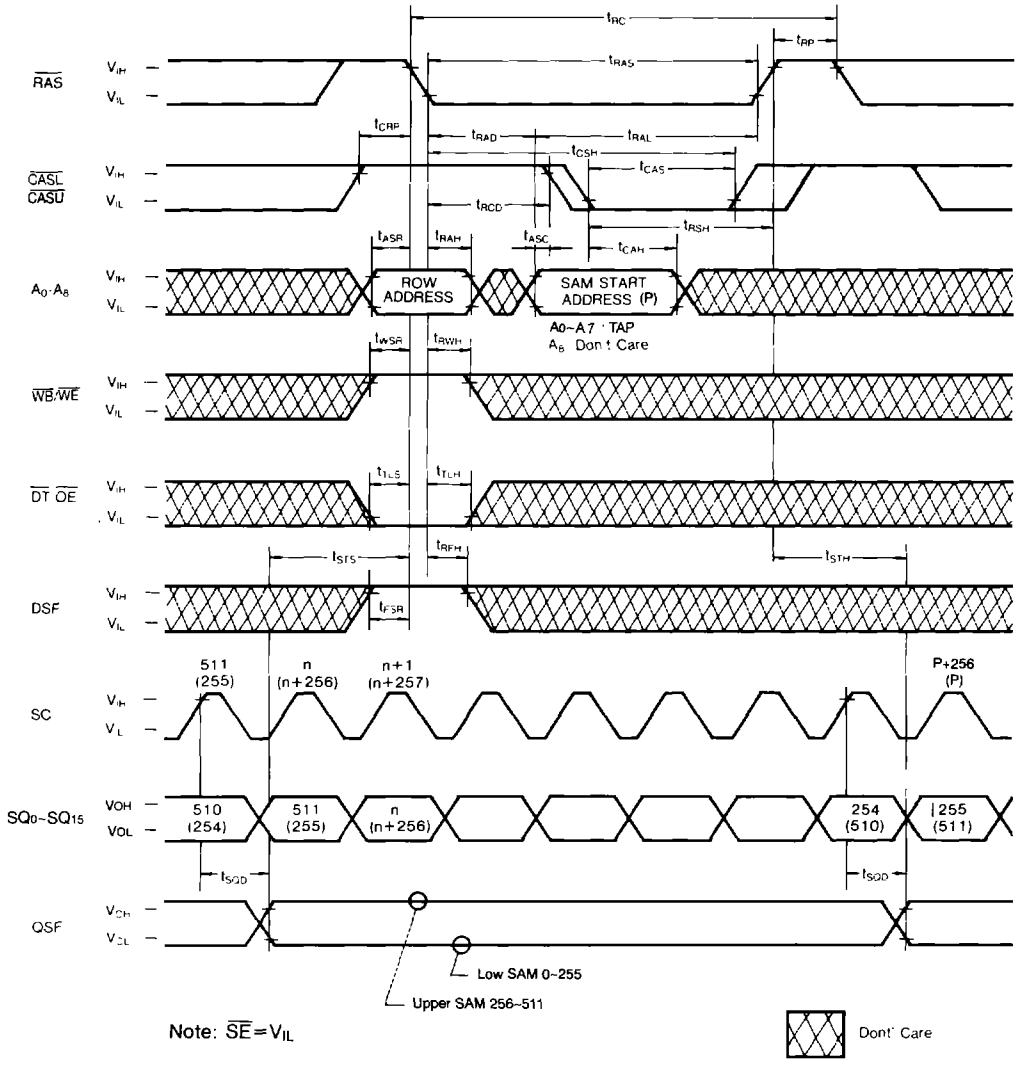


*CBR SELF REFRESH CYCLE IS APPLICABLE WITH CBRR, CBRS, OR CBRN CYCLE

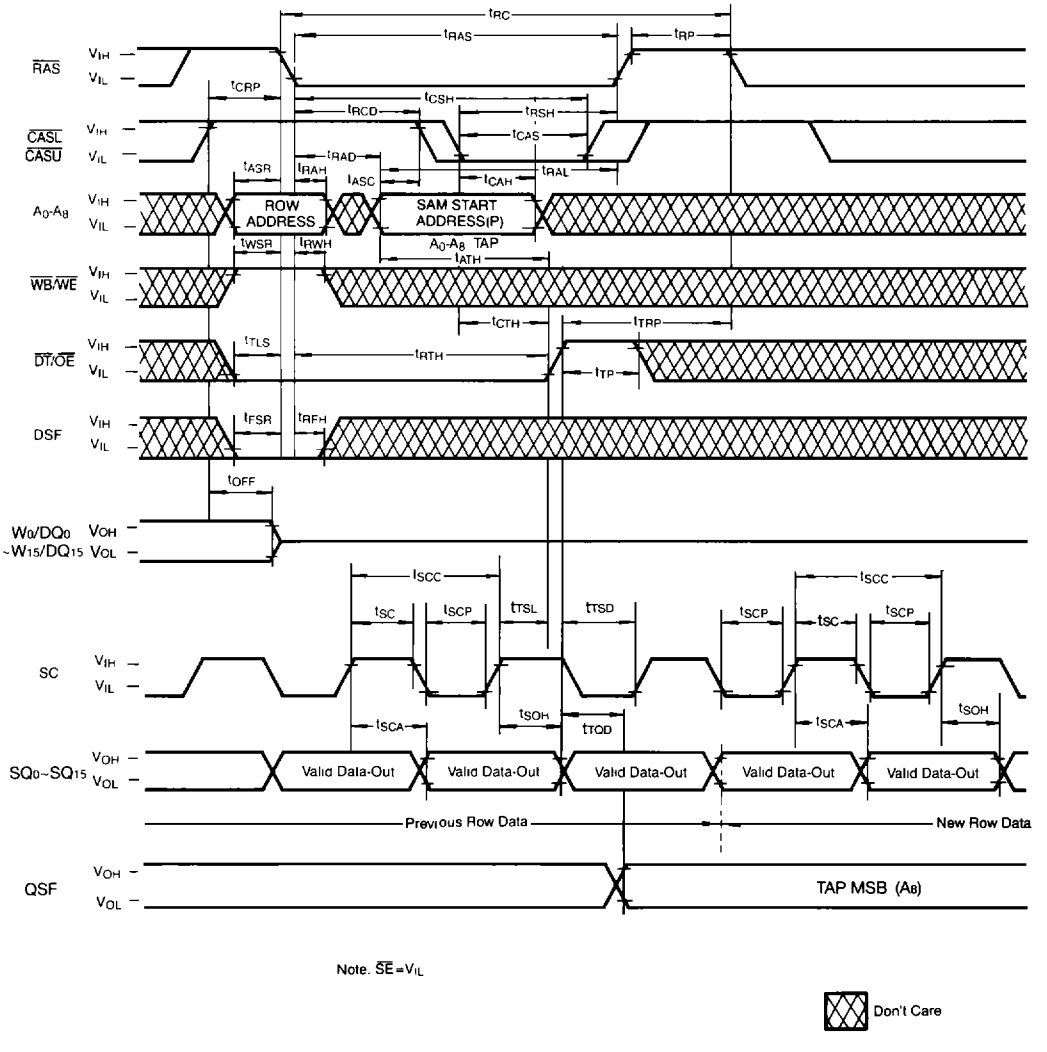
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SPLIT READ TRANSFER CYCLE



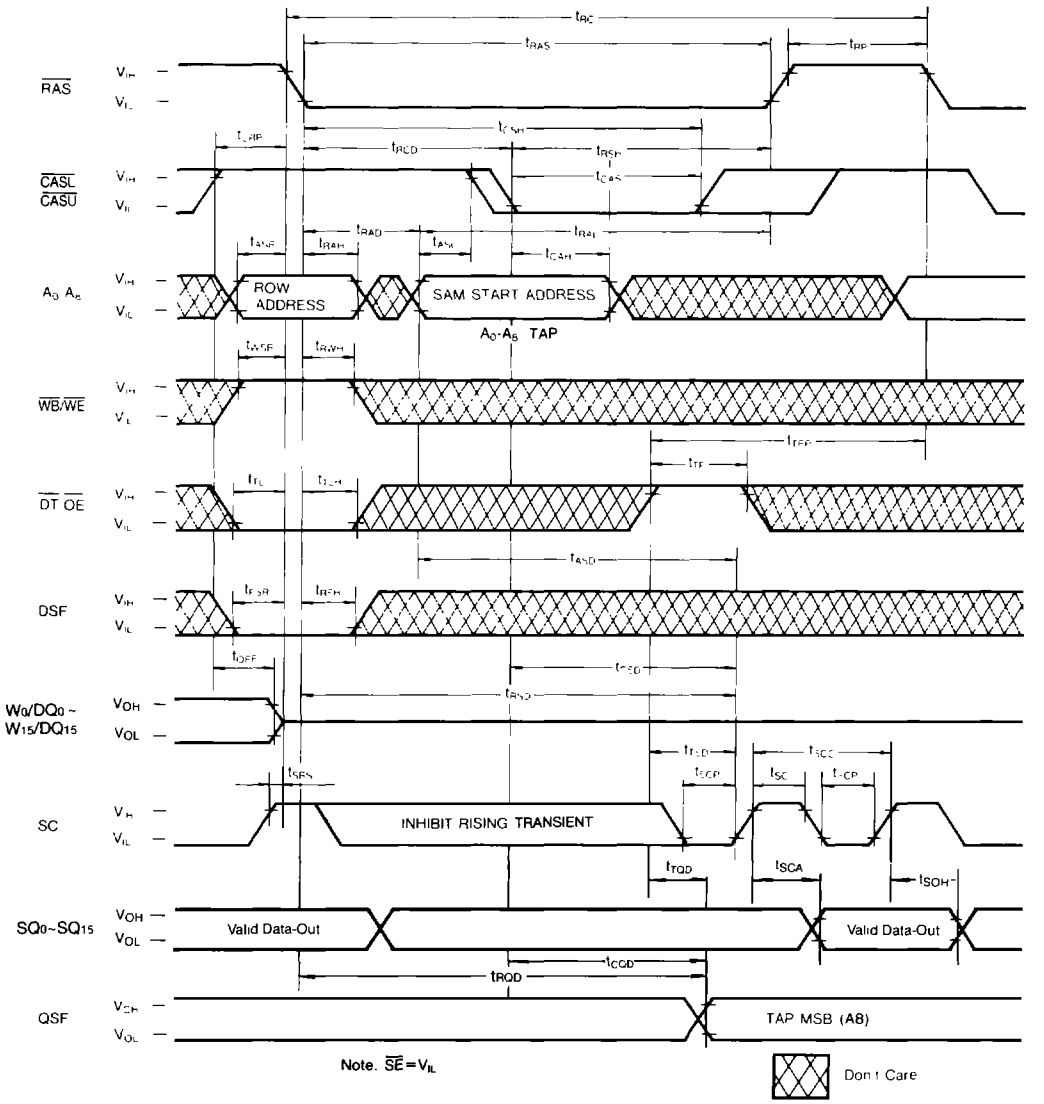
REAL TIME READ TRANSFER CYCLE



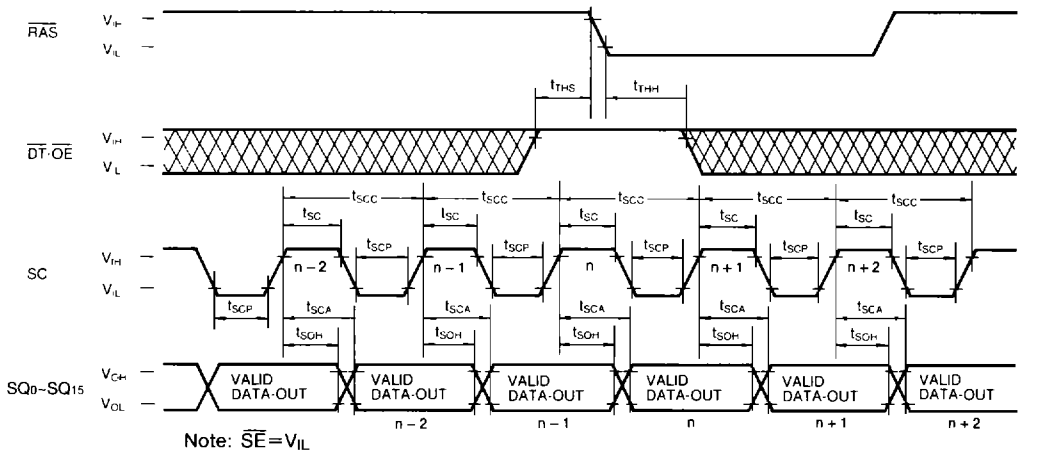
Note. $\overline{SE}$=V_{IL}

Don't Care

READ TRANSFER CYCLE

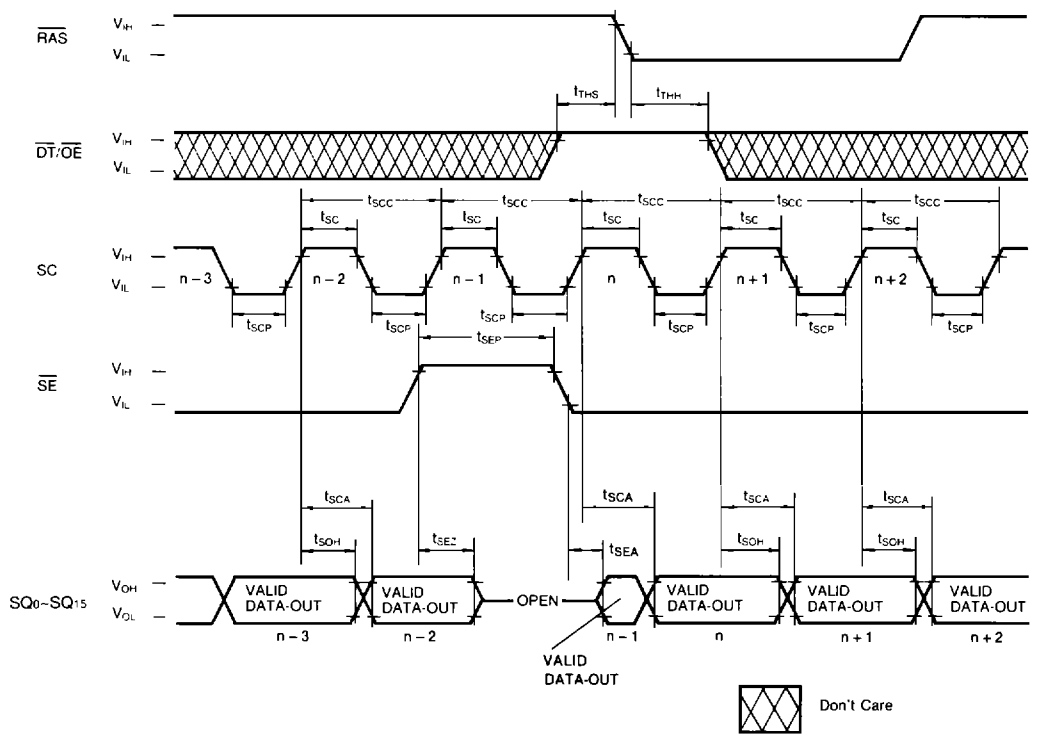


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$=V_{IL}

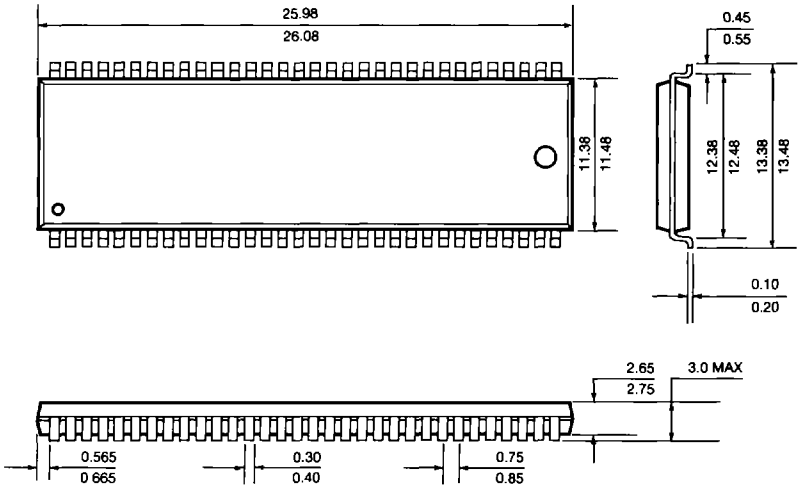
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



PACKAGE DIMENSIONS

Units: Millimeters

64 Pin Plastic Shrink Small Out Line Package



70(64) Pin Plastic Thin Small Out Line Package (Type II Forward)