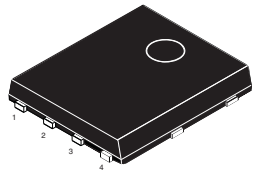
STL12P6F6

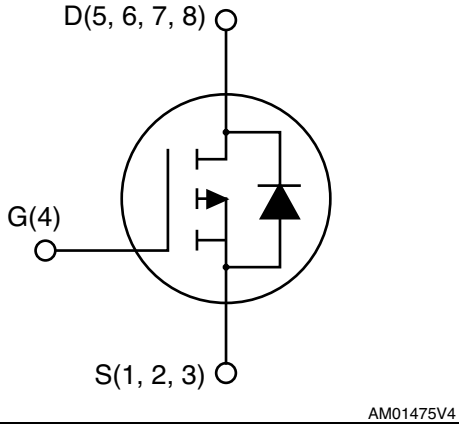
P-channel 60 V, 0.13 Ω typ., 3 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



PowerFLAT™ 5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)max}$	I_D
STL12P6F6	60 V	0.16 Ω @ 10 V	3 A

- $R_{DS(on)}$ * Qg industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL12P6F6	12P6F6	PowerFLAT 5x6	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	4	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	12	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	7	A
I_{DM} (2)(3)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25 °C	75	W
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	4.8	W
T_j P_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. The value is according to $R_{thj\text{-}case}$
2. The value is according to $R_{thj\text{-}pcb}$
3. Pulse width is limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	31.3	°C/W

1. When mounted on FR-4 board of 15 mm^2, 2 Oz Cu, t<10 sec

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 60 V V_{DS} = 60 V, T_C=125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.5 A		0.13	0.16	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 48 V, f = 1 MHz, V_{GS} = 0	-	340	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	20	-	pF
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 3 A, V_{GS} = 10 V (see *Figure 3*)	-	6.4	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	1.7	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 48 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2*)	-	6.4	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	14	-	ns
t_f	Fall time		-	3.7	-	ns

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		3 12	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 16 V, T_j = 150 °C (see *Figure 4*)	-	20		ns
Q_{rr}	Reverse recovery charge		-	17.8		nC
I_{RRM}	Reverse recovery current		-	1.8		A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 µs, duty cycle 1.5%

Note: For the P-channel Power MOSFET actual polarity of voltages and current has to be reversed.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

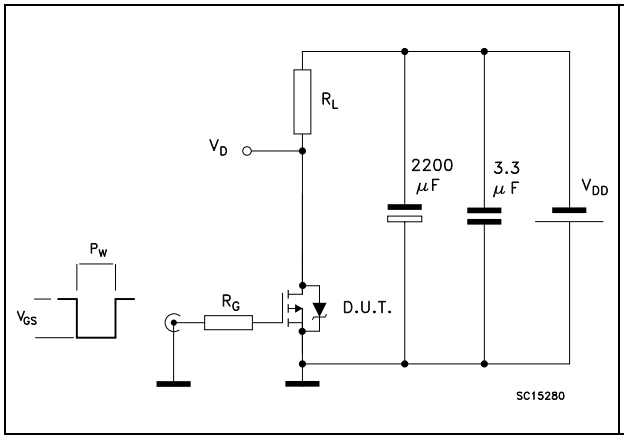


Figure 3. Gate charge test circuit

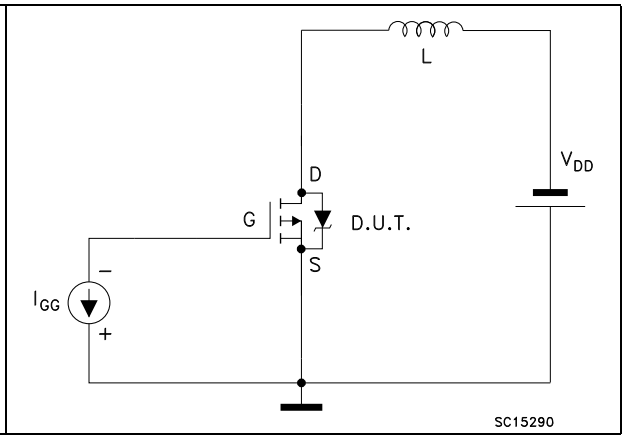
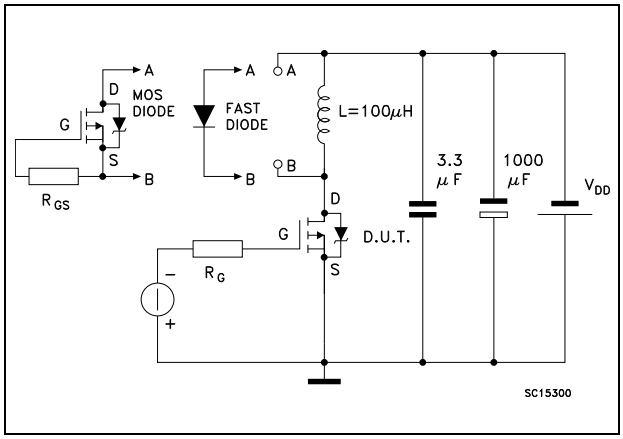


Figure 4. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 5. PowerFLAT™ 5x6 type S-R drawing

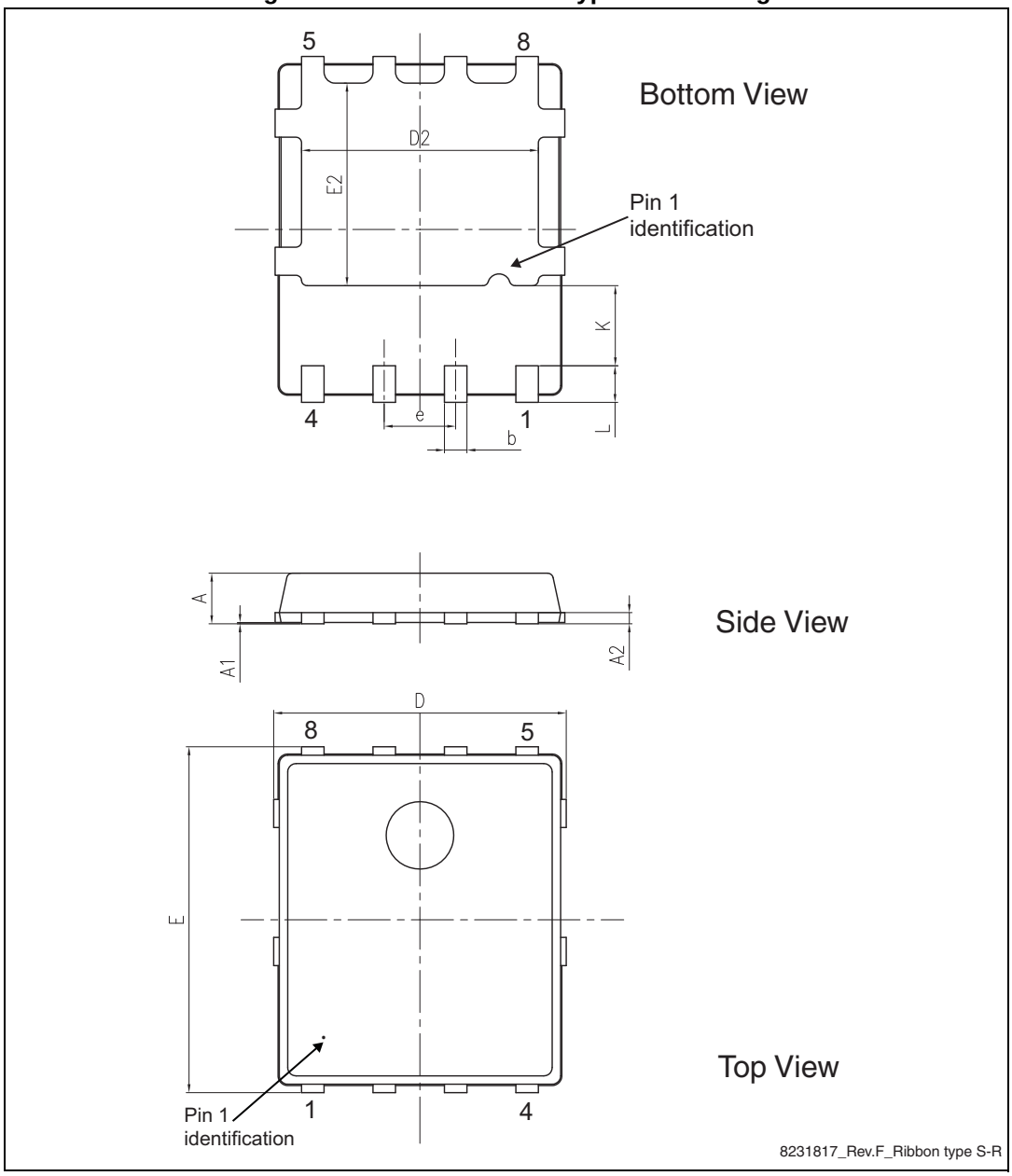
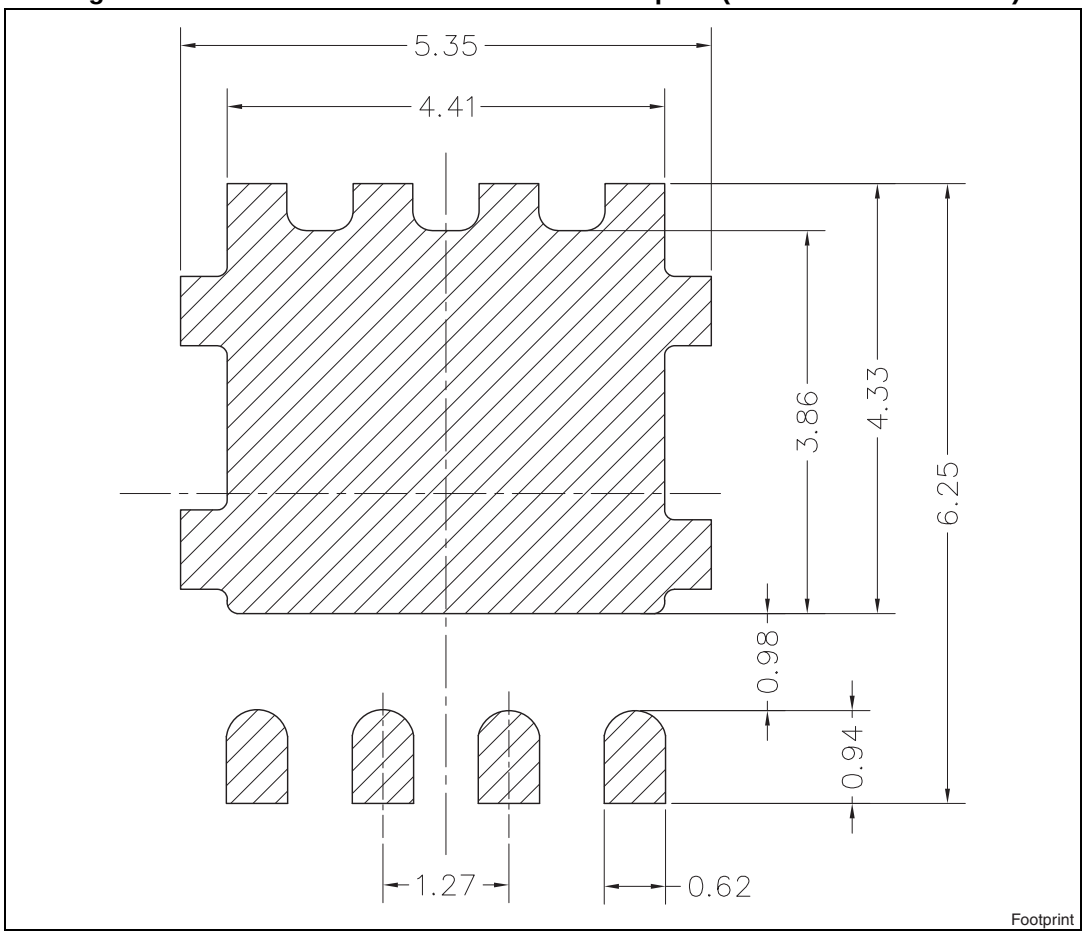


Figure 6. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 7. PowerFLAT™ 5x6 tape[(a)]

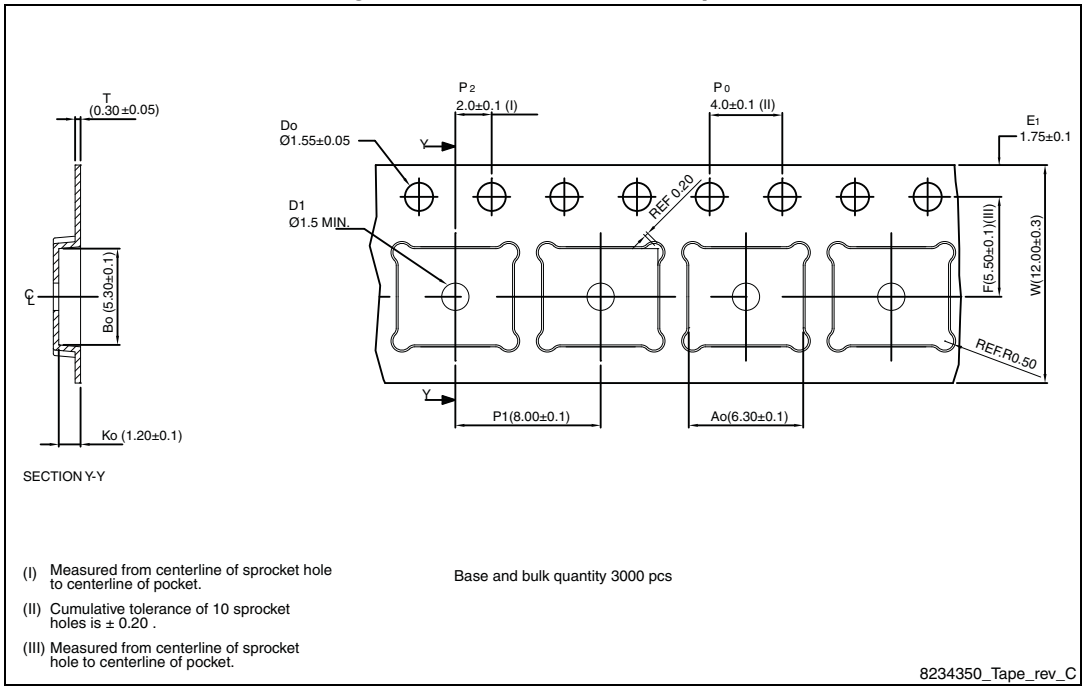
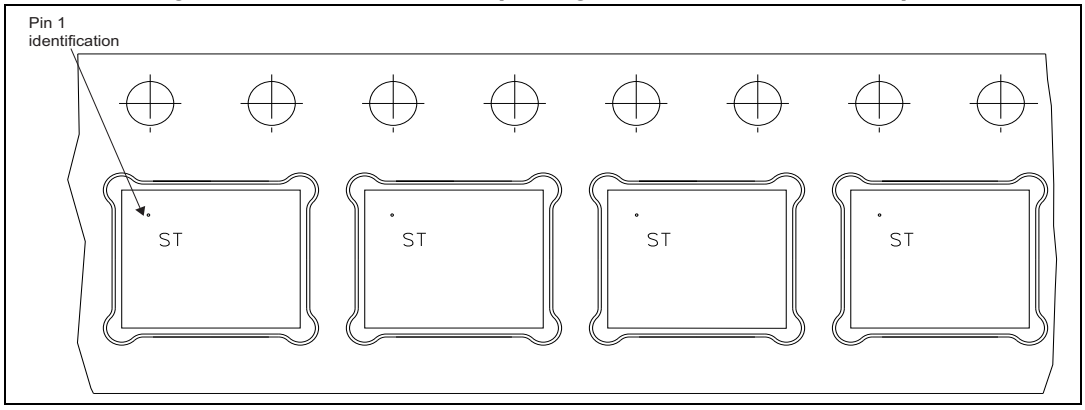
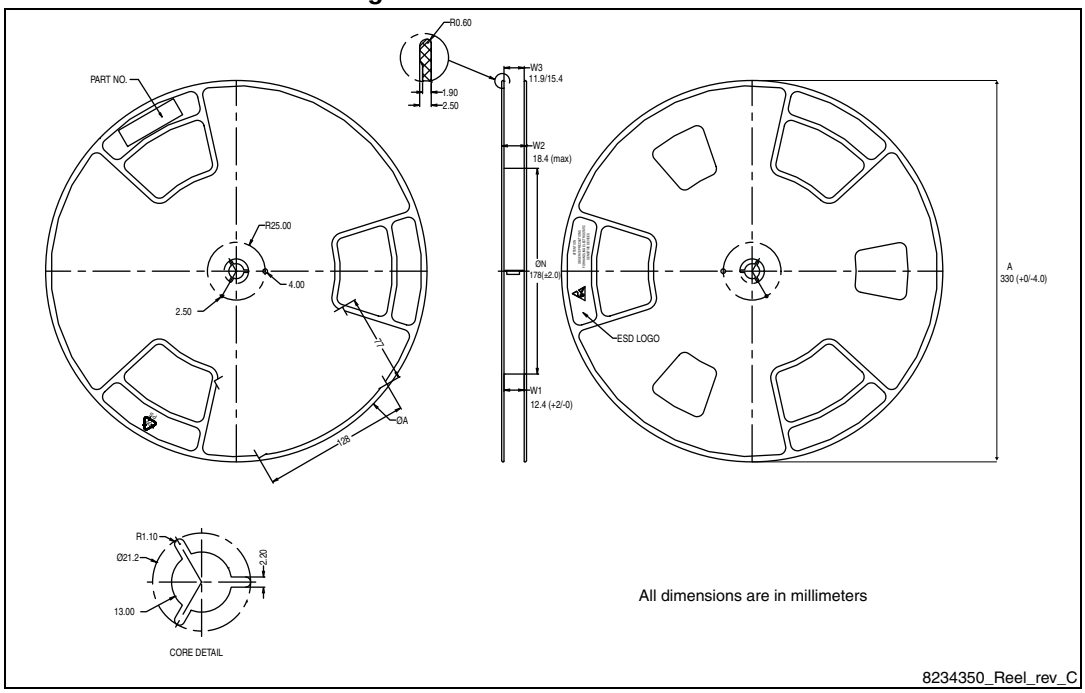


Figure 8. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 9. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Mar-2013	1	First release.