8KX16/4KX16X2-Way Cache Data Static RAM

FEATURES

- **Configurable for 2-Way or Direct Mapped Cache Organizations**
  - **—2-way: 4,096 words x 16 bits**
  - **—Direct: 8,192 words x 16 bits**
- **On-Chip Address Latches for A0-A11**
- **Direct interface to intel 32385 Cache Controller**
- **Single 5V±10% Power Supply**
- **Two Chip Selects**
- **Two Output Enables**
- **Two Write Enables**
- **TTL-Level Three-State Output**
- **52-PIN PLCC Package**

FAST ACCESS TIMES

Parameter	Symbol	-20	-25	-35	Unit
Cycle Time	t_{RC}	20	25	35	ns
Address Access Time	t_{AA}	20	25	35	ns
Output Enable Access Time	t_{OE}	8	10	12	ns

DESCRIPTION

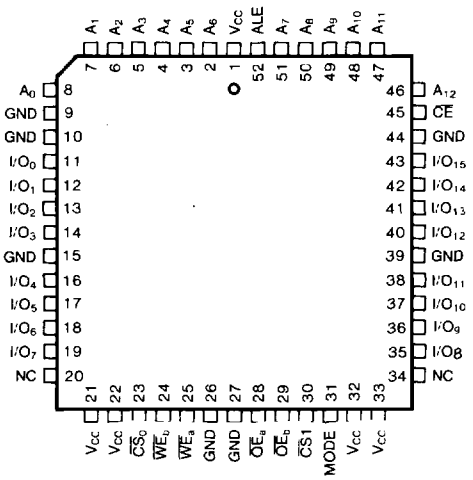
The KM78C80 is a 131,072 bit high speed TTL-Level Static Random Access Memory which can be configured as a 2-way 4K word by 16 bit or direct mapped 8K word by 16 bit Cache Data Ram.

The KM78C80 has internal address latches to increase system performance and reduce chip count. It also has two output enable inputs for precise control of data outputs, and two chip select and write enable inputs for design flexibility. The KM78C80 can directly interface with the intel 82385 or equivelent cache controller without requiring additional components such as latches, tranceivers and gates. It is packaged in a standard 52-pin PLCC for high density board assembly. Therefore, significant reductions in component count, real estate consumption and power dissipation can be acheived with this device.

The mode input allows the user to configure the memory internally as a 2-way 4K word by 16 bit organization suitable for 2-way set associative cache designs, or as an 8K word by 16 bit organization suitable for direct mapped cache designs.

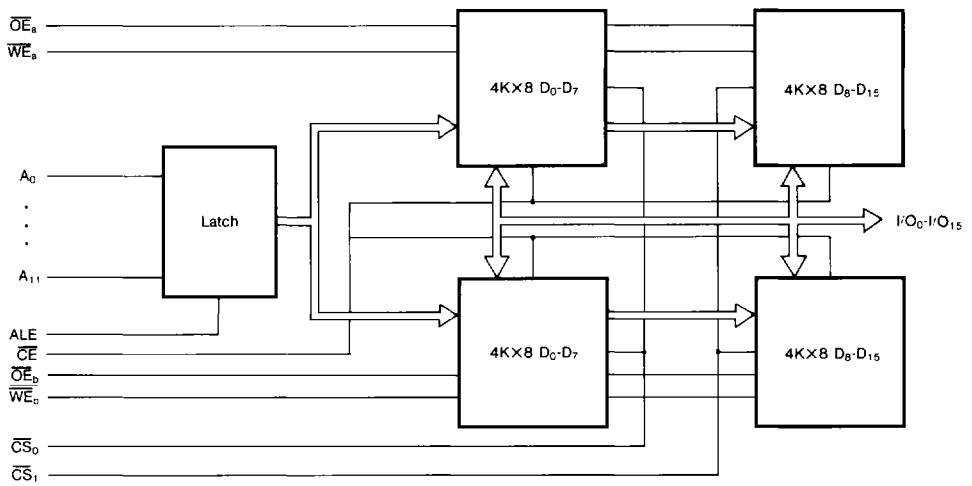
The KM78C80 can also be operated as a conventional asynchronous static RAM which can be accessed from a change of address, simply by keeping ALE at a high logic level.

PIN CONFIGURATION

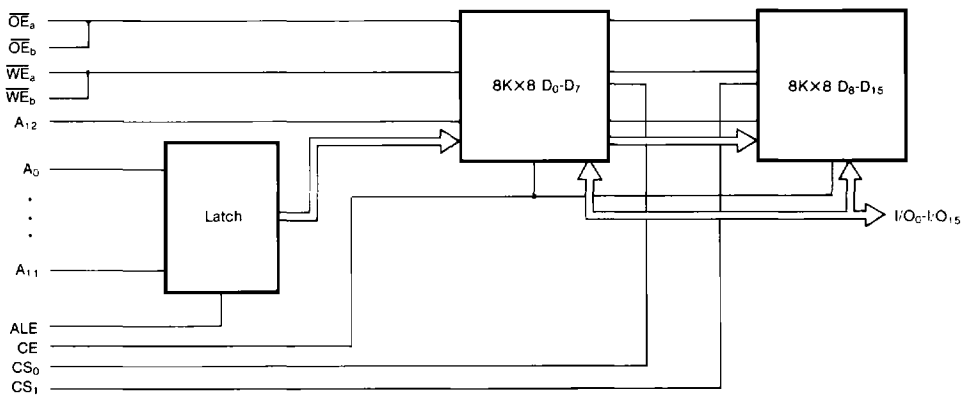


Pin Name	Pin Function
A_0-A_{12}	Address Inputs
ALE	Address Latch Enable
$\overline{WE}_a$, $\overline{WE}_b$	Write Enable
$\overline{CS}_0$, $\overline{CS}_1$	Chip Select
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable
$\overline{CE}$	Chip Enable
MODE	Mode Select
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection

LOGIC BLOCK DIAGRAMS



TWO WAY SET ASSOCIATIVE (MODE = HIGH)



DIRECT MAPPED (MODE = LOW)

FUNCTIONAL DESCRIPTION

TWO-WAY MODE (MODE = HIGH)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{OE_a}$	$\overline{OE_b}$	$\overline{WE_a}$	$\overline{WE_b}$	Operation	
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled	
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs High-Z	
X	X	X	L	L	X	X	Outputs High-Z	
L	L	H	L	H	H	H	Read I/O_0-I/O_7	Way-A
L	L	H	H	L	H	H	Read I/O_0-I/O_7	Way-B
L	H	L	L	H	H	H	Read I/O_8-I/O_{15}	Way-A
L	H	L	H	L	H	H	Read I/O_8-I/O_{15}	Way-B
L	L	L	L	H	H	H	Read I/O_0-I/O_{15}	Way-A
L	L	L	H	L	H	H	Read I/O_0-I/O_{15}	Way-B
L	L	H	X	X	L	H	Write I/O_0-I/O_7	Way-A
L	L	H	X	X	H	L	Write I/O_0-I/O_7	Way-B
L	H	L	X	X	L	H	Write I/O_8-I/O_{15}	Way-A
L	H	L	X	X	H	L	Write I/O_8-I/O_{15}	Way-B
L	L	L	X	X	L	H	Write I/O_0-I/O_{15}	Way-A
L	L	L	X	X	H	L	Write I/O_0-I/O_{15}	Way-B
L	L	H	X	X	L	L	Write I/O_0-I/O_7	Way-A & B
L	H	L	X	X	L	L	Write I/O_8-I/O_{15}	Way-A & B
L	L	L	X	X	L	L	Write I/O_0-I/O_{15}	Way-A & B

DIRECT ACCESS MODE (MODE = LOW)

$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{OE_a}$	$\overline{OE_b}$	$\overline{WE_a}$	$\overline{WE_b}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O_0-I/O_7
L	H	L	L	L	H	H	Read I/O_8-I/O_{15}
L	L	L	L	L	H	H	Read I/O_0-I/O_{15}
L	L	H	X	X	L	L	Write I/O_0-I/O_7
L	H	L	X	X	L	L	Write I/O_8-I/O_5
L	L	L	X	X	L	L	Write I/O_0-I/O_{15}

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.3	W
Storage Temperature	T_{stg}	−30 to +125	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature Range Under Bias	T_{BIAS}	−10 to +85	°C

* NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_A=0°C$ to $+70°C$)

Parameter	Symbol	Test Conditions		Min	Max	Units
Input Leakage Current	I_{IL}	V_{CC}=Max, V_{IN}=GND to V_{CC}		−1	+1	μA
Output Leakage Current	I_{OL}	Output Disabled		−1	+1	μA
Operating Current	I_{CC}	V_{CC}=Max	−20		230	mA
		I_{OUT}=0mA	−25		220	
		Duty Cycle=35% Single Way Write	−35		210	
Output Low Voltage	V_{OL}	I_{OL}=8mA V_{CC}=Min			0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA V_{CC}=Min		2.4		V
Input High Voltage	V_{IH}			2.2	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			−0.5	0.8	V

CAPACITANCE* ($T_A=25°C$, Freq=1MHz)

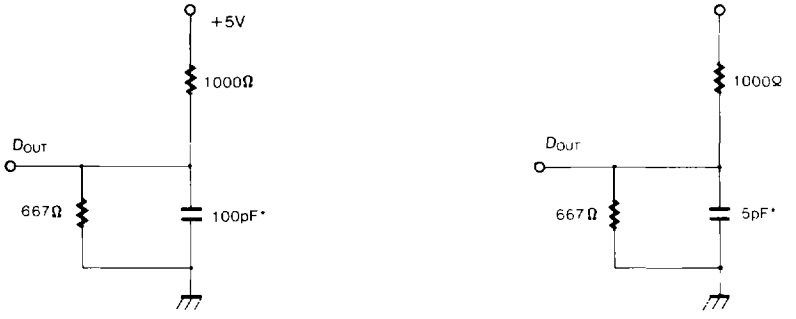
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

* Note: Sampled, not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



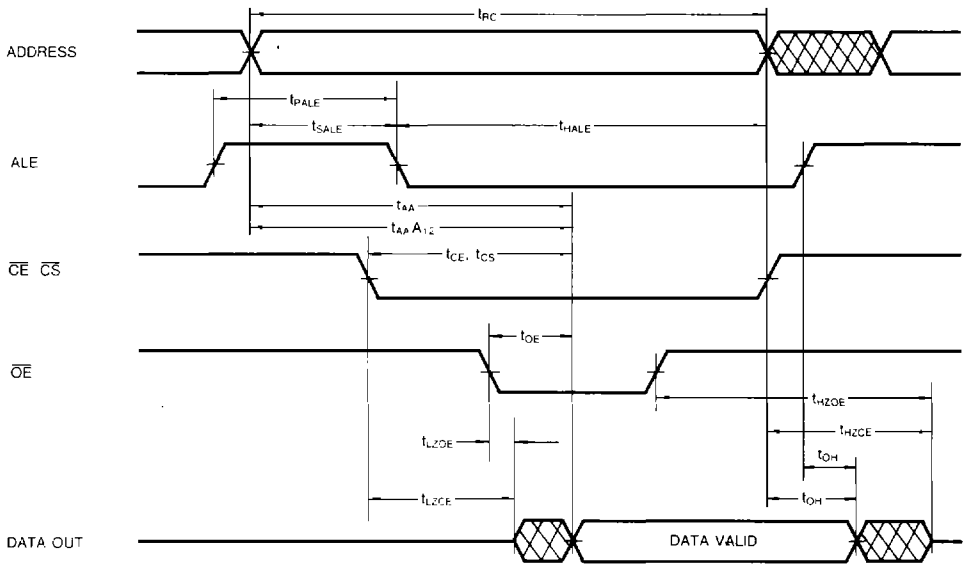
* Including Scope and Jig Capacitance

READ CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	Symbol	KM78C80-20		KM78C80-25		KM78C80-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
ALE Pulse Width	t_{PALE}	6		8		10		ns
Address Set-up to ALE Low	t_{SALE}	4		4		6		ns
Address Hold from ALE Low	t_{HALE}	4		4		4		ns
Address to Data Valid	t_{AA}		20		25		35	ns
Address A12 to Data Valid	$t_{AA\ A12}$		12		15		20	ns
Chip Enable to Data Valid	t_{CE}		10		12		15	ns
Chip Select to Data Valid	t_{CS}		10		12		15	ns
Output Enable to Data Valid	t_{OE}		8		10		12	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0		0		0		ns
CE and CS Low to Output Low-Z	t_{LZCE}	3		3		3		ns
Output Enable High to Output High-Z	t_{HZOE}		9		9		10	ns
CE or CS High to Output High-Z	t_{HZCE}		15		15		25	ns
Output Hold from Address Change (1)	t_{OH}	3		3		3		

Note 1: Data hold from address change or rising edge of ALE, whichever occurs later.

TIMING WAVEFORM OF READ CYCLE

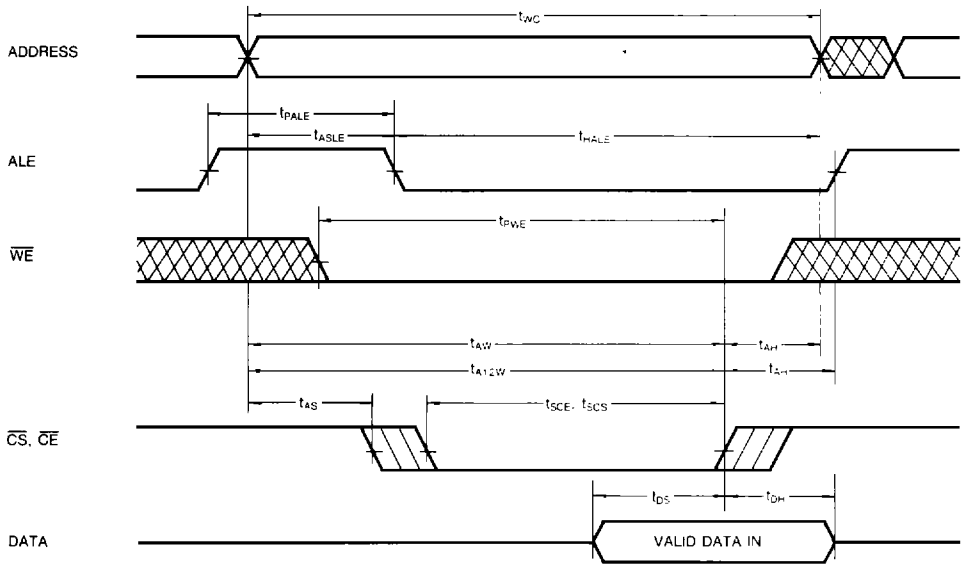


WRITE CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

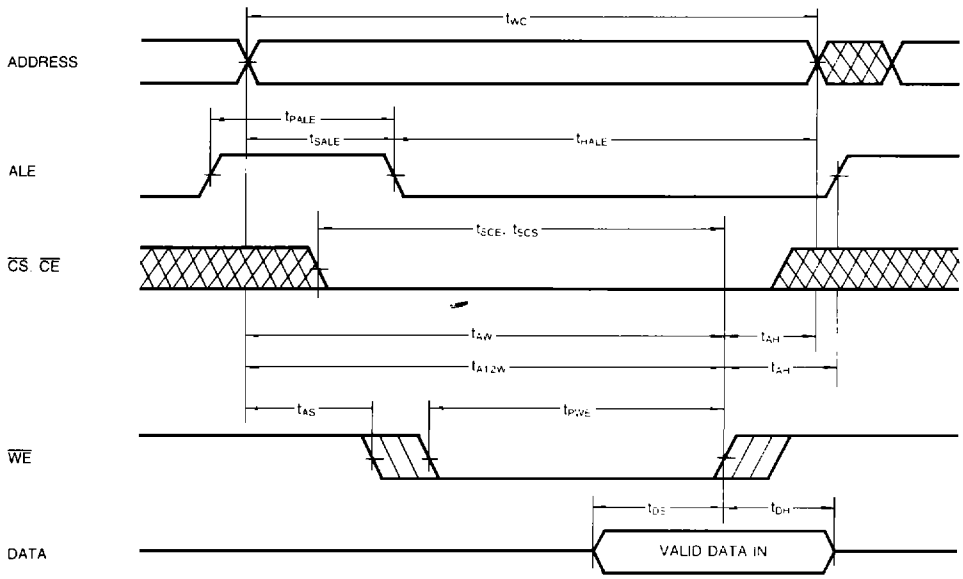
Parameter	Symbol	KM78C80-20		KM78C80-25		KM78C80-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
ALE Pulse Width	t_{PALE}	6		8		10		ns
Address Set-up to ALE Low	t_{SALE}	4		4		6		ns
Address Hold from ALE Low	t_{HALE}	4		4		4		ns
Chip Enable to Write End	t_{SCE}	15		20		25		ns
Chip Select to Write End	t_{SCS}	15		20		25		ns
Address Set-up to Write End	t_{AW}	15		20		30		ns
Address A12 Set-up to Write End	t_{A12W}	15		20		25		ns
Address Hold from Write End (1)	t_{AH}	0		0		0		ns
Address Set-up to Write Enable Low	t_{AS}	0		0		0		ns
Write Enable Pulse Width	t_{PWE}	15		20		25		ns
Write Enable Low to Output High-Z	t_{HZWE}		15		15		15	ns
Write Enable High to Output Low-Z	t_{LZWE}	3		3		3		ns
Data Set-up to Write	t_{DS}	10		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns

Note 1: Address should be held valid either by maintaining the address valid at the device address inputs or by latching the address with ALE.

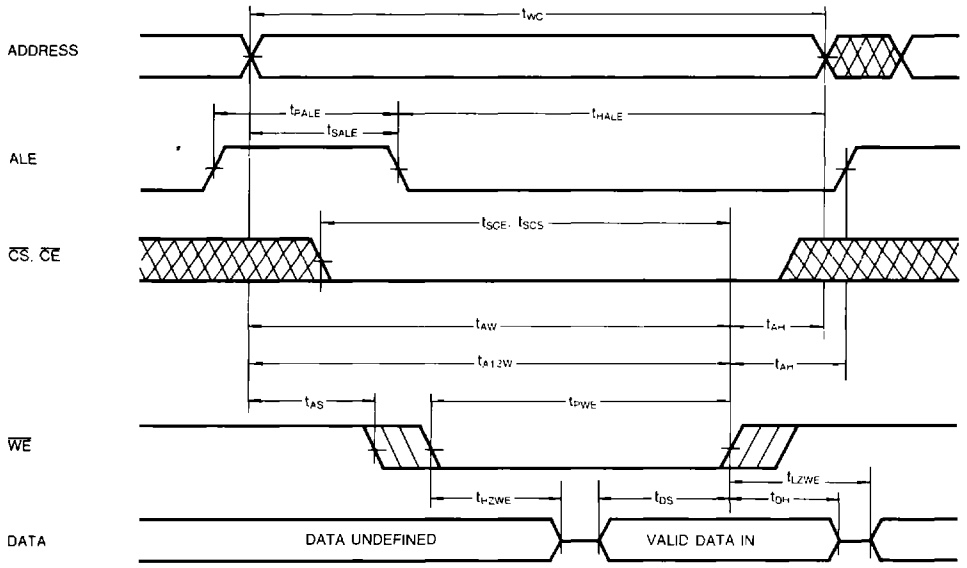
TIMING WAVEFORM OF WRITE CYCLE ($\overline{CE}$/$\overline{CS}$ Controlled, $\overline{OE}$ = H)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled, $\overline{OE}$ = H)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled, $\overline{OE}$ = H)



2

PACKAGE DIMENSIONS

52-PIN PLCC PACKAGE

Unit: Millimeters