ICS331-26

Single Output Clock Synthesizer

Description

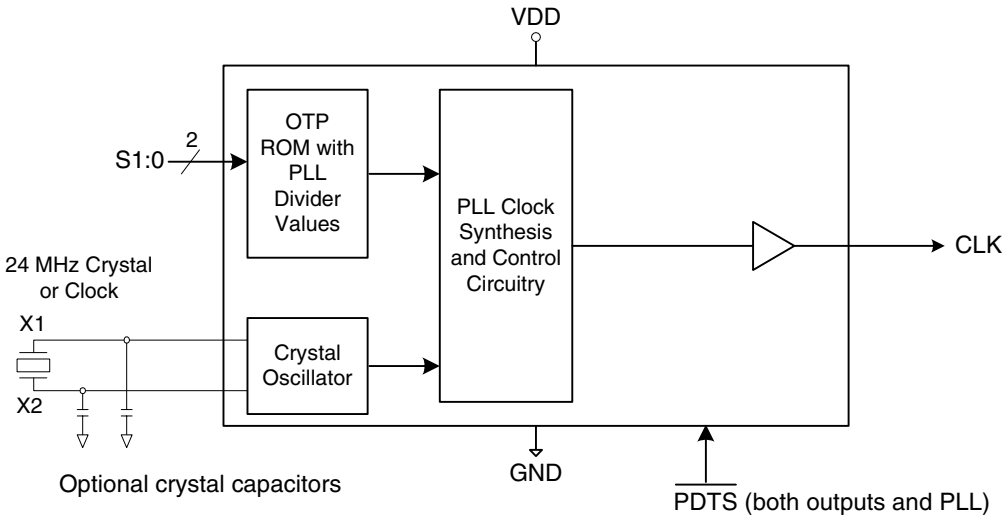
The ICS331-26 is a low cost frequency generator that is factory programmable. Using analog/digital Phase-Locked-Loop (PLL) techniques, the device accepts a 24 MHz clock input to produce selectable output clocks of 48 MHz and 72 MHz.

The device also has a power down feature that tri-states the clock outputs and turns off the PLLs when the $\overline{\text{PDTS}}$ pin is taken low.

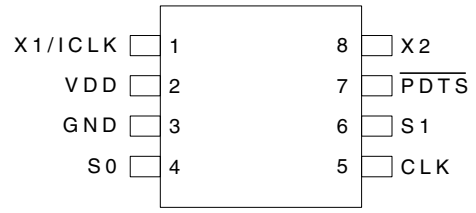
Features

- 8-pin SOIC package – Pb-free, RoHS compliant
- Input clock frequency of 24 MHz
- Selectable output clocks of 48 MHz or 72 MHz
- Spread spectrum
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



8 pin (150 mil) SOIC

Output Clock Selection Table

S1	S0	CLK (MHz)	Spread Percentage
0	0	48	±1.5%
0	1	72	±1.5%
1	0	48	±1.0%
1	0	72	±1.0%

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Connect this pin to a 24 MHz crystal or clock input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	S0	Input	Select pin 0 for frequency selection on CLK. Internal pull-up.
5	CLK	Output	Clock output per table above. Weak internal pull-down when tri-stated.
6	S1	Input	Select pin 1 for frequency selection on CLK. Internal pull-up.
7	$\overline{\text{PDTS}}$	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up.
8	X2	XO	Float for clock input.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS331-26 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors

must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS331-26. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS331-26. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	No load, $\overline{PDTS}$=1		18		mA
		No load, $\overline{PDTS}$=0		400		µA
Input High Voltage	V_{IH}	$\overline{PDTS}$ pin	VDD-0.5			V
Input Low Voltage	V_{IL}	$\overline{PDTS}$ pin			0.4	V
Input High Voltage	V_{IH}	SEL pin	2			V
Input Low Voltage	V_{IL}	SEL pin			0.4	V
Input High Voltage	V_{IH}	ICLK pin	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK pin			VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}			±70		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}	S0, S1, $\overline{PDTS}$ pins		360		kΩ
Internal Pull-down Resistor	R_{PD}	CLK output		510		kΩ

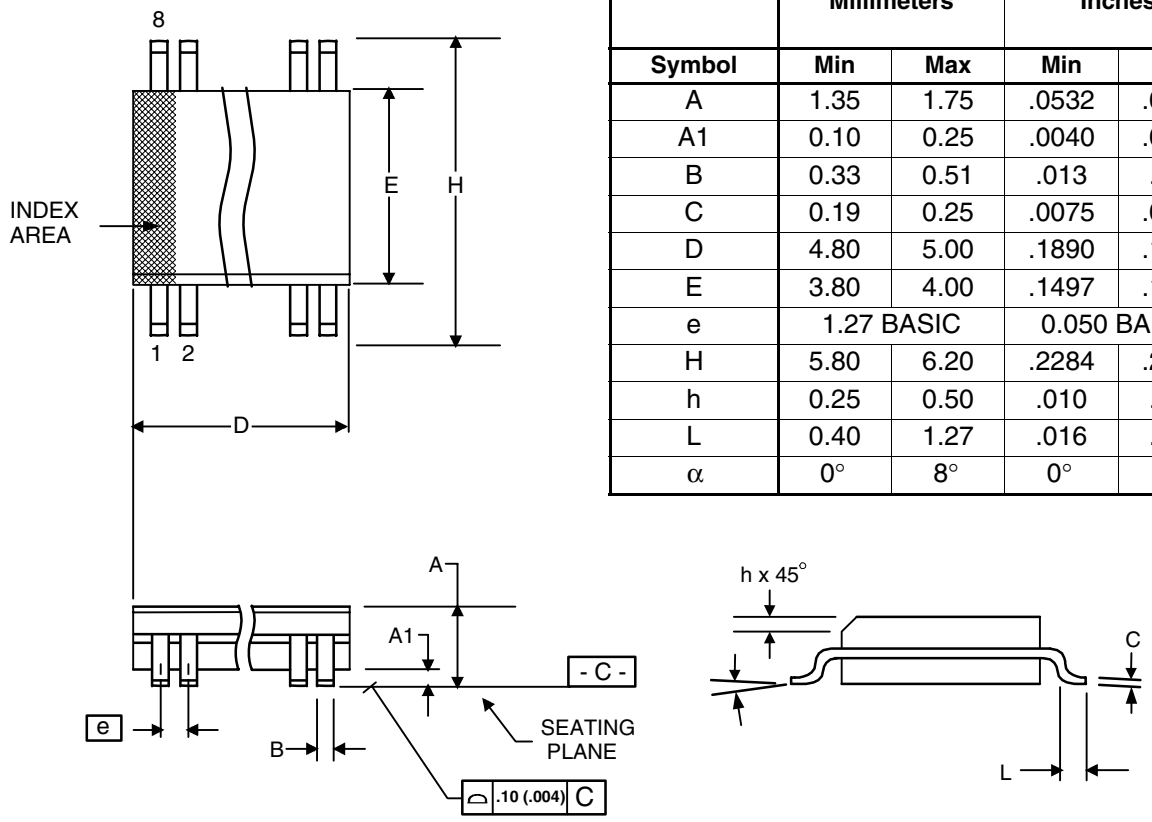
AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Rise Time	t_{OR}	0.8 to 2.0V, Note 1		1.0		ns
Output Fall Time	t_{OF}	2.0 to 0.8V, Note 1		1.0		ns
Duty Cycle		at VDD/2, Note 1	40		60	%
Cycle Jitter (short term jitter)	t_{ja}	cycle to cycle		150		ps
Input Frequency				24		MHz
Output Enable Time		$\overline{PDTS}$ high to spread profile stable		3		ms
Output Disable Time		$\overline{PDTS}$ low to tri-state		20		ns

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
331M-26LF	331M26LF	Tubes	8-pin SOIC	0 to +70° C
331M-26LFT		Tape and Reel	8-pin SOIC	0 to +70° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.