MIC2565

Dual Serial PCMCIA/CardBus Power Controller

Advance Information

General Description

The MIC2565 is an SMBus™-compatible, dual-slot PCMCIA* and CardBus power controller. It is a sophisticated power switching matrix that controls V_{CC} and V_{PP} voltages to two PC Card slots. The MIC2565 is used in conjunction with an SMBus logic controller (not provided by Micrel).

When connected to 3.3V, 5V, and 12V system power supplies, the MIC2565 can switch its V_{CC} outputs between 0V, 3.3V, 5.0V and high-impedance states at up to 1A and V_{PP} outputs between 0V, 3.3V, 5V, 12V, and high-impedance states at up to 250mA. Voltage rise and fall times are well controlled. The MIC2565 also features an efficient standby (sleep) mode at 0.3µA typical quiescent current.

12V and 5V supplies are not required for MIC2565 operation making it possible to omit one or both supplies when they are not required by the system. An internal charge pump supplies the voltages required for high-performance switching.

The MIC2565 power controller (slave) communicates with the logic controller (master) using SMBus, the new industry standard, two-wire, bidirectional, serial control bus. SMBus-based protocol allows full control of the power outputs and returns slot power status back to the logic controller.

The MIC2565 is protected by overtemperature shutdown, and protects itself and the system with current limiting and cross-conduction lockout.

The MIC2565 is available in a 28-pin SSOP.

* Personal Computer Memory Card International Association

Features

- Controls two card slots from one surface mount device
- SMBus™-compatible serial control bus (industry std.) reduces pin count and simplifies pcb layout
- Independent V_{CC} and V_{PP} voltage selection
- High-efficiency, low-resistance switches
- 12V supply optional (not required by MIC2565)
- External components not required
- Current limit and overtemperature shutdown
- Ultra-low power consumption
- Cross-conduction lockout (no switching transients)
- Break-before-make switching
- 1A minimum V_{CC} output per slot
- 250mA minimum V_{PP} output current per slot
- 28-pin surface-mount SSOP
- 4 discrete input/output points

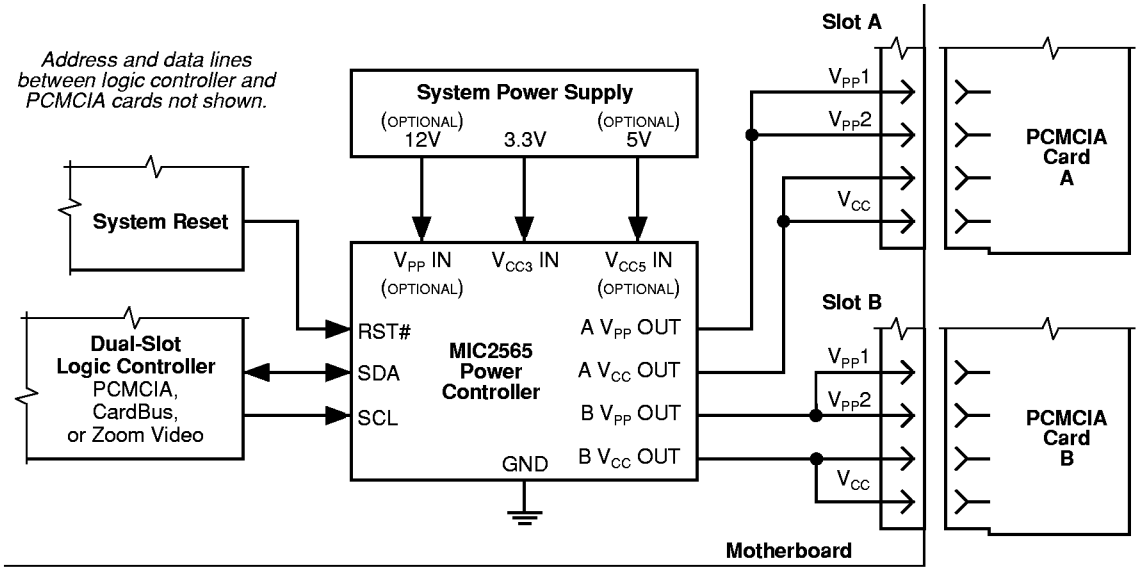
Applications

- PC Card and CardBus power control
- Zoom Video port power control
- Wireless communications
- Bar code data collection systems
- Docking stations (portable and desktop)
- Power supply management

Ordering Information

Part Number	Temperature Range	Package
MIC2565BSM	–40°C to +85°C	28-pin SSOP

Typical Application



PCMCIA Card Power Management Application

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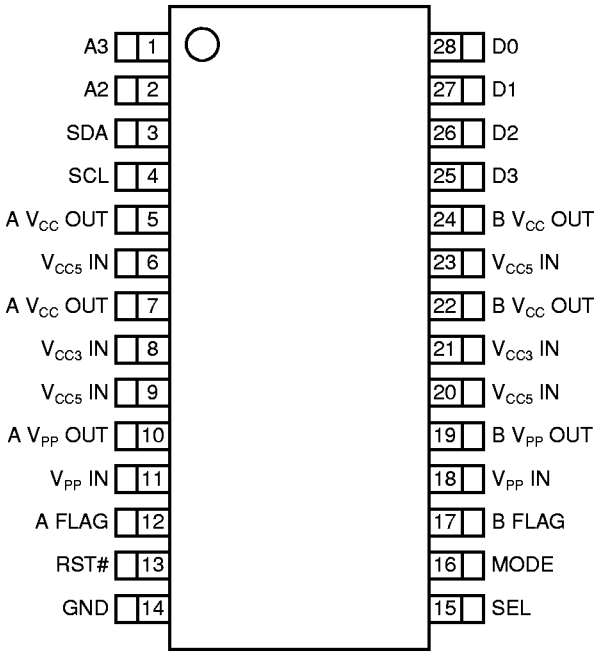
Pin Configuration



Duplicate pins must be connected together for proper operation.

Example: "A V_{CC3} IN" pins 5 and 7 must be connected.

28-lead SSOP (SM)

Pin Description

Pin Number	Pin Name	Pin Function
1, 2	A2–A3	SMBus Address Select (Input): Assigns specific SMBus device addresses within bank. Also see SEL.
3	SDA	Serial Data (Input/Output)
4	SCL	Serial Clock (Input)
5, 7	A V_{CC} OUT	Slot A V_{CC} Output
6, 9, 20, 23	V_{CC5} IN	5V Supply Input: Optional system power supply connection. Required only for 5V V_{CC} and V_{PP} output voltage.
8, 21	V_{CC3} IN	3.3V Supply Input: Required system power supply connection. Powers 3.3V V_{CC} and V_{PP} outputs and all internal circuitry.
10	A V_{PP} OUT	Slot A V_{PP} Output
11, 18	V_{PP} IN	12V Supply Input: Optional system power supply connection. Required only for 12V V_{PP} output voltage.
12	A FLAG	Slot A Fault Flag (Output): Open-drain output indicates power fault or transition at A V_{CC} OUT or A V_{PP} OUT.
13	RST#	System Reset (Input): Active low signal deactivates the MIC2565, clearing the serial registers and forcing the four power outputs to 0V (GND).
14	GND	Ground
15	SEL	Bank Select (Input): Selects one of two predefined SMBus address banks.
16	MODE	Protocol Mode Select (Input): Selects MIC2565 standard transaction protocols or simplified protocols.
17	B FLAG	Slot B Fault Flag (Output): Open-drain output indicates power fault or transition at B V_{CC} OUT or B V_{PP} OUT.

Absolute Maximum Ratings (Note 1)

V_{PP} IN ..... +14V
V_{CC3} IN ..... +4.0V
V_{CC5} IN ..... +6.0V
V_{SCL}, V_{SDA} ..... –0.3V to +6.0V
V_{A2}, V_{A3}, V_{SEL}, $V_{RST\#}$, V_{MODE} ..... –0.3V to +10V
V_{D0}, V_{D1}, V_{D2}, V_{D3} ..... –0.3V to +(V_{CC3} + 0.3V)
$V_{A\ FLAG}$, $V_{B\ FLAG}$ ..... +6.0V
A or B V_{PP} OUT ..... >200mA, Internally Limited
A or B V_{CC} OUT ..... >1A, Internally Limited
Power Dissipation at $T_A \le 25°C$ (P_D) ..... Internally Limited
Package Dissipation 800mW
Package Thermal Resistance (θ_{JA}) ..... 125°C/W
Junction Temperature (T_J) ..... +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (5 sec.) ..... +260°C

Operating Ratings (Note 1)

V_{PP} IN ..... 0V to +13.0V
V_{CC3} IN ..... +3.0V to +3.6V
V_{CC5} IN ..... 0V to +5.5V
V_{SCL}, V_{SDA} ..... 0V to +5.5V
V_{A2}, V_{A3}, V_{SEL}, $V_{RST\#}$, V_{MODE}, ... 0V to +5.5V
V_{D0}, V_{D1}, V_{D2}, V_{D3} ..... 0V to V_{CC3}
$V_{A\ FLAG}$, $V_{B\ FLAG}$ ..... 0V to +5.5V
A or B V_{PP} OUT ..... 0mA to 200mA
A or B V_{CC} OUT ..... 0mA to 1A
Ambient Temperature (T_A) ..... –40°C to +85°C

Electrical Characteristics

V_{CC3} IN = 3.3V, V_{CC5} IN = 5.0V, V_{PP} IN = 12V; $-40°C \le T_A \le +85°C$; unless noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PP} OUTPUT						
I_{PP} OUT Hi-Z	High Impedance Output Leakage Current	Shutdown Mode $0 \le V_{PP}$ OUT $\le 12V$		1		µA
I_{PPSC}	Short Circuit Current Limit	V_{PP} OUT = 0, Normal Mode V_{PP} OUT = 0, Standby Mode		0.3 10		A mA
R_O	Switch Resistance Normal Mode	Select V_{PP} OUT = 5V Select V_{PP} OUT = 3.3V I_{PP} OUT = –100mA (sourcing)		0.7 0.7		Ω Ω
R_O	Switch Resistance, Normal Mode. Select V_{PP} OUT = 12V	V_{PP} IN = 12V I_{PP} OUT = –100 mA (sourcing)		0.6		Ω
R_O	Switch Resistance, Select V_{PP} OUT = 0V	Select V_{PP} OUT = 0V (ground) I_{PP} OUT = 50µA (sinking)		2500		Ω
V_{PP} SWITCHING TIME (See Figure 1)						
t_1 t_2 t_3	Output Turn-On Delay, **Note 2**	V_{PP} OUT = Hi-Z to 10% of 3.3V V_{PP} OUT = Hi-Z to 10% of 5V V_{PP} OUT = Hi-Z to 10% of 12V		50 50 10		µs µs µs
t_4 t_5 t_6	Output Rise Time, **Note 2**	V_{PP} OUT = 10% to 90% of 3.3V V_{PP} OUT = 10% to 90% of 5V V_{PP} OUT = 10% to 90% of 12V		200 300 75		µs µs µs
t_7 t_8 t_9 t_{10}	Output Transition Timing, **Note 2**	V_{PP} OUT = 3.3V to 90% of 12V V_{PP} OUT = 5V to 90% of 12V V_{PP} OUT = 12V to 90% of 3.3V V_{PP} OUT = 12V to 90% of 5V		75 75 200 350		µs µs µs µs
t_{14} t_{15} t_{16}	Output Turnoff Delay Time, **Notes 2, 4**	V_{PP} OUT = 3.3V to Hi-Z V_{PP} OUT = 5V to Hi-Z V_{PP} OUT = 12V to Hi-Z		75 75 75		µs µs µs
t_{11} t_{12} t_{13}	Output Turnoff Fall Time, **Note 2**	V_{PP} OUT = 90% to 10% of 3.3V V_{PP} OUT = 90% to 10% of 5V V_{PP} OUT = 90% to 10% of 12V		75 75 75		µs µs µs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} OUTPUT						
I_{CCSC}	Short Circuit Current Limit	V_{CC} OUT = 0: Normal Mode V_{CC} OUT = 0: Standby Mode		1.5 50		A mA
R_O	Switch Resistance, Normal Mode	Select V_{CC} OUT = 3.3V I_{CC} OUT = –1A (sourcing) Select V_{CC} OUT = 5V I_{CC} OUT = –1A (sourcing) Select V_{CC} OUT = 0V (ground) I_{CC} OUT = 0.1mA (sinking)		120 70 500		mΩ mΩ Ω
V_{CC} SWITCHING TIME (See Figure 2)						
t_1 t_2	Output Turn-On Delay Time, **Note 3**	V_{CC} OUT = 0V to 10% of 3.3V V_{CC} OUT = 0V to 10% of 5.0V		150 200		µs µs
t_3 t_4	Output Rise Time, **Note 3**	V_{CC} OUT = 10% to 90% of 3.3V V_{CC} OUT = 10% to 90% of 5V		1000 1500		µs µs
t_7 t_8	Output Turnoff Delay, **Notes 3, 4**	V_{CC} OUT = 3.3V V_{CC} OUT = 5V		100 100		µs µs
t_5 t_6	Output Fall Time, **Note 3**	V_{CC} OUT = 90% to 10% of 3.3V V_{CC} OUT = 90% to 10% of 5.0V		3000 4000		µs µs
POWER SUPPLY						
I_{CC5}	V_{CC5} IN Supply Current (5V)	V_{CC} OUT = 5V or 3.3V, I_{CC} OUT = 0 V_{CC} OUT = 0V (Sleep Mode)		10 0.2		µA µA
I_{CC3}	V_{CC3} IN Supply Current (3.3V) **Note 5**	V_{CC} OUT = 5V or 3.3V, I_{CC} OUT = 0 V_{CC} OUT = 0V (Sleep Mode)		50 5		µA µA
I_{PP} IN	V_{PP} IN Supply Current (12V) **Note 6**	V_{PP} OUT = 3.3V or 5V. I_{PP} OUT = 0 V_{PP} OUT = Hi-Z, 0 or V_{PP}		0.3 0.3		µA µA
V_{CC5}	Operating Input Voltage (5V)	V_{CC5} IN not required for operation		5.0		V
V_{CC3}	Operating Input Voltage (3.3V)	**Note 5**				V
V_{PP} IN	Operating Input Voltage (12V)	V_{PP} IN not required for operation				V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature			130		°C
SMBus INTERFACE DC SPECIFICATIONS						
V_{IH}	Input Voltage: SDA, SCL pins					V
V_{IL}						V
V_{THRES}	Input Logic Threshold			1.2		V
I_{IN}	Input Current	$0V < V_{IN} < 5.5V$				µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SMBus INTERFACE AC SPECIFICATIONS						
f_{SMB}	Operating Frequency					kHz
t_{BUF}	Bus Free Time Between sto**P** and **S**tart Conditions			4.7		µs
$t_{HD:STA}$	Hold Time After Repeated **S**tart Condition (until first clock is generated)			4.0		µs
$t_{SU:STA}$	Repeat **S**tart-Condition Setup Time			4.7		µs
$t_{SU:STO}$	sto**P**-Condition Setup Time			4.0		µs
$t_{HD:DAT}$	SDA Hold Time					ns
$t_{SU:DAT}$	SDA Setup Time					ns
t_{LOW}	SCL Low Time					µs
t_{HIGH}	SCL High Time					µs
$t_{LOW:SP}$	**S**tart/sto**P**-Condition Low Time			20		µs
t_F	SCL/SDA Fall Time					ns
t_R	SCL/SDA Rise Time					ns

General Note: Devices are ESD sensitive. Handling precautions recommended.

Note 1: Functional operation outside the operating ratings is not implied.

Note 2: R_L = 1000Ω connected to ground.

Note 3: R_L = 10Ω connected to ground.

Note 4: Delay from commanding Hi-Z or 0V to beginning slope. Does not apply when device is in current limit or overtemperature shutdown.

Note 5: The MIC2565 requires V_{CC3} IN for operation.

Note 6: V_{PP} IN and V_{CC5}IN are not required for operation.

Electrical Characteristics

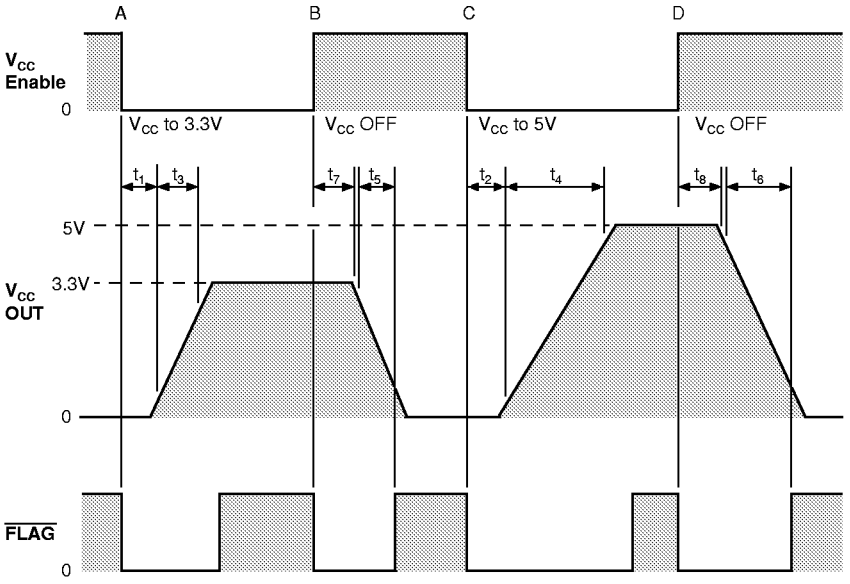


Figure 1. MIC2565 V_{CC} Timing Diagram

V_{CC} Enable is shown generically. R_L = 10Ω. Refer to the serial control timing diagrams for specific control logic input. At time **A**) V_{CC} is programmed to 3.3V, **B**) V_{CC} is disabled, **C**) V_{CC} is programmed to 5V, **D**) V_{CC} is disabled.

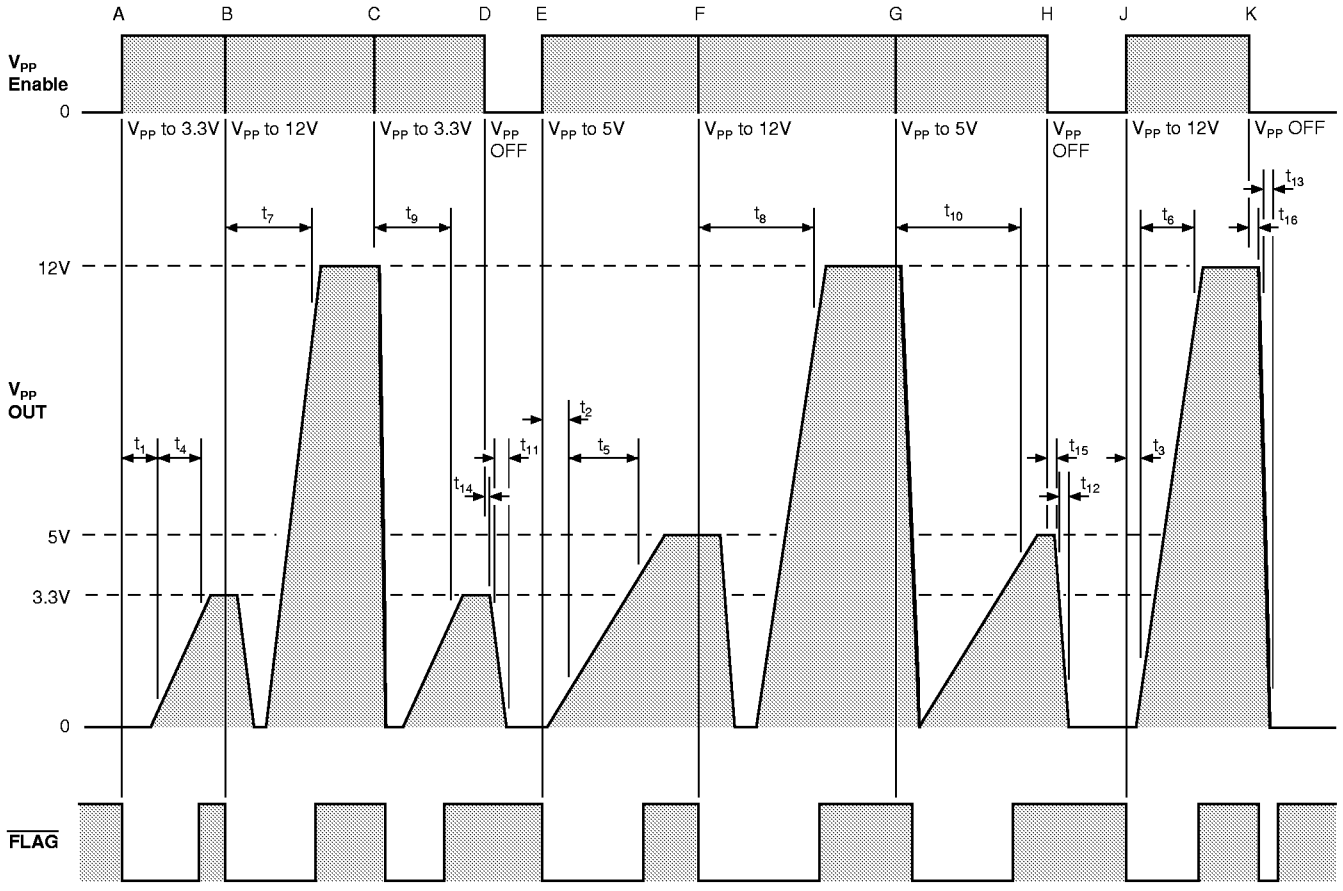
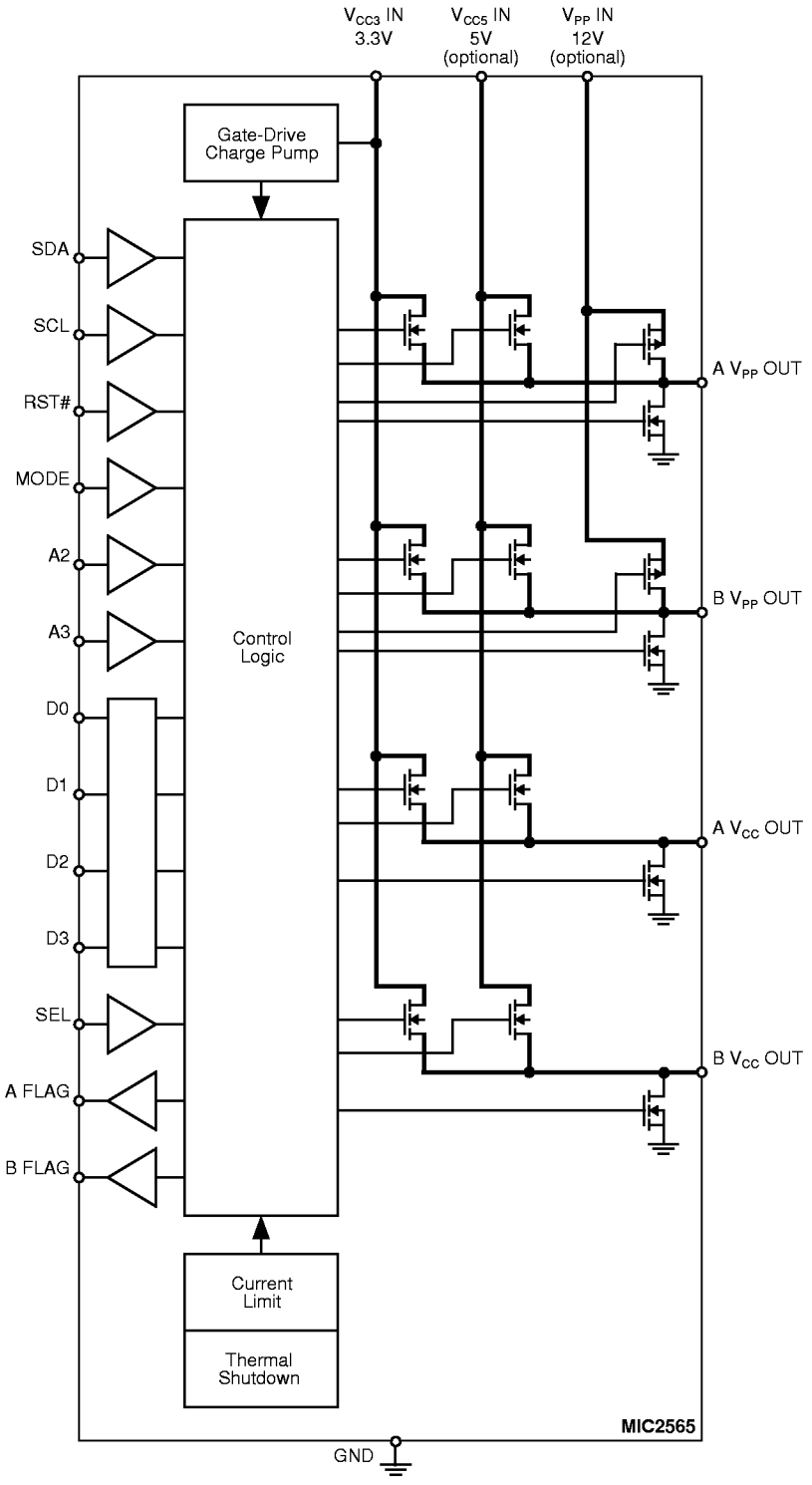


Figure 2. MIC2565 V_{PP} Timing Diagram

V_{PP} Enable is shown generically. R_L = 100Ω. C_L = negligible. Refer to the serial control timing diagrams for details. At time **A**) V_{PP} = 3.3V is selected, **B**) V_{PP} is set to 12V, **C**) V_{PP} = 3.3V (from 12V), **D**) V_{PP} is disabled, **E**) V_{PP} is programmed to 5V, **F**) V_{PP} is set to 12V, **G**) V_{PP} is programmed to 5V, **H**) V_{PP} is disabled, **J**) V_{PP} is set to 12V, **K**) V_{PP} is again disabled.

Functional Diagram



Applications Information

PC Card power control for two sockets is easily accomplished using the MIC2565 PC Card/CardBus power controller. Control commands from a two-wire serial bus determine V_{CC} and V_{PP} output voltages and standby or operate mode.

V_{CC} outputs of 3.3V and 5V at the maximum allowable PC Card current are supported. The V_{CC} outputs also support GND (0V) and high-impedance states. The V_{PP} outputs support V_{PP} (12V), V_{CC} voltages (3.3V or 5V), GND (0V), or high impedance. When the "V_{CC} = 0V" condition is selected, the device switches into "sleep" mode and draws only leakage current.

Full protection during hot switching is provided which prevents feedback from the V_{CC} output (from 5V to 3.3V, for example) by locking out the low voltage switch until the initial switch's gate voltage drops below 0.7V.

The MIC2565's internal logic and MOSFET drive circuitry is powered from the V_{CC3} input and internal charge-pump voltage multipliers. Switching speeds are carefully controlled to prevent damage to sensitive loads and meet all PC Card Specification timing requirements, including those for the CardBus option.

Supply Bypassing

External capacitors are not required for operation. The MIC2565 is a switch and has no stability problems. For improved output ripple, bypass the V_{CC3} IN, V_{CC5} IN, and V_{PP} IN inputs with 1µF capacitors. As all internal device logic and comparison functions are powered from the V_{CC3} IN line, the power supply quality of this line is the most important and a bypass capacitor may be necessary for some layouts. The V_{CC} OUT and V_{PP} OUT pins may use 0.01µF to 0.1µF capacitors for noise reduction and to reduce the chance of ESD (electrostatic discharge) damage.

PC Card Slot Implementation

The MIC2565 is designed for full compatibility with the Personal Computer Memory Card International Association (PCMCIA) PC Card Specification (March 1995) including the CardBus option. See "Typical Application."

When a PC card is initially inserted, it should receive V_{CC} (3.3V ± 0.3V or 5.0V ±5%). The initial voltage is determined by a combination of mechanical socket "keys" and voltage sense pins. The card sends a handshaking data stream to the logic controller, which then determines if this card requires V_{PP} and if the card is designed for dual V_{CC}. If the card is compatible with, and requires, a different V_{CC} level, the logic controller commands the power controller to make this change by disabling V_{CC}, waiting at least 100ms, and then re-enabling the other V_{CC} voltage.

V_{CC} switches are turned on and off slowly. If commanded to immediately switch from one V_{CC} to another (without turning off and waiting 100ms first), enhancement of the second switch begins only after the first is off (break-before-make protection) and V_{CC} OUT has fallen below 0.7V. V_{PP} switches are turned on and off slowly. A V_{PP} switch is not turned on until all other V_{PP} switches are off, which prevents cross conduction.

If no card is inserted, or the system is in sleep mode, the logic controller commands the MIC2565 to shut down V_{CC}. This also places the switch into a shutdown (sleep) mode, where current consumption drops to nearly zero, with only tiny CMOS leakage currents flowing.

Internal device control logic and MOSFET drive and bias voltage is powered from V_{CC3} IN. The high voltage bias is generated by an internal charge pump multiplier. Input logic threshold voltages are compatible with common PC Card logic controllers using either 3.3V or 5V supplies.

Flash Memory Implementation

When programming flash memory (standard +12V flash memories), the PC Card slot logic controller enables V_{PP} on the MIC2565, which connects V_{PP} IN (nominally +12V) to V_{PP} OUT. The low on-resistance of the MIC2565 switch allows using a small bypass capacitor on the V_{PP} OUT pins, with the main filtering performed by a large filter capacitor on V_{PP} IN. (Usually the main power supply filter capacitor is sufficient.) Using a small-value capacitor such as 0.1µF on the output causes little or no timing delays.

The V_{PP} OUT transition from V_{CC} to 12.0V typically takes 250µs. After programming is completed, the logic controller signals to the MIC2565, which then reduces V_{PP} OUT to the V_{CC} level. Break-before-make switching action and controlled rise times reduce switching transients and lower current spikes through the switch.

Output Current and Protection

MIC2565 output switches are capable of passing the maximum current needed by any PC Card. The MIC2565 meets or exceeds all PCMCIA specifications. For system and card protection, output currents are internally limited. For full system protection, long term (millisecond or longer) output short circuits invoke overtemperature shutdown, protecting the MIC2565, the system power supplies, the card socket pins, and the PC Card. Individual open-drain error flags and internal status registers for each slot indicate when power problems exist.

In the standby mode, the MIC2565 features a reduced current limit on both the V_{CC} and V_{PP} outputs. This feature protects sleeping computer systems from inadvertent rebooting if the card suddenly demands more current than the standby-mode power supply can deliver.

Control Bus Interface Overview

The MIC2565 power controller (slave) communicates with a logic controller (master) via a two-wire interface. This interface is a compatible subset of the System Management Bus (SMBus) developed by Intel Corporation.

The MIC2565 supports an enhancement (**S**tart/sto**P**) that allows a slave-only SMBus device to signal the host without requiring an optional hardware interrupt line.

Control Bus Electrical Interface

The two wires of the MIC2565 communication interface are SCL (serial clock) and SDA (serial data). Figure 1 shows that SCL is a unidirectional clock input and SDA is bidirectional and accommodates data input (write) and output (read) operations. The open-drain SDA output is part of a wired-OR configuration that supports multiple devices on this bus. The SDA signal line must have a pull-up (usually a resistor) in the system.

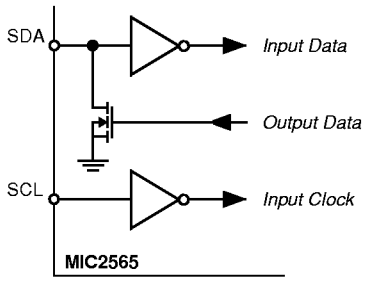


Figure 1. Serial Port Interface

Interface Signal Conditions

There are four signal conditions associated with transactions on the two-wire interface. Figure 2 illustrates these conditions, two of which are used to frame data transfers in conformance to a protocol.

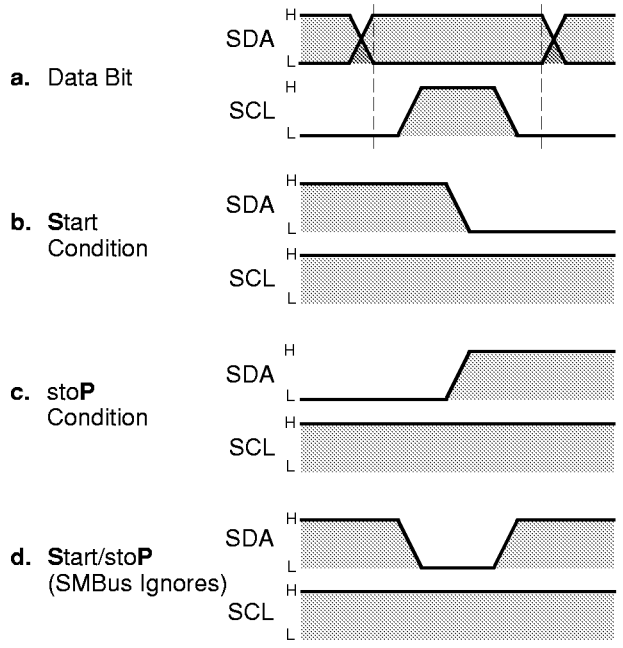


Figure 2. Serial Port Signal Conditions

Data Read and Write

Figure 2a shows that, when reading or writing a data bit, data on SDA must be stable for a setup time prior to the rising edge of the clock SCL, and data must remain stable until after a hold time following the falling edge of the clock. SDA is allowed to change state only when SCL is low.

Start, Stop, and Interrupt

Three additional signal conditions are defined by changing SDA's state while the clock is high: **S**tart (Figure 2b), sto**P** (Figure 2c), and **S**tart/sto**P** (Figure 2d).

Start and sto**P** are the conditions used to "frame" or identify the beginning and end of transactions. A transaction is a complete, two-way communications exchange between the logic controller (master) and MIC2565 power controller (slave).

Start/sto**P** is a special condition (interrupt) asserted by the MIC2565 (slave) to alert the logic controller (master). Figure 3 illustrates these conditions within a partial signal stream on the SCL and SDA lines.

The MIC2565 will correctly recognize a **S**tart condition at any time after RST# (reset) is logic high.

Clock

The MIC2565's internal state machine is implemented with static logic, so the frequency of SCL (clock input) may range from dc to 100kHz. The part readily accepts a stretched clock from the controller (as if the clock had been temporarily halted and then resumed). The MIC2565 itself does not stretch the clock and does not respond to the SMBus timeout.

Addresses

The MIC2565 has two address types: SMBus addresses and register addresses. SMBus addresses identify individual MIC2565 card slots on the SMBus. Register addresses identify specific read or write registers associated with the selected card slot. Refer to figures 5, 6, and 7 for usage within transactions.

SMBus Addresses

Each MIC2565 occupies two consecutive SMBus addresses, one for each of the two card slots. (The MIC2565 is a *dual* card-slot power controller; each controller appears as one SMBus device) The MIC2565 is assigned its SMBus addresses using the SEL (bank select), A3, and A2 pins. There can be one or more MIC2565 power controllers on an SMBus.

Each SMBus device address is seven bits in length, identified as A7 though A1 in Table 1. (Individual SMBus address transmissions within a transaction are a byte long, however, the "bit 0" portion of the byte is used to identify the transmission as a read or write request.)

Bank Select

The SEL input pin selects one of two predefined address banks designated by bits A7, A6, A5, and A4. See Table 1 for the MIC2565 standard bank addresses. Although these addresses have been *proposed* for the SMBus specification for PC Card/CardBus power control functions, they are not, at this printing, officially specified or allocated.

Bank addresses are factory mask programmable if addresses outside of the standard range are required.

Address Pins

The A3 and A2 address input pins assign the specific SMBus addresses within the selected address bank. Pins A3 and A2 correspond to SMBus address bits A3 and A2, as shown in Table 1.

Bank Select Pin	7-Bit SMBus Address AAAA AAA 7654 321 Note 8	Function	Comment
0	0011 XXY **Note 9**	selects address bank 0	bits A7–A4 are factory configured
1	1101 XXY **Note 9**	selects address bank 1	bits A7–A4 are factory configured
x	0001 100 **Note 10**	alert response address	addresses all slaves

Table 1. Proposed PC Card/CardBus Power Control SMBus Addresses

Note 8: The bit "A0" position is occupied by the read/write control bit.

Note 9: "Y" (LSB = A1) represents the slot selection bit (0 = Slot A; 1 = Slot B)

Note 10: Requests all devices with pending interrupts to send their address using the modified receive byte protocol (see Figure 7).

Slot Addressing

Card slot A or slot B is selected by SMBus address bit A1 which is transmitted during a transaction. (A1 = 0 selects card slot A, A1 = 1 selects card slot B.)

Alert Response Address

The alert response address is a unique address which the controller uses to request a response from slaves, such as the MIC2565, that have an interrupt pending. All slaves on the bus decode this address. Refer to the "Modified Receive Byte Protocol" section for details.

Registers and Register Addresses

The registers, their internal addresses, their bit allocations, and functions are shown in Table 2a and 2b.

Register Addr. Hex	Binary	Data Written	Function
00	0000 0000	0ccc 0ppp	Voltage select
01	0000 0001	sxxx xxx0	Standby control
02	0000 0010	xxxx xxxx	None
03	0000 0011	xxxx xxxx	None
04	0000 0100	xxxx xxxx	None
05	0000 0101	DDDD eeee	Write and selectively enable discrete I/O bits

Table 2a. Write Registers

Register Addr. Hex	Binary	Data Read	Function
80	1000 0000	0000 0000	None
81	1000 0001	s000 0000	Standby status
82	1000 0010	1101 1010	Interrupt Mask
83	1000 0011	hj0m f0u0	Interrupt Flags, **Note 11**
84	1000 0100	hjkm fpu0	Status Flags
85	1000 0101	DDDD 0000	Read discrete I/O pin pin data, **Note 12**

Table 2b. Read Registers

Six registers are provided for writing and six are provided for reading. Note that writing to only three of the six registers provided is meaningful: Voltage Selection, Standby Control, and Discrete Input/Output (I/O). Similarly, reading from five of the six provided registers is meaningful. Any attempt to write to a read-only register is ignored; any attempt to read from a write-only register will return all zeros.

Writing to a register outside those in the table is ignored and reading from a register outside those in the table will return all zeros.

Abbreviations

ccc	"V_{CC} select" code
ppp	"V_{PP} select" code
s	standby bit
x	don't care
e	enable output bit driver
D	discrete output bit value
h	thermal shutdown
j	V_{CC} okay
k	V_{CC} slewing
m	V_{CC} current limit
f	V_{PP} okay
u	V_{PP} current limit

Note 11: Interrupt flags are reset when they are read.

Note 12: The state I/O *pin* is read, which is not necessarily the state of the corresponding discrete output data.

Voltage Select Codes

The V_{CC} and V_{PP} voltage selection codes shown in Tables 3a and 3b are used to select the supply voltages that are output to the card slots. These codes are part of the "Data Written" to register 00_{HEX} as shown in Table 2a.

V_{CC} Code (ccc)	V_{CC}
000	Ground
001	Ground
010	5V
011	3.3V
100	Ground
101	Ground
110	Ground
111	High Impedance

Table 3a. V_{CC} Voltage Selection Codes

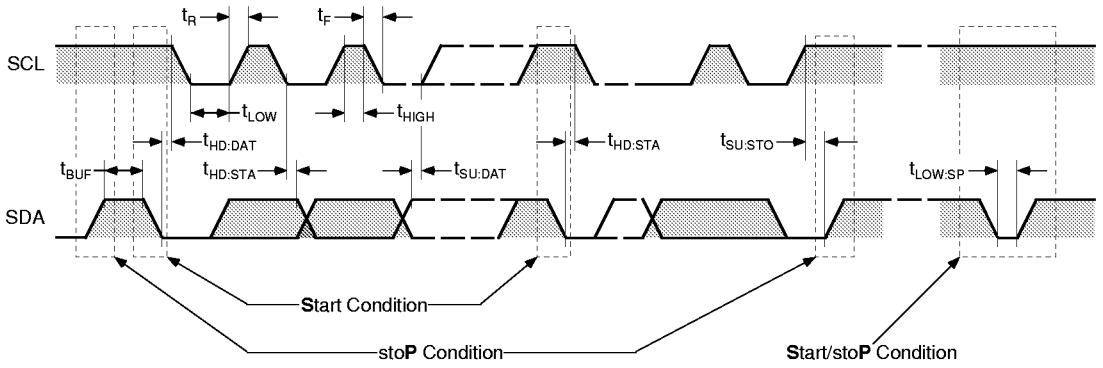


Figure 3. Interface Transaction Protocols

V_{PP} Code (PPP)	V_{PP}
000	Ground
001	12V
010	5V
011	3.3V
100	Ground
101	Ground
110	Ground
111	High Impedance

Table 3b. V_{PP} Voltage Selection Codes

Interface Transaction Protocols

There are three types of bus transactions that are supported by the MIC2565: Write-Byte Protocol, Read-Byte Protocol, and Modified Receive Byte Protocol.

With the exception of **S**tart/sto**P** condition timing, all transactions are timed by the controller clock (SCL). Figure 4 shows the bit order with respect to time (MSB first, LSB last).

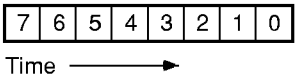


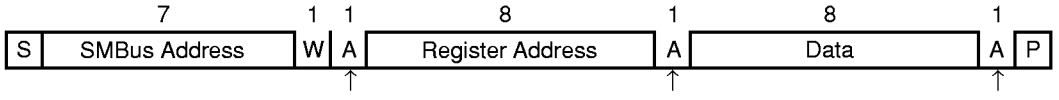
Figure 4. Communications Bit Order

Write-Byte Protocol

The format, or protocol, for writing a byte to the MIC2565 is shown in Figure 8. Bytes are written to the MIC2565 to effect controls or output discrete data as summarized in Table 2a.

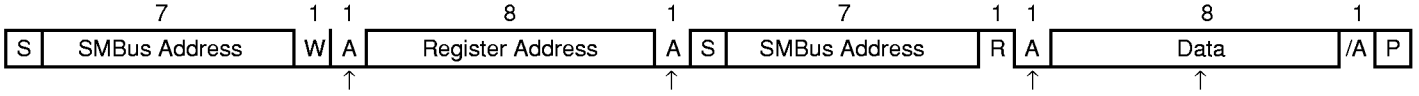
The write byte transaction consists of:

1. controller sends **S**tart
2. controller sends SMBus (device) address
3. controller sends **W**rite bit (active low)
4. MIC2565 sends **A**cknowledge bit (active low)
5. controller sends MIC2565 register address
6. MIC2565 sends **A**cknowledge bit (active low)
7. controller sends data byte
   (the data byte is a either a command or discrete outputs and enables)
8. MIC2565 sends **A**cknowledge bit (active low)
9. controller sends a sto**P**



↑ *data sent by MIC2565*
S **S**tart condition
W **W**rite request bit
A **A**cknowledge bit (active low)
/A **not A**cknowledge bit (inverse A)
P sto**P** condition

Figure 5. Write Byte Transaction Protocol



↑ *data sent by MIC2565*
S **S**tart condition
R **R**ead request bit
W **W**rite request bit
A **A**cknowledge bit (active low)
/A **not A**cknowledge bit (inverse A)
P sto**P** condition

Figure 6. Read Byte Transaction Protocol

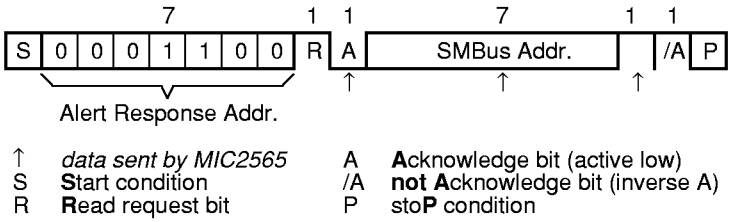


Figure 7. Modified Receive Byte Transaction Protocol

Read-Byte Protocol

The format, or protocol, for reading a byte from the MIC2565 is also shown in Figure 6. Bytes are read from the MIC2565 to learn the status of various device signals or to read discrete inputs as summarized in Table 2b.

The read byte transaction consists of:

1. controller sends **S**tart
2. controller sends SMBus (device) address
3. controller sends **W**rite bit (active low)
4. MIC2565 sends an **A**cknowledge bit (active low)
5. controller sends MIC2565 register address
6. MIC2565 sends **A**cknowledge bit (active low)
7. controller sends another **S**tart
8. controller again sends SMBus (device) address
9. controller sends **R**ead bit (active high)
10. MIC2565 sends **A**cknowledge bit (active low)
11. MIC2565 sends data byte
    (the data byte is standby status, interrupt mask or flags, status flags, or discrete input)
12. controller sends **not A**cknowledge bit (logic high)
13. controller sends sto**P**

Modified Receive Byte Protocol

The format, or protocol, for a modified receive byte is shown in Figure 7. This bus transaction is for servicing interrupts.

When an SMBus device signals a controller, which may be via the SMBALERT# (third-wire option, not supported by the MIC2565) or the **S**tart/sto**P** condition (implemented by the MIC2565), a controller (master) needs to determine which of several possible devices (slaves) requires attention. The controller may poll all the slaves or use the SMBus Alert transaction (modified receive byte) to identify which slaves have requested attention.

After receiving a **S**tart/sto**P** (interrupt) from the MIC2565 (slave), the logic controller (master) sends a **S**tart condition and the SMBus alert response address. This unique address is decoded by all slaves on the bus and informs them that the master wants to know if they have fault conditions or other interrupts pending. The controller also sends a **R**ead bit (active high). Slaves requiring service will respond with an **A**cknowledge bit (active low) and the slave's SMBus device address.

Interrupt Management

Multiple slaves will simultaneously send their addresses if more than one requires service. To detect a data collision on the bus, the MIC2565 monitors the SDA line bit-by-bit while sending its device address. Because the time order of sending bits is high-to-low, and because the SDA line is open-drain (slaves can only pull SDA low), it is simple to detect whether the address being sent is a higher address than any other involved in a collision. If the SDA line is pulled low and a logic-high signal was being sent, the address being sent is the higher address.

When a collision is detected, the slave with the higher address ceases sending data and the slave with the lower address continues communicating with the controller. The higher-address device (which has just forfeited communicating) must keep track of this situation and again attempt to communicate the request for service to the controller. In the MIC2565 this is again accomplished via the **S**tart/sto**P** condition.

The modified receive byte operation consists of:

1. controller sends **S**tart
2. controller sends SMBus alert response address
3. controller sends a **R**ead bit (active high)
4. MIC2565 sends an **A**cknowledge bit (active low if an interrupt is pending)
5. if an interrupt flag is set, MIC2565 sends its SMBus address plus a logic-high bit
6. controller sends **not A**cknowledge bit (logic high)
7. controller sends a sto**P**

Discrete Input/Outputs

The MIC2565 provides four discrete I/O (input/output) bits that can be used to control additional hardware in the PC Card/CardBus design. See Figure 9. Writing, selective enabling, and reading the discrete I/O bits is done with the write byte and read byte protocols. The four output bits, each of which can be individually enabled or disabled, are accessible through pins D0 through D3.

The four pins are also read as discrete input bits. Depending upon the written enable bits, the input logic states may or may not be the same as the bits that were written. A read always

indicates the actual pin output state, not necessarily the write register state.

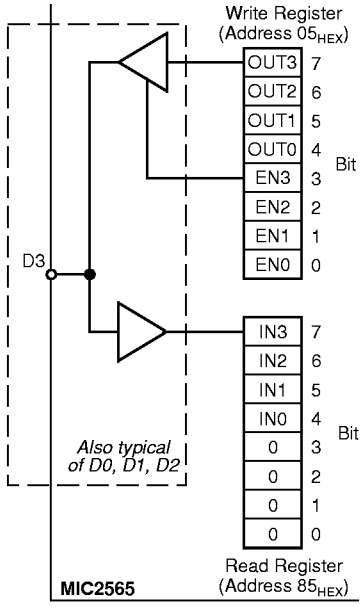


Figure 8. Discrete Input/Outputs

Reading Jumpers with Discrete Input/Outputs

The MIC2565's discrete I/Os can be used to detect the configuration of up to four jumpers or switches. Refer to Figure 9 for a typical discrete I/O with a jumper attached.

The presence of a jumper can be detected by commanding a discrete output high and reading its actual state from the corresponding discrete input. If the output pin reads high, the jumper is absent. If the output reads low, a jumper is present. The current available from each driver is limited to approximately 3.3mA by the driver's 1kΩ impedance.

The discrete output drivers source current from V_{CC3} IN. To conserve energy, especially in battery-powered applications, command the output high only when it is necessary to check for the presence of a jumper.

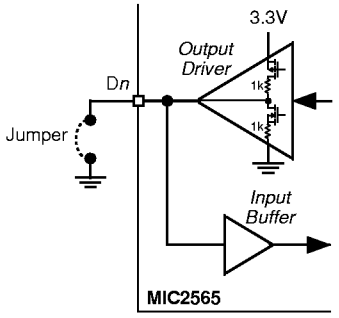


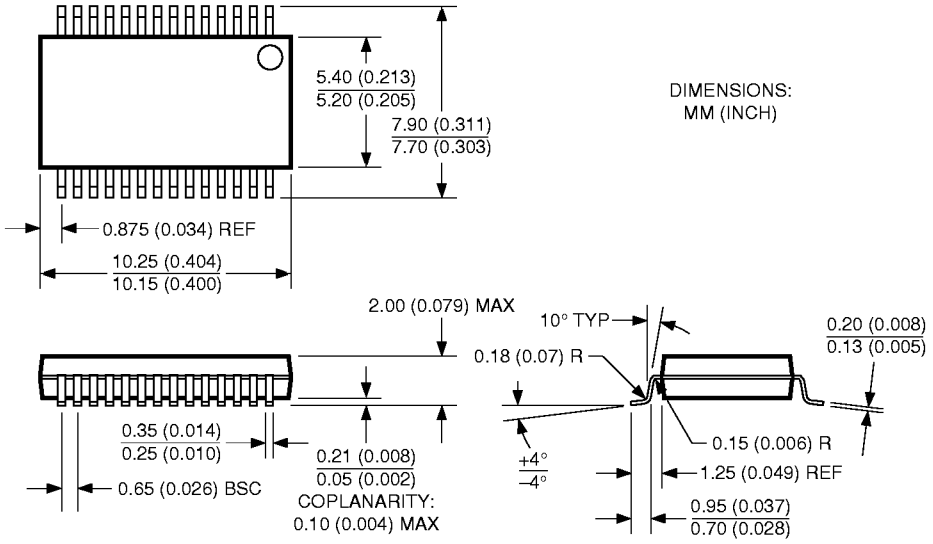
Figure 9. Typical Discrete Input/Output with Jumper

Communication Mode

The MIC2565 operates either in standard *MIC2565 SMBus-compatible communication mode*, or a *simplified SMBus-compatible communications mode*. The simplified mode is available for use with logic controllers that have limited communications capabilities. The MODE pin is used to configure the MIC2565's operating mode.

Contact Micrel applications for details.

Package Dimensions



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