

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Product Features

- Supports Intel 440BX, and VIA Promedia chipsets
- Supports mobile Pentium® II and Pentium® III
- 2 REF clocks
- 2 Low Skew (<175pS) CPU clocks
- 6 PCI Clocks (1 free running, 5 manageable)
- 1 48MHz fixed clock
- 1 selectable 48 or 24 MHz fixed clock
- Separate supply pins for mixed 3.3/2.5V application.
- High Speed host bus operation, up to 150MHz
- IMI Spread Spectrum technology for reducing EMI
- Rich Power Management Functions.
- 28-pin SSOP & TSSOP packages for minimum board space.

### Frequency Table(MHz)

| HFS# | SEL 100/66# | CPU(1:2) | PCI(_F,1:5) |
|------|-------------|----------|-------------|
| 1    | 0           | 66.6     | 33.3        |
| 1    | 1           | 100      | 33.3        |
| 0    | 0           | 150      | 37.5        |
| 0    | 1           | 133.3    | 33.3        |

Table 1

### Block Diagram

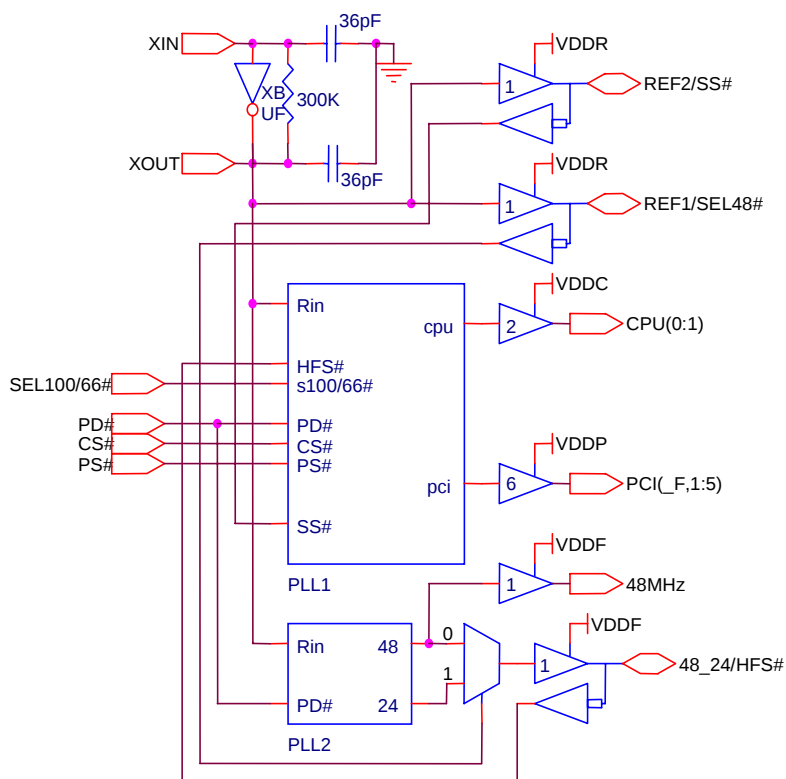


Fig.1

### Pin Configuration

|            |    |    |             |
|------------|----|----|-------------|
| VSS        | 1  | 28 | VDDR        |
| XIN        | 2  | 27 | REF1/SEL48# |
| XOUT       | 3  | 26 | REF2/SS#    |
| PCI_F      | 4  | 25 | VDDC        |
| PCI1       | 5  | 24 | CPU1        |
| PCI2       | 6  | 23 | CPU2        |
| VSS        | 7  | 22 | VSS         |
| VDDP       | 8  | 21 | VSS         |
| PCI3       | 9  | 20 | PS#         |
| PCI4       | 10 | 19 | VDD         |
| PCI5       | 11 | 18 | CS#         |
| VDDF       | 12 | 17 | PD#         |
| 48M        | 13 | 16 | SEL100/66#  |
| 48_24/HFS# | 14 | 15 | VSS         |

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Preliminary

### Pin Description

| PIN No.       | Pin Name        | PWR  | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------|-----------------|------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2             | XIN             | VDD  | I   | On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal                                                                                                                                                                                                                                                                                                                                                         |
| 3             | XOUT            | VDD  | O   | O-chip reference oscillator output pin. Drives an external parallel resonant crystal (14.318 MHz) when an externally generated reference signal is used.                                                                                                                                                                                                                                                                                                                                                              |
| 19            | VDD             | -    | P   | 3.3 volt power supply for core logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 23, 24        | CPU(2,1)        | VDDC | O   | CPU Clock outputs. See frequency table page 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 17            | PD#             | -    | I   | Powers down device when LOW <sup>(1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 18            | CS#             | -    | I   | When signal is LOW, stops CPU clocks in low state. <sup>(1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 16            | SEL100/66#      | -    | I   | Frequency select input pins. See frequency select table 1 on page 1. NO INTERNAL PULLUP RESISTOR AT THIS INPUT.                                                                                                                                                                                                                                                                                                                                                                                                       |
| 25            | VDDC            | -    | P   | 2.5V power for CPU and Host clock outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 4             | PCI_F           | VDDP | O   | Free running PCI clock 3.3V. Does not stop when PS# is at a logic LOW level                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5,6,9, 10,11  | PCI(1:5)        | VDDP | O   | PCI output clocks. See frequency table of page 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 20            | PS#             | -    | I   | When signal is LOW, stops all PCI clocks in low state. <sup>(1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 8             | VDDP            | -    | P   | 3.3 Volt power supply pins for free running PCI clock output buffer.                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 13            | 48M             | VDDF | O   | Fixed 48 MHz clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 14            | 48-24MHZ / HFS# | VDDF | I/O | This is a Power up Bi-directional pin. During power up, this pin is an HFS# input. HFS# is a High Frequency Select line for programming the CPU/PCI output clock frequency, see table 1 page 1. For strapping resistor, see application note page 5. When the power reaches the rail, this pin becomes an SIO or USB clock output depending on the state of pin 27, SEL48#. If SEL48# is strapped high, then the frequency is 24MHz, SIO. If SEL48# is strapped low, then the frequency is 48MHz, USB. <sup>(1)</sup> |
| 26            | REF1 / SS#      | VDDR | I/O | At power up this pin determines if the device's spread spectrum modulation feature is enabled or disabled. After power up this pin becomes a reference clock output. A 0 (logic low) enables SSCG and a 1 (logic high) disables SSCG. <sup>(1)</sup>                                                                                                                                                                                                                                                                  |
| 27            | REF2 / SEL48#   | VDDR | I/O | At power up this pin determine the frequency of the clock at pin 14. If it is LOW, the clock will be 48 MHz, if HIGH the clock will be 24 MHz. After power up this pin will become a reference clock output. (Default high)                                                                                                                                                                                                                                                                                           |
| 12            | VDDF            | -    | P   | Power for fixed clock output buffer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1,7,15, 21,22 | VSS             | -    | P   | Ground pins for device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 28            | VDDR            | -    | P   | Power for Reference Oscillator output buffer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

Note:

1. Pins have internal pullup resistors that will guarantee to a logic 1 (high) level if no connection is made to the device's pin. Other pins do not contain this function and must be electrically connected to VDD or VSS by external circuitry to ensure a valid logic 1 or 0 is sensed.

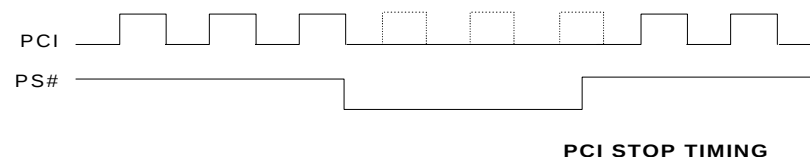
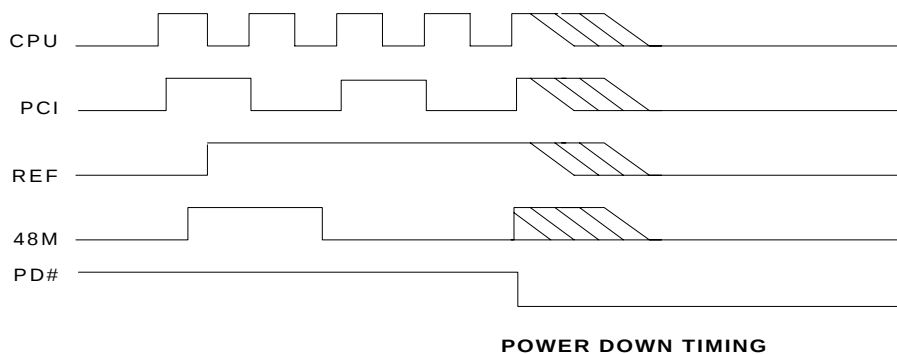
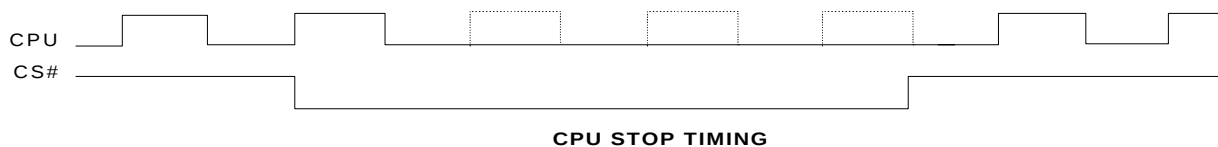
## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Power Management Functions

| PS# | CS# | PD# | CPU (1:2) | 48M, 48_24M | PCI (1:5) | PCI_F | REF (1:2) | VCOs |
|-----|-----|-----|-----------|-------------|-----------|-------|-----------|------|
| X   | X   | 0   | LOW       | LOW         | LOW       | LOW   | LOW       | OFF  |
| 1   | 0   | 1   | LOW       | ON          | ON        | ON    | ON        | ON   |
| 0   | 1   | 1   | ON        | ON          | LOW       | ON    | ON        | ON   |
| 0   | 0   | 1   | LOW       | ON          | LOW       | ON    | ON        | ON   |
| 1   | 1   | 1   | ON        | ON          | ON        | ON    | ON        | ON   |

CS# is the CPU stop control pin. It is used to turn off the CPU clocks for low power operation. CS# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU Clock) and must be internally synchronized to the external PCI\_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. CPU clock on latency need to be **2 or 3 CPU clocks** periods in time and CPU clock off latency needs to be **2 or 3 CPU clocks** periods in time.



## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Power Management Functions (Cont.)

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PD# is active low, all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power-up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. AS# and CS# are considered to be don't cares during the power down operations.

### Power Management Timing

| Signal | Signal State                    | Latency                                              |
|--------|---------------------------------|------------------------------------------------------|
|        |                                 | No. of rising edges of free running PCI CLOCK (PCIF) |
| CS#    | 0 (disabled)                    | 1                                                    |
|        | 1 (enabled)                     | 1                                                    |
| PD#    | 1 (cold start/normal operation) | 3 mS                                                 |
|        | 0 (power down)                  | 1                                                    |

**NOTES:** Clock on/off latency is defined in the number of rising edges of free running PCI CLOCK between the clock disable goes low/high to the first valid clock comes out of the device.

### Power on Bi-Directional Pins

#### Power Up Condition:

Pins 14, 26, and 27 are Power up bi-directional pins and are used for different features in this device (see Pin description, Page 2). During power-up, these pins are in input mode (see Fig 2, below), therefore, they are considered input select pins internal to the IC. After a settling time, the Selection data is latch into internal control registers and these pins become toggling clock outputs.

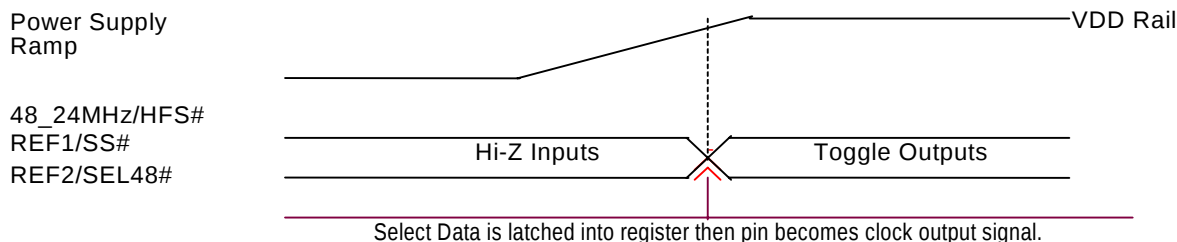


Fig. 2

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Strapping Resistor Options for pins with internal Pull-ups:

The power up bidirectional pins have a large value pull-up each (250K $\Omega$ ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 3mS settling time), then **it is recommended** to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig. 3A and Fig. 3B.

Fig. 3A represents an additional pull up resistor 50K $\Omega$  connected from the pin to the power line, which allows a faster pull to a high level.

If a selection "0" is desired, then a jumper is placed on JP1 to a 5K $\Omega$  resistor as implemented as shown in Fig.3A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 3B represent a single resistor 10K $\Omega$  connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

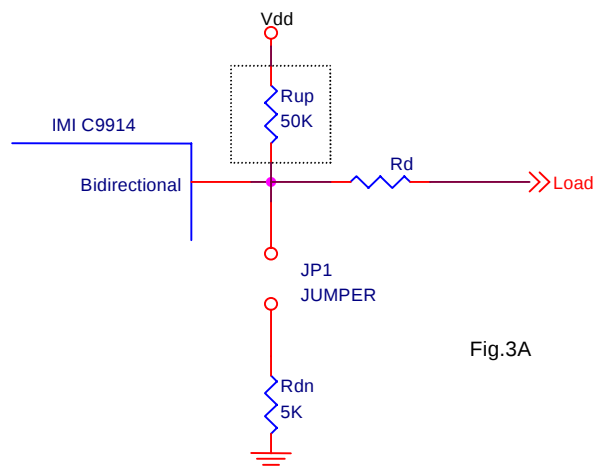


Fig.3A

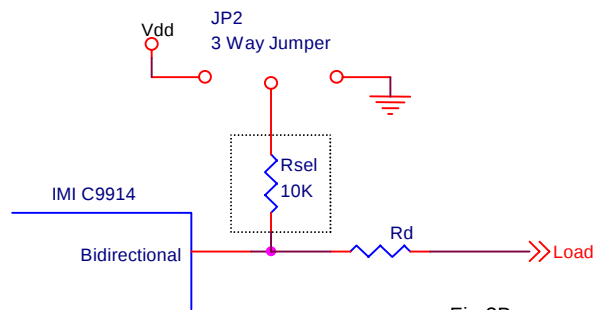
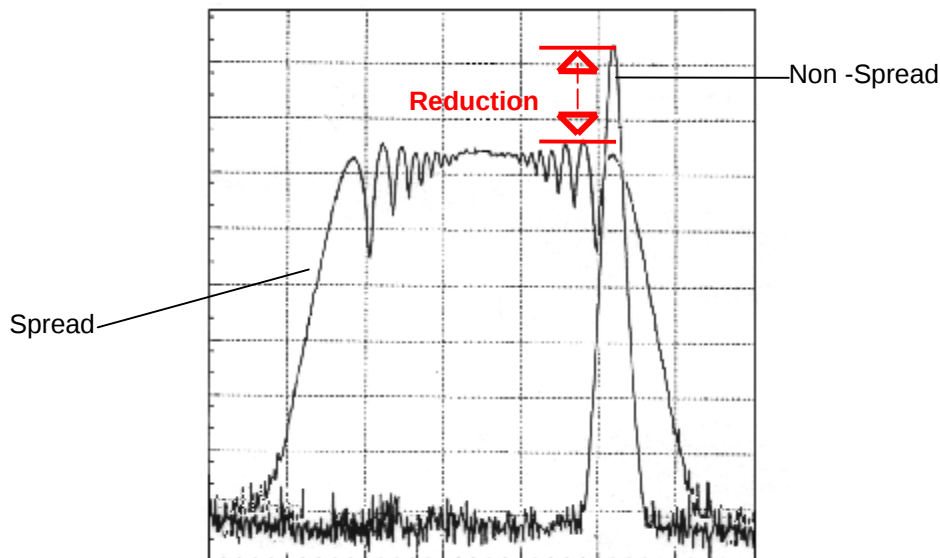


Fig.3B

### Spectrum Spread Clocking



Spectrum Analysis

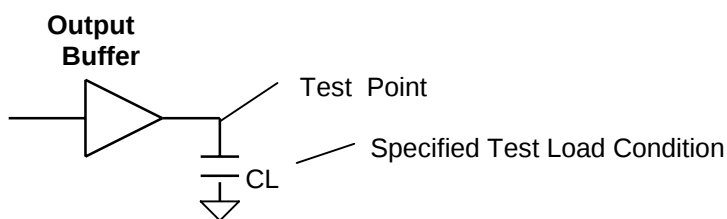
## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

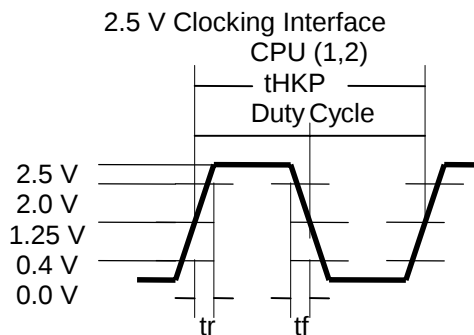
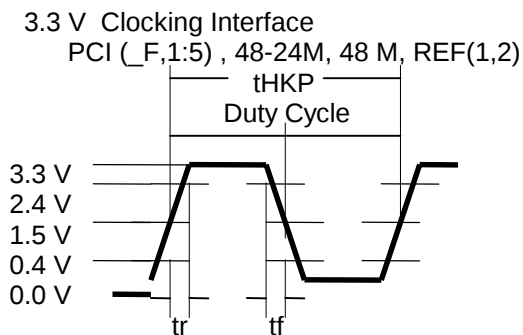
### Spectrum Spreading Selection Table

| Min (MHz) | Center (MHz) | Max (MHz) | CPU Frequency | % OF FREQUENCY SPREADING | MODE        |
|-----------|--------------|-----------|---------------|--------------------------|-------------|
| 99.3      | 99.65        | 100       | 100           | .7% (-.7% + 0%)          | Down Spread |
| 66.13     | 66.37        | 66.6      | 66            | .7% (-.7% + 0%)          | Down Spread |
| 132.4     | 132.87       | 133.33    | 133.3         | .7% (-.7% + 0%)          | Down Spread |
| 148.95    | 149.48       | 150       | 150           | .7% (-.7% + 0%)          | Down Spread |

### Test and Measurement Condition



### Clock Output Wave Form



## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Absolute Maximum Ratings

Maximum Input Voltage Relative to VSS:  $V_{SS} - 0.3V$   
Maximum Input Voltage Relative to VDD:  $V_{DD} + 0.3V$   
Storage Temperature:  $-65^{\circ}C$  to  $+150^{\circ}C$   
Operating Temperature:  $0^{\circ}C$  to  $+85^{\circ}C$   
Maximum ESD protection 2KV  
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

### DC Electrical Characteristics

| Characteristic                              | Symbol               | Min | Typ | Max | Units   | Conditions                                        |
|---------------------------------------------|----------------------|-----|-----|-----|---------|---------------------------------------------------|
| Input Low Voltage                           | VIL                  | -   | -   | 0.8 | Vdc     |                                                   |
| Input High Voltage                          | VIH                  | 2.0 | -   | -   | Vdc     |                                                   |
| Input Low Current                           | IIL                  |     |     | -66 | $\mu A$ |                                                   |
| Input High Current                          | IIH                  |     |     | 5   | $\mu A$ |                                                   |
| Output Low Voltage<br>IOL = 4mA             | VOL                  | -   | -   | 0.4 | Vdc     | All Outputs (see buffer spec)                     |
| Output High Voltage<br>IOH = 4mA            | VOH                  | 2.4 | -   | -   | Vdc     | All Outputs Using 3.3V Power<br>(see buffer spec) |
| Dynamic Supply Current<br>(2.5 Volt Supply) | I <sub>dd2.66</sub>  | -   | -   | 70  | mA      | CPU = 66.6M                                       |
| Dynamic Supply Current<br>(3.3 Volt Supply) | I <sub>dd3.100</sub> | -   | -   | 40  | mA      | CPU = 66.6M                                       |
| Dynamic Supply Current<br>(3.3 Volt Supply) | I <sub>dd3.100</sub> | -   | -   | 70  | mA      | CPU = 100M                                        |
| Power Down Mode                             | I <sub>2.5PD</sub>   | -   | -   | 50  | $\mu A$ | PD# at logic low level                            |
| Power Down Mode                             | I <sub>3.3PD</sub>   | -   | -   | 4.5 | mA      | PD# at logic low level                            |

$$V_{DD} = V_{DDF} = V_{DDP} = V_{DDR} = 3.3V \pm 5\%, V_{DDC} = 2.5V \pm 5\%, T_A = 0^{\circ}C \text{ to } +70^{\circ}C$$

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### AC Switching Characteristics

| Characteristic                                                                 | Symbol | Min | Typ | Max  | Units | Conditions                                                          |
|--------------------------------------------------------------------------------|--------|-----|-----|------|-------|---------------------------------------------------------------------|
| Output Duty Cycle                                                              | -      | 45  | 50  | 55   | %     | CPU= Measured at 1.25V<br>all others measured at 1.50V              |
| CPU to PCI Offset<br>(CPU leads)                                               | tOFF   | 1.5 | -   | 4    | ns    | CPU=20 pF load Measured at 1.25V<br>PCI=30 pF load Measure at 1.50V |
| ΔPeriod Adjacent Cycles                                                        | ΔP     | -   | -   | ±500 | pS    | PCI Only                                                            |
| <b>VDD = VDDF = VDDP = VDDR = 3.3V ±5%, VDDC = 2.5V ±5%, TA = 0°C to +70°C</b> |        |     |     |      |       |                                                                     |

### AC Skew Requirements

| Characteristic    | Bank Skew | Cycle to Cycle Jitters | VDD  | Skew, Jitters Measure Point |
|-------------------|-----------|------------------------|------|-----------------------------|
| CPU (20pF)        | 175pS     | 250pS                  | 2.5V | 1.25V                       |
| 48 MHz            | n/a       | 500pS                  | 3.3V | 1.5V                        |
| PCI, PCI_F (30pF) | 500pS     | 500pS                  | 3.3V | 1.5V                        |
| REF               | n/a       | 500pS                  | 3.3V | 1.5V                        |

### Buffer Characteristics

#### Buffer Characteristics for CPU Outputs

| Characteristic                                                                 | Symbol             | Min | Typ | Max | Units | Conditions     |
|--------------------------------------------------------------------------------|--------------------|-----|-----|-----|-------|----------------|
| Pull-Up Current Min                                                            | IOH <sub>min</sub> | -27 | -   |     | mA    | Vout = 1.0 V   |
| Pull-Up Current Max                                                            | IOH <sub>max</sub> |     |     | -27 | mA    | Vout = 2.375 V |
| Pull-Down Current Min                                                          | IOL <sub>min</sub> | 27  | -   | -   | mA    | Vout = 1.2 V   |
| Pull-Down Current Max                                                          | IOL <sub>max</sub> | -   | -   | 30  | mA    | Vout = 0.3 V   |
| Rise Time<br>Between 0.4 V and 2.0 V                                           | TR                 | 0.4 | -   | 1.6 | nS    | 20 pF Load     |
| Fall Time<br>Between 0.4 V and 2.0 V                                           | TF                 | 0.5 | -   | 1.6 | nS    | 20 pF Load     |
| <b>VDD = VDDF = VDDP = VDDR = 3.3V ±5%, VDDC = 2.5V ±5%, TA = 0°C to +70°C</b> |                    |     |     |     |       |                |

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Buffer Characteristics for 48M, 48-24M and REF Outputs

| Characteristic                       | Symbol      | Min | Typ | Max | Units | Conditions     |
|--------------------------------------|-------------|-----|-----|-----|-------|----------------|
| Pull-Up Current Min                  | $IOH_{min}$ | -29 | -   | -   | mA    | Vout = 1.0 V   |
| Pull-Up Current Max                  | $IOH_{max}$ | -   | -   | -63 | mA    | Vout = 3.135 V |
| Pull-Down Current Min                | $IOL_{min}$ | 20  | -   | -   | mA    | Vout = 1.95 V  |
| Pull-Down Current Max                | $IOL_{max}$ | -   | -   | 27  | mA    | Vout = 0.4 V   |
| Rise Time<br>Between 0.4 V and 2.4 V | TR          | 0.5 | -   | 2.0 | nS    | 20 pF Load     |
| Fall Time<br>Between 0.4 V and 2.4 V | TF          | 0.5 | -   | 2.0 | nS    | 20 pF Load     |

### DC Buffer Characteristics for PCI\_F, PCI (1:5)

| Characteristic                       | Symbol      | Min | Typ | Max  | Units | Conditions     |
|--------------------------------------|-------------|-----|-----|------|-------|----------------|
| Pull-Up Current Min                  | $IOH_{min}$ | -33 | -   | -    | mA    | Vout = 1.0 V   |
| Pull-Up Current Max                  | $IOH_{max}$ | -   | -   | -100 | mA    | Vout = 3.135 V |
| Pull-Down Current Min                | $IOL_{min}$ | 20  | -   | -    | mA    | Vout = 1.95 V  |
| Pull-Down Current Max                | $IOL_{max}$ | -   | -   | 38   | mA    | Vout = 0.4 V   |
| Rise Time<br>Between 0.4 V and 2.4 V | TR          | 0.5 | -   | 2.0  | nS    | 30 pF Load     |
| Fall Time<br>Between 0.4 V and 2.4 V | TF          | 0.5 | -   | 2.0  | nS    | 30 pF Load     |

**$VDDP = VDDR = 3.3V \pm 5\%$ ,  $VDDC = 2.5V \pm 5\%$ ,  $TA = 0^{\circ}C$  to  $+70^{\circ}C$**

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Suggested Oscillator Crystal Parameters

| Characteristic                    | Symbol            | Min   | Typ      | Max     | Units | Conditions                                    |
|-----------------------------------|-------------------|-------|----------|---------|-------|-----------------------------------------------|
| Frequency                         | F <sub>0</sub>    | 14.17 | 14.31818 | 14.46   | MHz   |                                               |
| Tolerance                         | T <sub>C</sub>    | -     | -        | +/-100  | PPM   | Note 1                                        |
| Frequency Stability               | T <sub>S</sub>    | -     | -        | +/- 100 | PPM   | Stability (T <sub>A</sub> -10 to +60C) Note 1 |
| Operating Mode                    | -                 | -     | -        | -       |       | Parallel Resonant, Note 1                     |
| Load Capacitance                  | C <sub>XTAL</sub> | -     | 20       | -       | pF    | The crystal's rated load. Note 1              |
| Effective Series Resistance (ESR) | R <sub>ESR</sub>  | -     | 40       | -       | Ohms  | Note 2                                        |

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

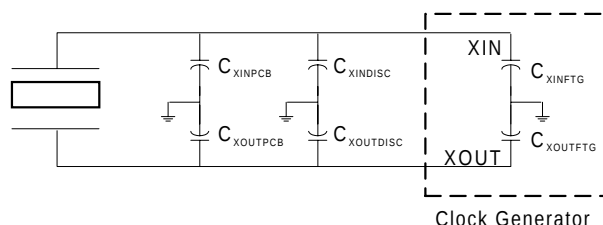
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C<sub>XTAL</sub>. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C<sub>FTG</sub>), any circuit trace capacitance (C<sub>PCB</sub>), and any onboard discrete load capacitance (C<sub>DISC</sub>).

The following formula and schematic illustrates the application of the loading specification of a crystal (C<sub>XTAL</sub>)for a design.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}$$

Where:

- C<sub>XTAL</sub> = the load rating of the crystal
- C<sub>XOUTFTG</sub> = the clock generators XIN pin effective device internal capacitance to ground
- C<sub>XOUTFTG</sub> = the clock generators XOUT pin effective device internal capacitance to ground
- C<sub>XINPCB</sub> = the effective capacitance to ground of the crystal to device PCB trace
- C<sub>XOUTPCB</sub> = the effective capacitance to ground of the crystal to device PCB trace
- C<sub>XINDISC</sub> = any discrete capacitance that is placed between the XIN pin and ground
- C<sub>XOUTDISC</sub> = any discrete capacitance that is placed between the XOUT pin and ground



As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C<sub>DISC</sub>) and each of the crystal to device PCB traces has a capacitance (C<sub>PCB</sub>) to ground of 4pF (typical value) would calculate as:

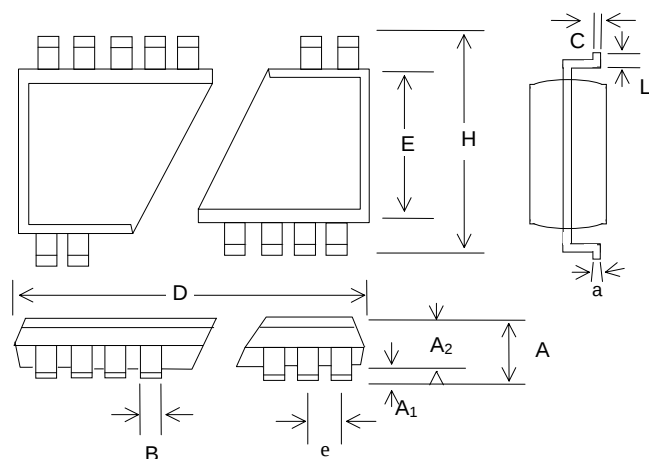
$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Package Drawings and Dimensions



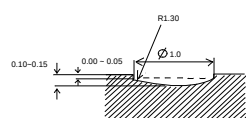
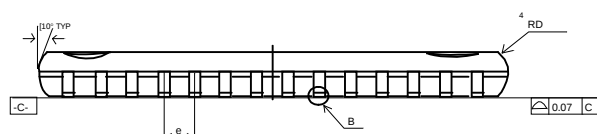
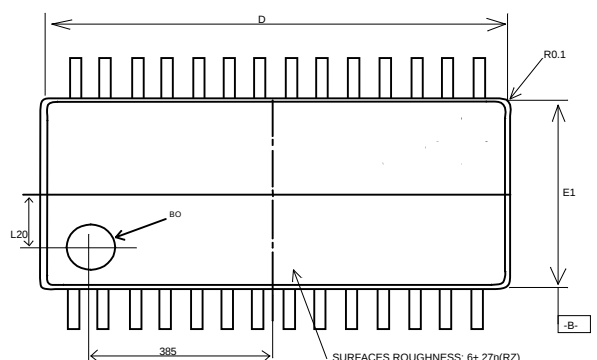
### 28 Pin SSOP Outline Dimensions

| SYMBOL         | INCHES    |       |       | MILLIMETERS |       |       |
|----------------|-----------|-------|-------|-------------|-------|-------|
|                | MIN       | NOM   | MAX   | MIN         | NOM   | MAX   |
| A              | 0.068     | 0.073 | 0.078 | 1.73        | 1.86  | 1.99  |
| A <sub>1</sub> | 0.002     | 0.005 | 0.008 | 0.05        | 0.13  | 0.21  |
| A <sub>2</sub> | 0.066     | 0.068 | 0.070 | 1.68        | 1.73  | 1.78  |
| B              | 0.010     | 0.012 | 0.015 | 0.25        | 0.30  | 0.38  |
| C              | 0.005     | 0.006 | 0.009 | 0.13        | 0.15  | 0.22  |
| D              | 0.397     | 0.402 | 0.407 | 10.07       | 10.20 | 10.33 |
| E              | 0.205     | 0.209 | 0.212 | 5.20        | 5.30  | 5.38  |
| e              | 0.025 BSC |       |       | 0.635 BSC   |       |       |
| H              | 0.301     | 0.307 | 0.311 | 7.65        | 7.80  | 7.90  |
| a              | 0°        | 4°    | 8°    | 0°          | 4°    | 8°    |
| L              | 0.022     | 0.030 | 0.037 | 0.55        | 0.75  | 0.95  |

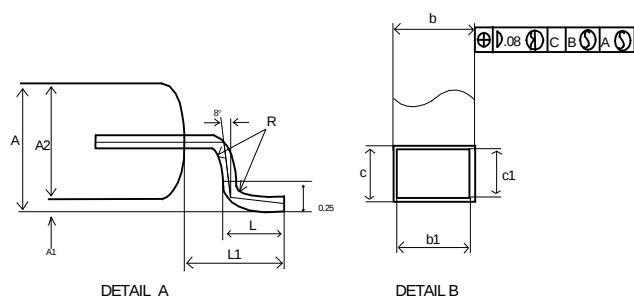
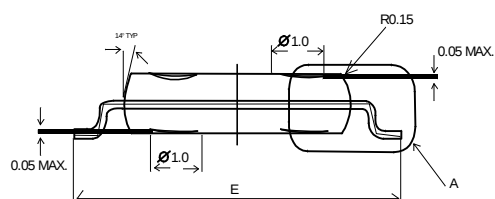
## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Package Drawings and Dimensions



SECTION V-V



### 28 Pin TSSOP Dimensions

| SYMBOL | INCHES    |       |       | MILLIMETERS |       |       |
|--------|-----------|-------|-------|-------------|-------|-------|
|        | MIN       | NOM   | MAX   | MIN         | NOM   | MAX   |
| A      | -         | -     | 0.047 | -           | -     | 1.20  |
| A1     | 0.002     | 0.004 | 0.006 | 0.05        | 0.10  | 0.15  |
| A2     | 0.037     | 0.039 | 0.041 | 0.95        | 1.00  | 1.05  |
| L      | 0.019     | 0.023 | 0.029 | 0.50        | 0.60  | 0.75  |
| L1     | 0.035     | 0.039 | 0.043 | 0.90        | 1.00  | 1.10  |
| b      | 0.007     | -     | 0.011 | 0.19        | -     | 0.30  |
| b1     | 0.007     | 0.008 | 0.010 | 0.19        | 0.22  | 0.25  |
| c      | 0.004     | -     | 0.007 | 0.105       | -     | 0.175 |
| c1     | 0.004     | 0.005 | 0.006 | 0.105       | 0.125 | 0.145 |
| θ      | 0°        | -     | 8°    | 0°          | -     | 8°    |
| e      | 0.026 BSC |       |       | 0.65 BSC    |       |       |
| D      | 0.378     | 0.382 | 0.386 | 9.6         | 9.7   | 9.8   |
| E      | 0.244     | 0.252 | 0.260 | 6.2         | 6.4   | 6.6   |
| E1     | 0.169     | 0.173 | 0.177 | 4.3         | 4.4   | 4.5   |
| R      | 0.035     | -     | -     | 0.9         | -     | -     |

## Clock Generator for 100MHz and 133.3MHz Mobile Applications

Preliminary

### Ordering Information

| Part Number | Package Type | Production Flow           |
|-------------|--------------|---------------------------|
| IMIC9914BY  | 28 PIN SSOP  | Commercial, 0°C to + 85°C |
| IMIC9914BT  | 28 PIN TSSOP | Commercial, 0°C to + 85°C |

**Note:** The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: IMI  
C9914  
Date Code, Lot #

IMIC9914BY

Package  
Y = SSOP  
T = TSSOP

Revision

IMI Device Number