Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  - — Military: 20/25/30/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Three-state outputs
- Available in:
  - — 28-pin DIP, SOIC, SOJ, and CERPACK
  - — 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When $\overline{CS_1}$ goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power stand by mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

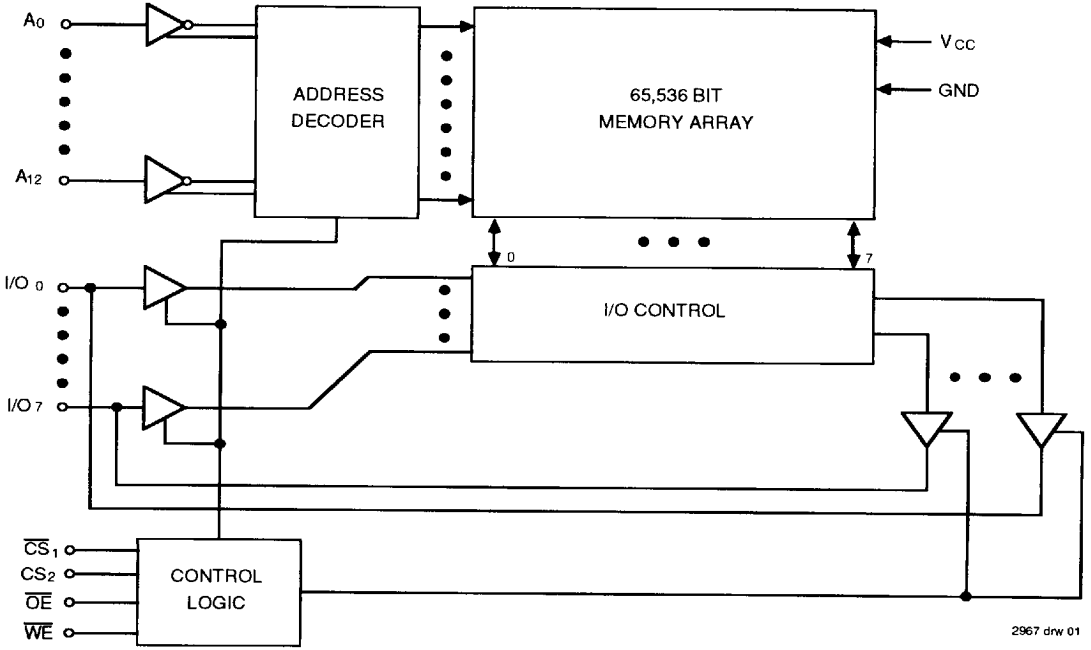
All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin LCC; and 28-pin CERPACK.

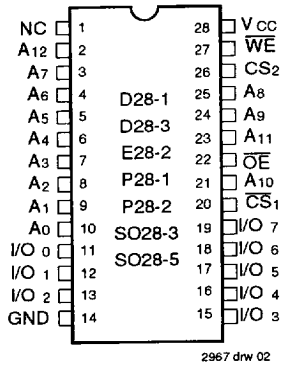
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

6

FUNCTIONAL BLOCK DIAGRAM

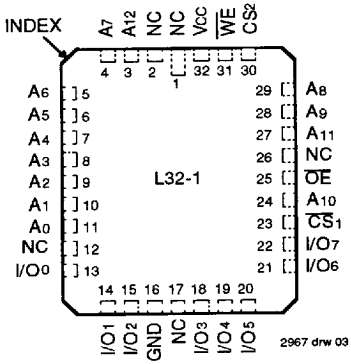


PIN CONFIGURATIONS



2967 drw 02

DIP/SOIC/SOJ/CERPACK
TOP VIEW



2967 drw 03

32-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A12	Address
I/O0–I/O7	Data Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2967 tbl 01

TRUTH TABLE(1,2,3)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Deselected – Standby (ISB)
X	X	L	X	High-Z	Deselected – Standby (ISB)
X	VHC	VHC or VLC	X	High-Z	Deselected –Standby (ISB1)
X	X	VLC	X	High-Z	Deselected –Standby (ISB1)
H	L	H	H	High-Z	Output Disabled
H	L	H	L	DataOUT	Read Data
L	L	H	X	DataIN	Write Data

2967 tbl 02

NOTES:
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2
2. H = VIH, L = VIL, X = don't care.
3. VLC = 0.2V, VHC = VCC - 0.2V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0 5 to +7.0	–0 5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1 0	1.0	W
IOUT	DC Output Current	50	50	mA

2967 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0 5V

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	VCC + 0 5	V
VIL	Input LOW Voltage	–0 5(1)	—	0.8	V

2967 tbl 06

NOTE:
1. VIL (min) = –1 5V for pulse width less than 10ns, once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1 This parameter is determined by device characterization, but is not production tested

2967 tbl 04

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15 Com'l.	7164S15 7164L15 Mil.	7164S20 7164L20 Com'l.	7164S20 7164L20 Mil.	7164S25 7164L25 Com'l.	7164S25 7164L25 Mil.	7164S30 7164L30 Com'l.	7164S30 7164L30 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max , f = 0[3]	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max , f = f_{MAX}[3]	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ V_{IH} or CS_2 ≤ V_{IL} V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max 1 $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC}, or 2 CS_2 ≤ V_{LC}	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0 2	1	0.2	1	0 2	1	

6

DC ELECTRICAL CHARACTERISTICS[1] (Continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S35 7164L35 Com'l.	7164S35 7164L35 Mil.	7164S45 7164L45 Com'l.	7164S45 7164L45 Mil.	7164S55 7164L55 Com'l.	7164S55 7164L55 Mil.	7164S70/85[2] 7164L70/85[2] Com'l.	7164S70/85[2] 7164L70/85[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max , f = 0[3]	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} Outputs Open, V_{CC} = Max , f = f_{MAX}[3]	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ V_{IH}, or CS_2 ≤ V_{IL} V_{CC} = Max , Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	5	—	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max 1 $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC}, or 2 CS_2 ≤ V_{LC}	S	15	20	—	20	—	20	—	20	mA
		L	0 2	1	—	1	—	1	—	1	

NOTES:
1 All values are maximum guaranteed values
2 Also available 100, 120, 150 and 200ns military devices
3 f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}), f = 0 means no address input lines are changing

2967 tbl 07

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7164S Min.	IDT7164S Max.	IDT7164L Min.	IDT7164L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max , V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min			0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min		—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min		2 4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL	—	10	15	200	300	µA
			COM'L	—	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time	1. $\overline{CS_1} \geq V_{HC}$ $CS_2 \geq V_{HC}$, or		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time	2 $CS_2 \leq V_{LC}$		t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2967 tbl 10

NOTES:
1 T_A = +25°C
2 t_{RC} = Read Cycle Time
3 This parameter is guaranteed by device characterization, but is not production tested

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1 5V
Output Reference Levels	1 5V
AC Test Load	See Figures 1 and 2

2967 tbl 08

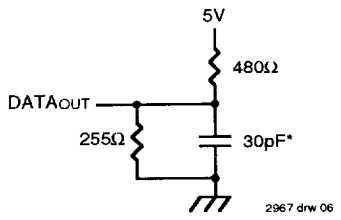


Figure 1. AC Test Load

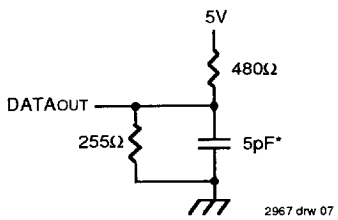


Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S15[1] 7164L15[1]		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	15	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	29	ns
tACS1[3]	Chip Select-1 Access Tim	—	15	—	20	—	25	—	30	ns
tACS2[3]	Chip Select-2 Access Time	—	20	—	25	—	30	—	35	ns
tCLZ1,2[4]	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
tOLZ[4]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tCHZ1,2[4]	Chip Select-1, 2 to Output in High-Z	—	8	—	9	—	13	—	13	ns
tOHZ[4]	Output Disable to Output in High-Z	—	7	—	8	—	10	—	12	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU[4]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD[4]	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	30	ns
Write Cycle										
tWC	Write Cycle Time	15	—	20	—	25	—	30	—	ns
tCW1, 2	Chip Select to End-of-Write	14	—	15	—	18	—	22	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	18	—	22	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	15	—	21	—	23	—	ns
tWR1	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
tWHZ[4]	Write Enable to Output in High-Z	—	6	—	8	—	10	—	12	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
tDH1	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
tOW[4]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

NOTES:
1 0° to +70°C temperature range only
2 –55°C to +125°C temperature range only Also available 100, 120, 150 and 200ns military devices.
3 Both chip selects must be active for the device to be selected
4 This parameter is guaranteed by device characterization, but is not production tested

2967 tbl 11

6

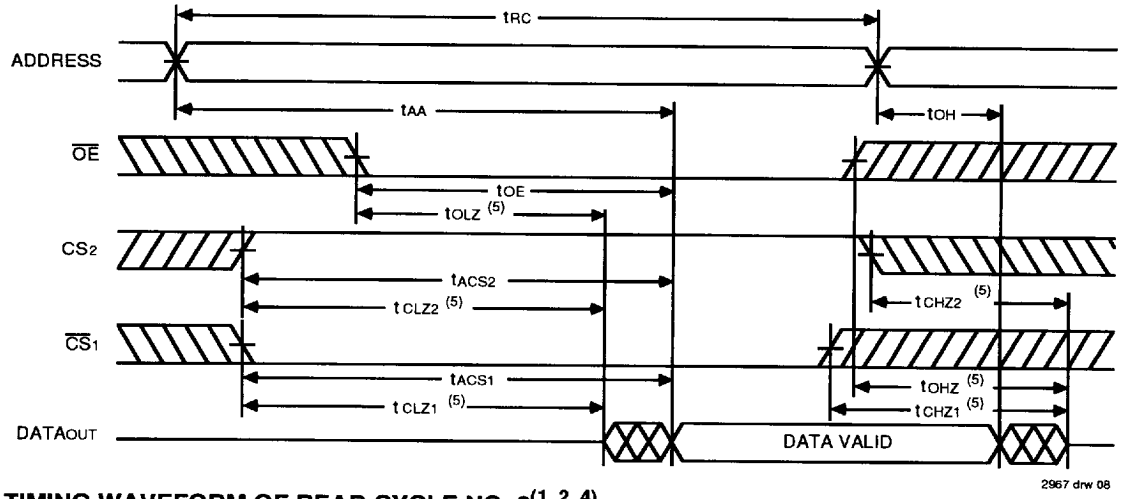
AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45[2] 7164L45[2]		7164S55[2] 7164L55[2]		7164S70[2]/85[2] 7164L70[2]/85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS1}[3]	Chip Select-1 Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS2}[3]	Chip Select-2 Access Time	—	40	—	45	—	55	—	70/85	ns
$t_{CLZ1,2}$[4]	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
t_{OLZ}[4]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$[4]	Chip Select-1, 2 to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t_{OHZ}[4]	Output Disable to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[4]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[4]	Chip Deselect to Power Down Time	—	35	—	45	—	55	—	70/85	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}[4]	Write Enable to Output in High-Z	—	14	—	18	—	25	—	30/35	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}[4]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

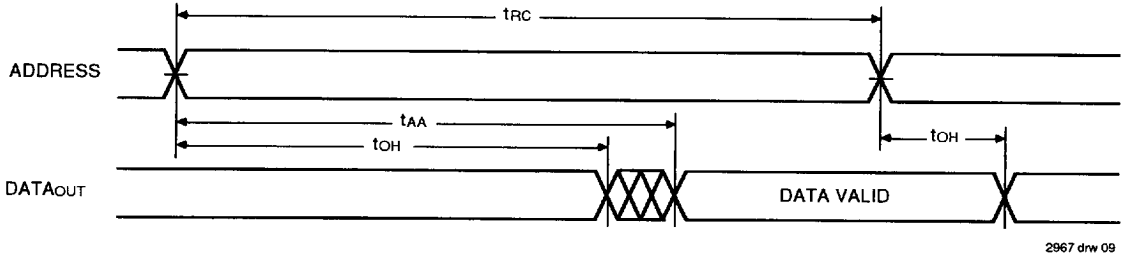
2967 tbl 11

NOTES:
1 0° to +70°C temperature range only
2 −55°C to +125°C temperature range only. Also available 100, 120, 150, and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4 This parameter is guaranteed by device characterization, but is not production tested

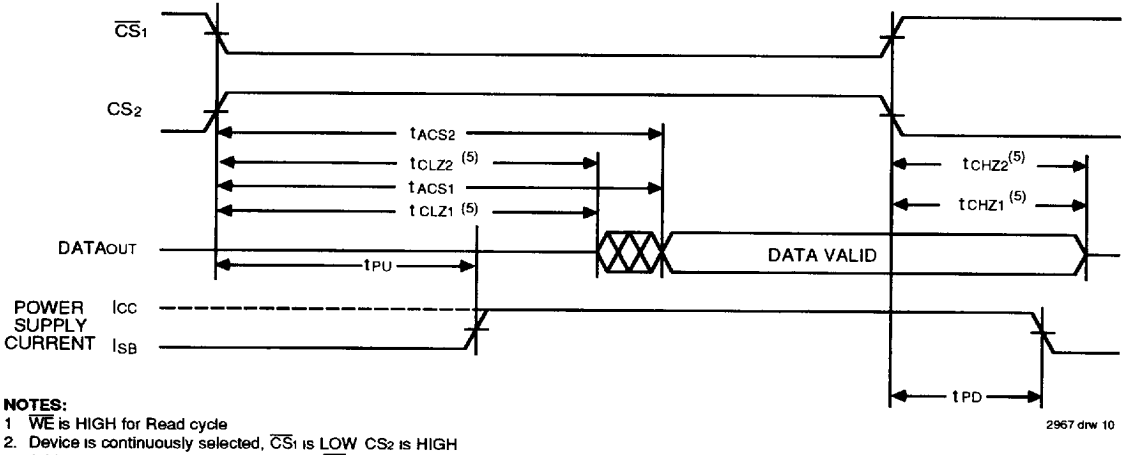
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

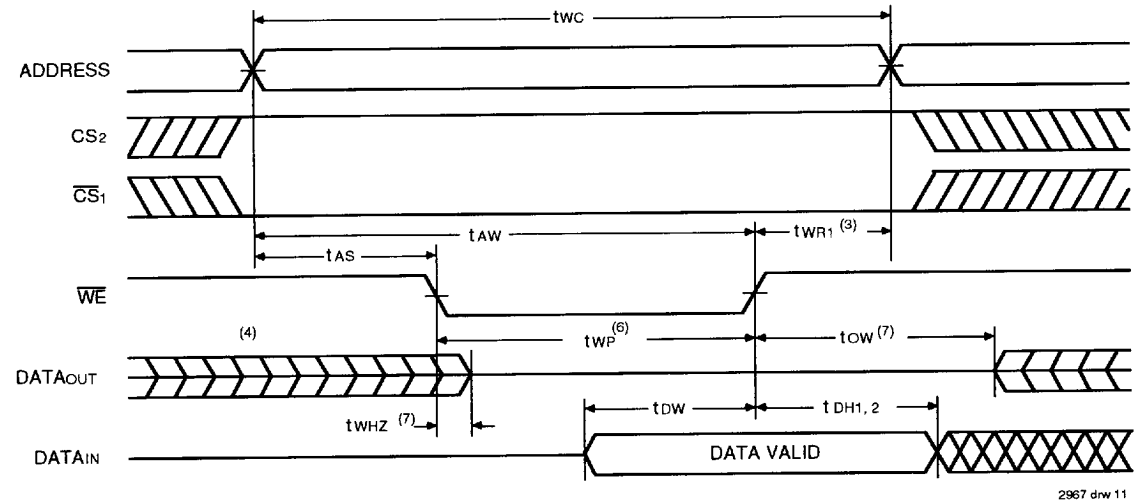


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

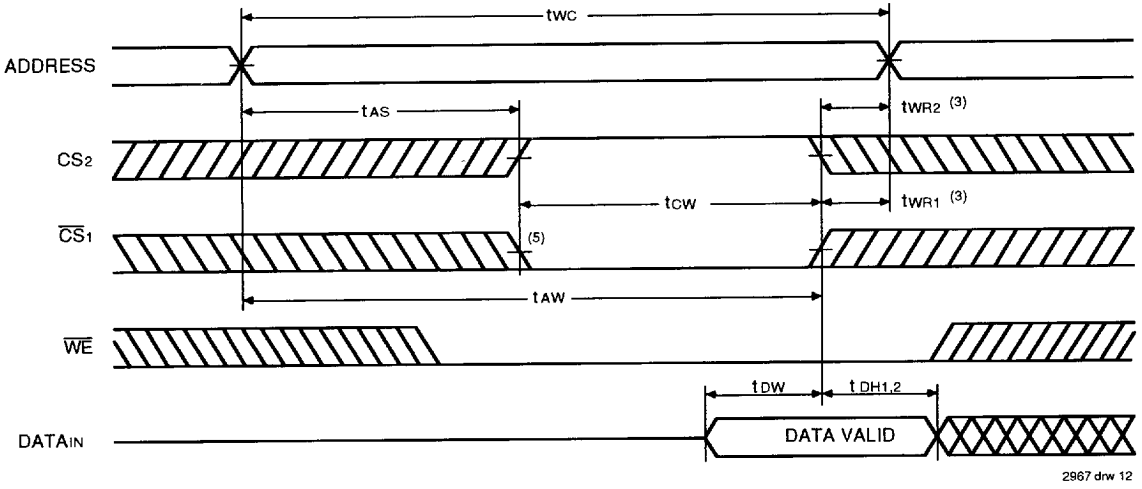


NOTES:
1. $\overline{WE}$ is HIGH for Read cycle
2. Device is continuously selected, $\overline{CS_1}$ is LOW CS_2 is HIGH
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH
4. $\overline{OE}$ is LOW
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 6)

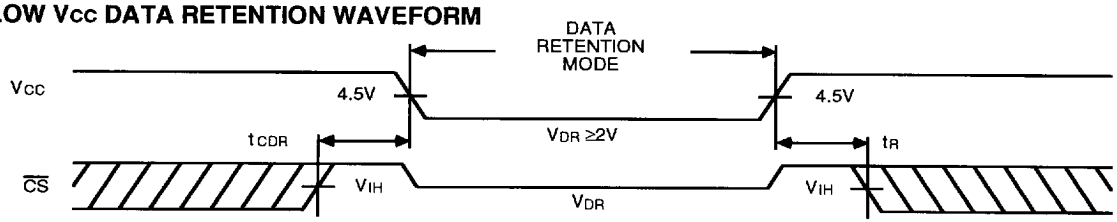


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2)



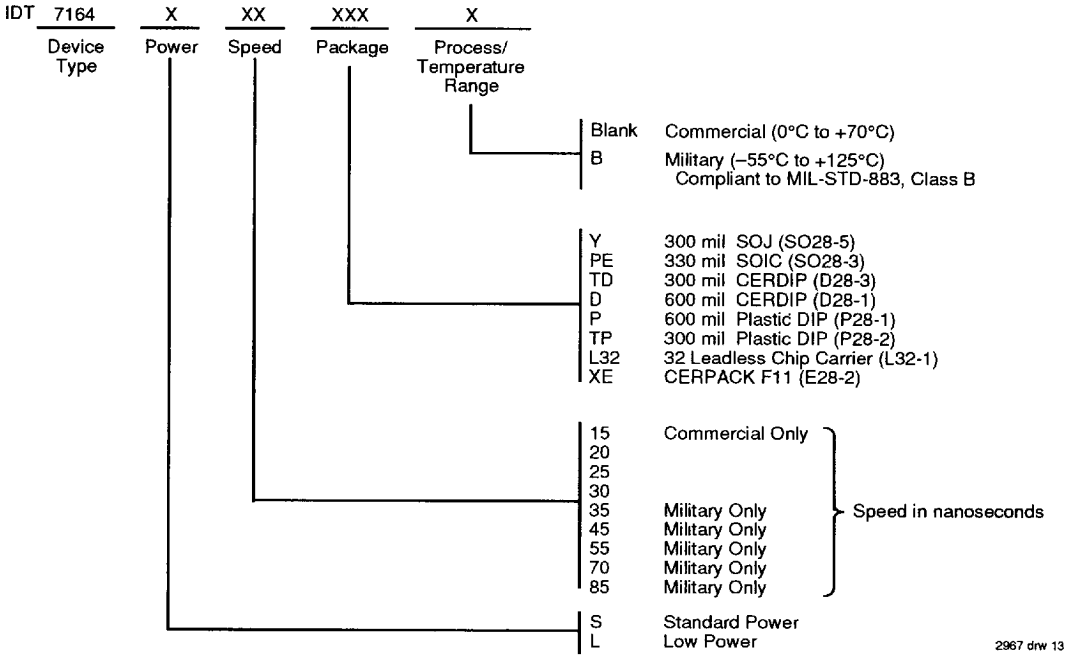
NOTES:
1 $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2 A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a HIGH CS_2.
3. $t_{WR1, 2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle
4 During this period, I/O pins are in the output state so that the input signals must not be applied
5. If the $\overline{CS_1}$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state
6 $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}
7 Transition is measured ±200mV from steady state

LOW Vcc DATA RETENTION WAVEFORM



2967 drw 05

ORDERING INFORMATION



2967 drw 13

6