HARRIS SEMICONDUCTOR

CA3242

Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load

April 1994

Features

- Driven Outputs Capable of Switching 600mA Load Currents Without Spurious Changes In Output State
- Inputs Compatible with TTL or 5V CMOS Logic
- Suitable for Resistive or Inductive Loads
- Output Overload Protection
- Power-Frame Construction for Good Heat Dissipation

Applications

- Relays
- Solenoids
- AC and DC Motors
- Heaters
- Incandescent Displays
- Vacuum Fluorescent Displays

Description

The CA3242 quad-gated inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Output overload protection is provided when the load current (approximately 1.2A) causes the output V_{CE}(sat) to rise above 1.3V. A built-in time delay, nominally 25µs, is provided during output turn-on as output drops from V_{DD} to V_{SAT}. That output will be shut down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

Steering diodes in the outputs in conjunction with external zener diodes protect the IC against voltage transients due to switching inductive loads.

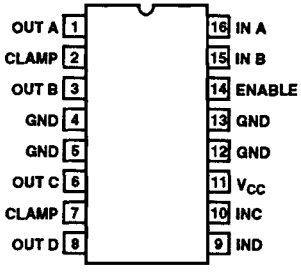
To allow for maximum heat transfer from the chip, the four center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 60°C/W (typical). This coefficient can be lowered by suitable design of the PC board to which the CA3242 is soldered.

Ordering Information

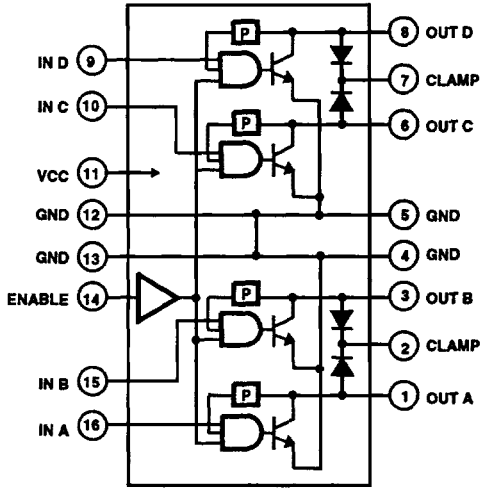
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3242E	-40°C to +105°C	16 Lead Plastic DIP

Pinout

CA3242 (PDIP)
TOP VIEW



Block Diagram



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

File Number 1561.2

Absolute Maximum Ratings (Note 1)

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} ..... $50V_{DC}$
Output Sustaining Voltage, V_{CESUS} ..... $35V_{DC}$
Output Current, I_O ..... $1A_{DC}$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JL}
Plastic DIP	60°C/W	-
Plastic DIP (to Pins 4, 5, 12, 13)	-	12°C/W

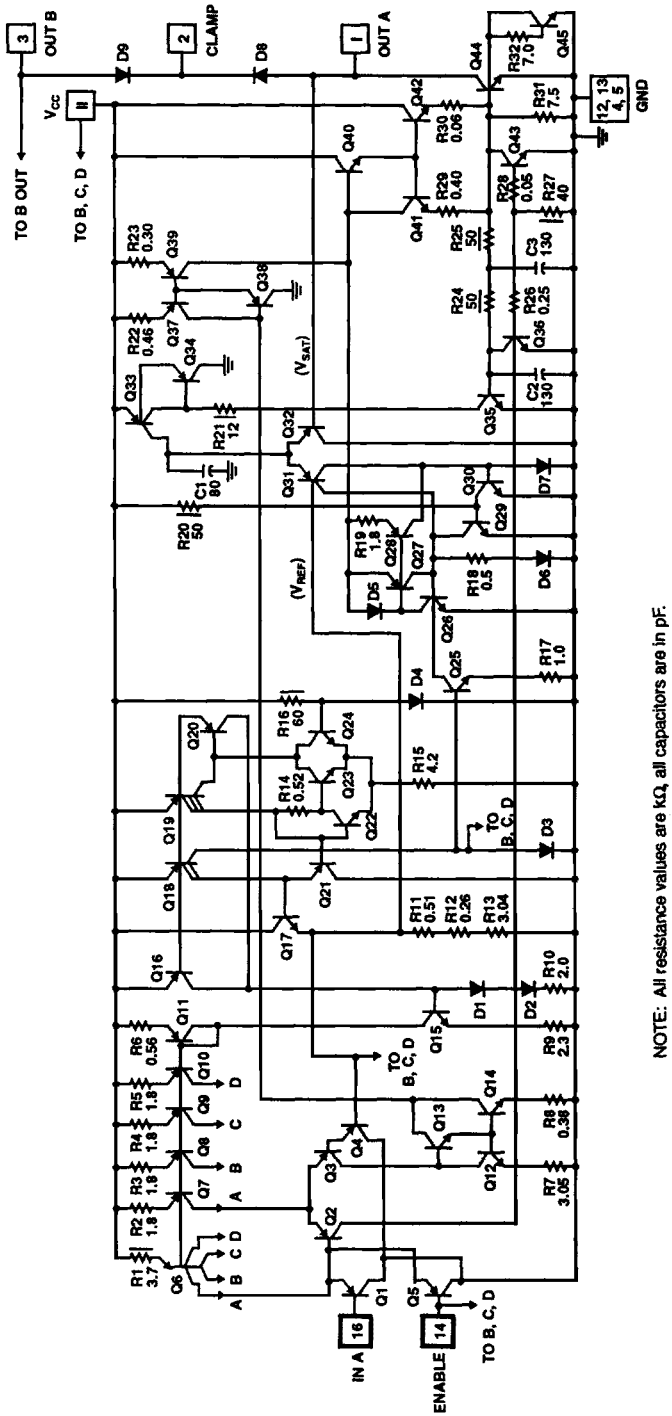
Power Dissipation, P_D
Up to 60°C 1.5W
Above 60°C ..... Derate Linearly at 16.6mW/°C
Up to 90°C w/Heat Sink (PC Board) 1.5W
Above 90°C w/Heat Sink (PC Board).. Derate Linearly at 25mW/°C
Ambient Temperature Range
Operating ..... -40°C to +105°C
Storage ..... -55°C to +150°C
Maximum Junction Temperature, T_J ..... +150°C
Lead Temperature (During Soldering)
At distance 1/16 inch ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +105°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{IN} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 100mA, V_{IN} = 0.8V	30	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA, V_{IN} = 2.4V	-	0.35	V
		I_C = 400mA, V_{IN} = 2.4V	-	0.6	V
		I_C = 600mA, V_{IN} = 2.4V	-	0.8	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	±10	µA
Input High Voltage	V_{IH}	I_C = 600mA	2	-	V
Input High Current	I_{IH}	I_C = 700mA, V_{IN} = 4.5V	-	10	µA
Supply Current ON	$I_{CC(ON)}$	I_C = 700mA, V_{CC} = V_{IH} = 5.5V	-	80	mA
Supply Current OFF	$I_{CC(OFF)}$		-	5	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 1A	-	1.8	V
		I_F = 1.5A	-	2.5	V
Turn-On Delay	t_{PHL}		-	20	µs
Turn-Off Delay	t_{PLH}		-	30	µs

NOTE:
1. T_A = +25°C, Unless Otherwise Specified



NOTE: All resistance values are KΩ, all capacitors are in pF.

FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3242 (SWITCH SECTION A)

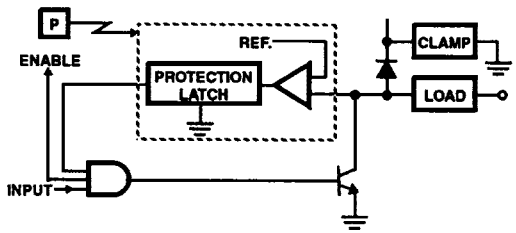


FIGURE 2. LOGIC DIAGRAM FOR EACH OUTPUT

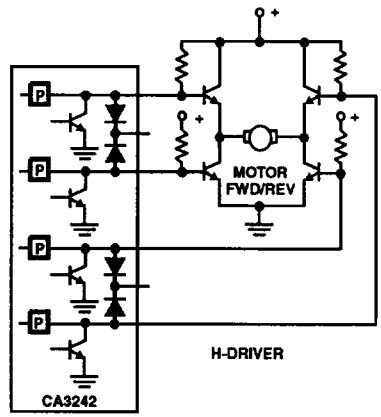


FIGURE 3. TYPICAL APPLICATIONS FOR THE CA3242 QUAD

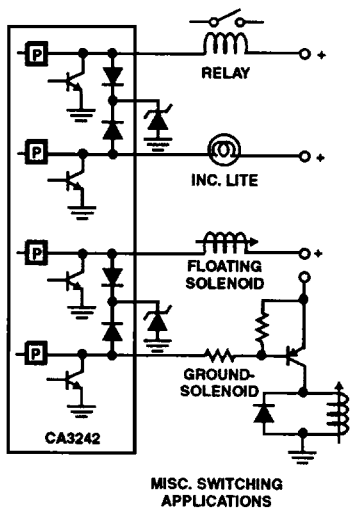


FIGURE 4. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

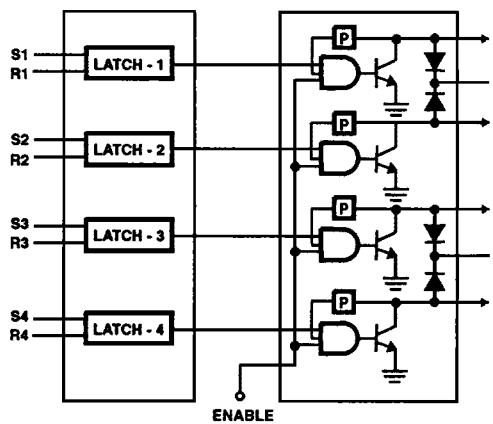


FIGURE 5. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER