

Features

- High speed access times
Com'l: 10, 12, 15, 17, 20 and 25 ns
Ind'l: 15, 17, 20, and 25 ns
- Low power operation
 - PDM41024SA
Active: 400 mW (typ.)
Standby: 150 mW (typ.)
 - PDM41024LA
Active: 350 mW (typ.)
Standby: 100 mW (typ.)
- Single +5V (±10%) power supply
- Packages
 - CerDIP (400 mil) - D
 - Plastic SOJ (300 mil) - TSO
 - Plastic SOJ (400 mil) - SO
 - Plastic DIP (400 mil) - P
 - Plastic TSOP - T

Description

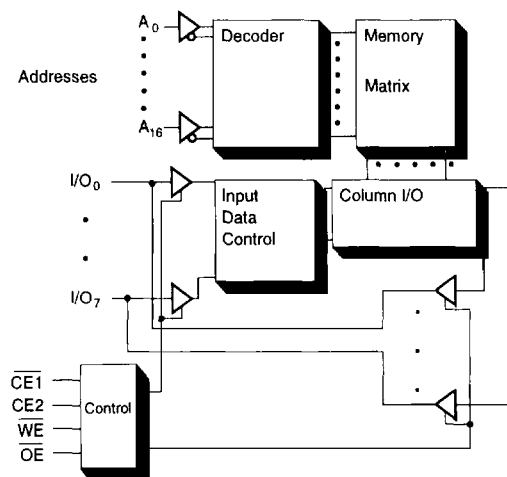
The PDM41024 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE1}$) inputs are both LOW and $\overline{CE2}$ is HIGH. Reading is accomplished when $\overline{WE}$ and $\overline{CE2}$ remain HIGH and $\overline{CE1}$ and $\overline{OE}$ are both LOW.

The PDM41024 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41024 comes in two versions, the standard power version PDM41024SA and a low power version the PDM41024LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41024 is available in a 32-pin 400 mil cer-DIP, 400 mil Plastic DIP, plastic TSOP, 300 mil and 400 mil SOJ.

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Functional Block Diagram



Pin Configuration

DIP, SOJ, TSOP			
NC	1	32	Vcc
A16	2	31	A15
A14	3	30	$\overline{CE2}$
A12	4	29	$\overline{WE}$
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
GND	16	17	I/O3

Truth Table⁽¹⁾

OE	WE	CE1	CE2	VO	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D _{OUT}	Read
X	L	L	H	D _{IN}	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Ind.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Military	Ambient Temperature	-55	25	125	°C
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	-0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±10%)

Symbol	Parameter	Test Conditions		PDM41024SA		PDM41024LA		Unit
				Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = MAX., V _{IN} = GND to V _{CC}	Com'l/ Ind.	-5	5	-2	5	μA
I _{LO}	Output Leakage Current	V _{CC} = MAX., CE = V _{IH} , V _{OUT} = GND to V _{CC}	Com'l/ Ind.	-5	5	-2	5	μA
V _{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V _{IL}	Input Low Voltage			-0.5 ⁽¹⁾	0.8	-0.5 ⁽¹⁾	0.8	V
V _{OL}	Output Low Voltage	I _{OL} = 8 mA, V _{CC} = Min. I _{OL} = 10 mA, V _{CC} = Min.		—	0.4 0.5	—	0.4 0.5	V V
V _{OH}	Output High Voltage	I _{OH} = -4 mA, V _{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = -3.0V for pulse width less than 20 ns

Power Supply Characteristics

Symbol	Parameter	Power	-10	-12	-15		-17		-20		-25		Unit
			Com'l.	Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I _{CC}	Operating Current CE = V _{IL} , and CE2 = V _{IH} f = f _{MAX} = 1/f _{RC} V _{CC} = Max. I _{OUT} = 0 mA	SA	250	230	185	195	165	175	155	165	145	155	mA
		LA	230	210	165	175	155	165	140	150	135	145	
I _{SB}	Standby Current CE1 = V _{IH} or CE2 = V _{IL} f = f _{MAX} = 1/f _{RC} V _{CC} = Max.	SA	80	70	55	55	50	50	45	45	40	40	mA
		LA	75	65	50	50	45	45	40	40	35	35	
I _{SB1}	Full Standby Current CE1 ≥ V _{HC} or CE2 ≤ V _{LC} f = 0 V _{CC} = Max., V _{IN} ≥ V _{CC} - 0.2V or ≤ 0.2V	SA	20	20	10	15	10	15	10	15	10	15	mA
		LA	10	10	5	10	5	10	5	10	5	10	

SHADED AREA = PRELIMINARY DATA

NOTES: All values are maximum guaranteed values.

V_{LC} ≤ 0.2V, V_{HC} ≥ V_{CC} - 0.2V

Capacitance⁽¹⁾ (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C _{IN}	Input Capacitance	8	pF
C _{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

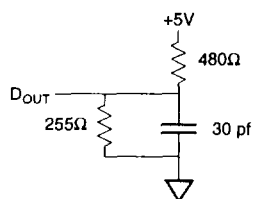


Figure 1. Output Load Equivalent

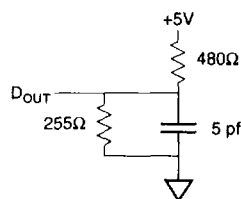


Figure 2. Output Load Equivalent
(for t_{LZCE} , t_{HZWE} , t_{LZWE} , t_{HZWE} , t_{LZOE} , t_{HZOE})

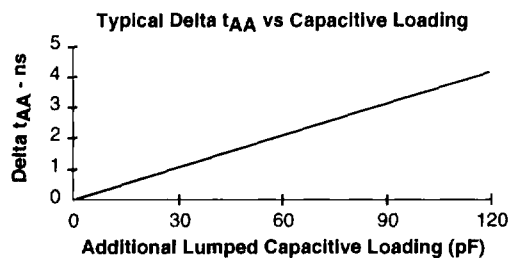
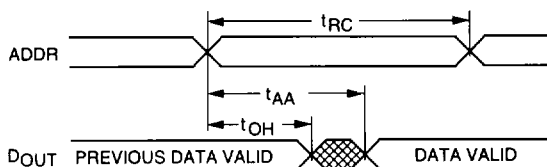
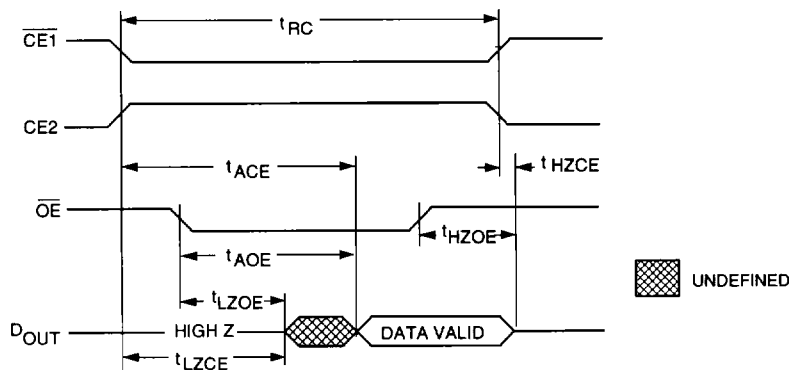


Figure 4.

Read Cycle No. 1^(4, 5)



Read Cycle No. 2^(2, 4, 6)



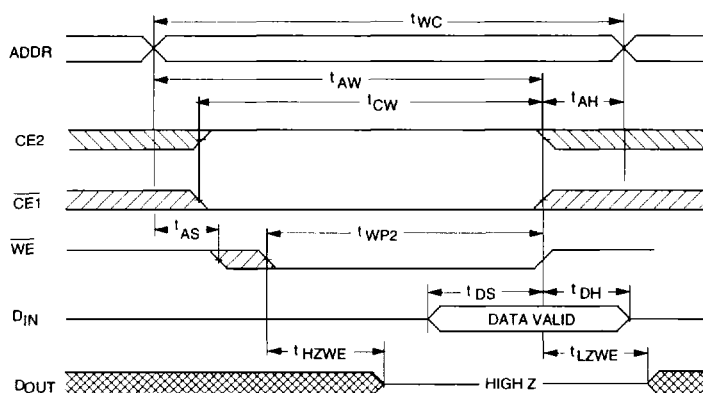
AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

Description		-10 ⁽⁷⁾		-12 ⁽⁷⁾		-15		-17		-20		-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ Cycle	Sym													
READ cycle time	t_{RC}	10		12		15		17		20		25		ns
Address access time	t_{AA}		10		12		15		17		20		25	ns
Chip enable access time	t_{ACE}		10		12		15		17		20		25	ns
Output hold from address change	t_{OH}	5		3		3		3		3		3		ns
Chip enable to output in low Z ^(1, 3)	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z ^(1, 2, 3)	t_{HCZE}		8		6		7		7		8		10	ns
Chip enable to power up time ⁽³⁾	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time ⁽³⁾	t_{PD}		10		12		15		17		20		25	ns
Output enable access time	t_{AOE}		6		6		6		6		6		8	ns
Output Enable to output in low Z ^(1, 3)	t_{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z ^(1, 3)	t_{HZOE}		6		6		6		6		6		8	ns

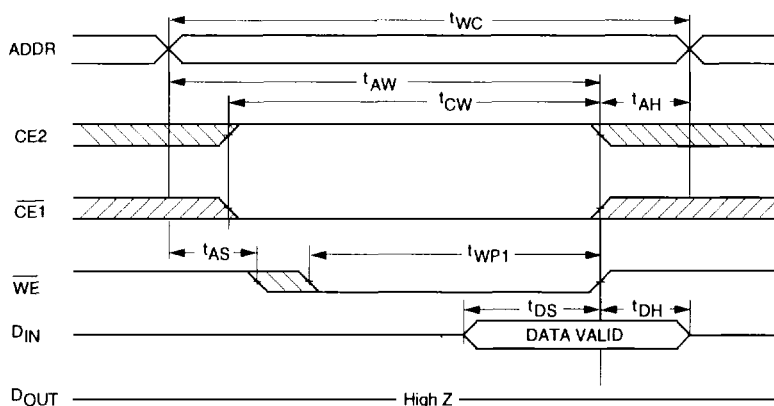
SHADED AREA = PRELIMINARY DATA.

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)

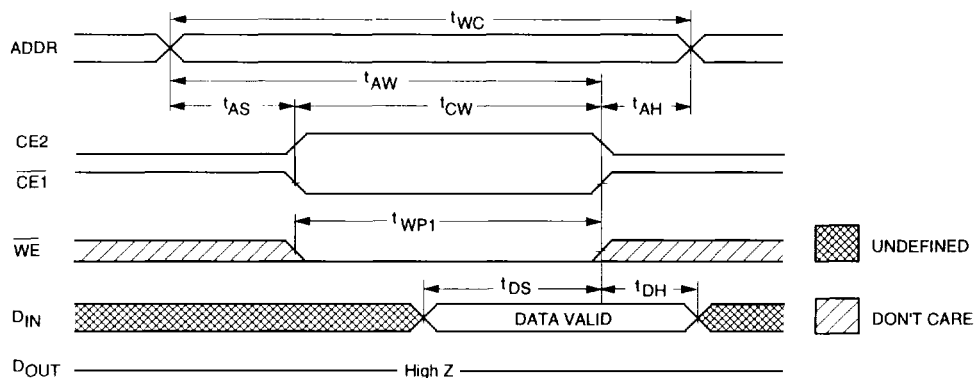


Write Cycle No. 2 (Write Enable Controlled)



NOTE: Output Enable ($\overline{OE}$) is inactive (high)

Write Cycle No. 3 (Chip Enable Controlled)



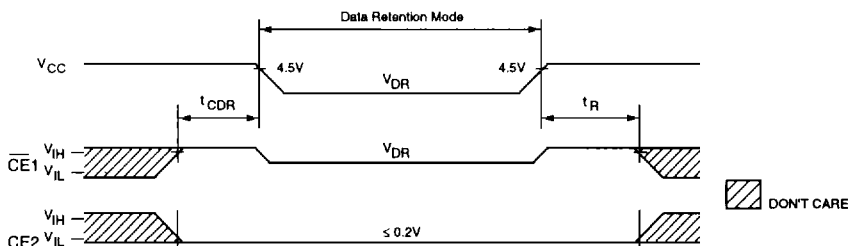
NOTE: Output Enable ($\overline{OE}$) is inactive (high)

AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-10 ⁽⁷⁾	-12 ⁽⁷⁾	-15	-17	-20	-25	
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE Cycle time	t _{WC}	10		12		15		ns
Chip enable access time	t _{CW}	10		10		11		ns
Address Valid to end of write	t _{AW}	10		10		11		ns
Address setup time	t _{AS}	0		0		0		ns
Address hold from end of write	t _{AH}	0		0		0		ns
Write pulse width	t _{WP1}	9		10		11		ns
Write pulse width	t _{WP2}	10		11		12		ns
Data setup time	t _{DS}	7		7		8		ns
Data hold time	t _{DH}	0		0		0		ns
Write disable to output in low Z ^(1, 3)	t _{LZ}	0		0		0		ns
Write enable to output in high ^(1, 3)	t _{HZWE}	7		7		7		ns

SHADED AREA = PRELIMINARY DATA

Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{CC} for Retention Data		2	—	—	V
I _{CCDR}	Data Retention Current	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ V _{SS} + 0.2V V _{IN} ≥ V _{CC} - 0.2V or ≤ 0.2V	V _{CC} = 2V — V _{CC} = 3V —	—	500 750	μA
t _{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

- The parameter is tested with CL = 5 pF as shown in Fig. #2. Transition is measured ±200 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
- This parameter is sampled.
- WE is high for a READ cycle.
- The device is continuously selected. All the Chip Enables are held in their active state.
- The address is valid prior to or coincident with the latest occurring Chip Enable.
- V_{CC} = 5V ±5%.

Ordering Information

PDM	XXXXX	A	XX	A	A	Process / Temperature Range	
						Device Type	Power
						Blank	Commercial (0° to +70°C)
						I	Industrial (–40°C to +85°C)
						P	400 mil Plastic DIP
						D	400 mil CerDIP
						TSO	300 mil Plastic SOJ
						SO	400 mil Plastic SOJ
						T	Plastic TSOP
						10	Commercial Only
						12	
						15	
						17	
						20	
						25	
						SA	Standard Power
						LA	Low Power
						41024	1 Meg (128K x 8) Static RAM

Chip	Package Type
PDM41024	32-pin Plastic SOJ 300 Mil
	32-pin Plastic SOJ 400 Mil
	32-pin Plastic TSOP
	32-pin Plastic DIP 400 Mil
	32-pin CerDIP 400 Mil