

M5M5258CP,J-15,-20,-25,-35, -20L,-25L,-35L

262144-BIT (65536-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5258C is a family of 65536 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicongate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5258CP,J-15.....15ns(max)
M5M5258CP,J-20,-20L.....20ns(max)
M5M5258CP,J-25,-25L.....25ns(max)
M5M5258CP,J-35,-35L.....35ns(max)
- Low power dissipation
Active.....300mW(typ)
Stand by(-15,-20,-25,-35).....5mW(typ)
Stand by(-20L,-25L,-35L).....50μW(typ)
- Power down by $\bar{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\bar{S}$) input
- All address inputs are changeable with each other

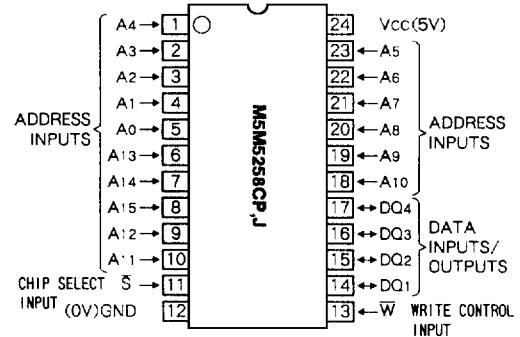
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\bar{S}$ low and $\bar{W}$ low

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y(P)
24P0J(J)

if the address signals are stable, the data is available at the DQ terminal.

When $\bar{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state useful for OR-ties

M5M5258CP, J-15, -20, -25, -35, -20L, -25L, -35L**262144-BIT (65536-WORD BY 4-BIT) CMOS STATIC RAM****MODE SELECTION**

S	W	Mode	Data I/O	I _{cc}
H	X	Non selection	High-impedance	Stand by
L	L	Write	D _{in}	Active
L	H	Read	D _{out}	Active

H: V_{IH} L: V_{IL} X: V_{IL} or V_{IH}**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 3.5* ~ 7	V
V _I	Input voltage		- 3.5* ~ 7	V
V _O	Output voltage		- 3.5* ~ 7	V
P _D	Maximum power dissipation		1	W
T _{opr}	Operating temperature		0~70	°C
T _{stg(bias)}	Storage temperature(bias)		- 10~85	°C
T _{stg}	Storage temperature		- 65~150	°C

* Pulse width ≤ 10ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70 °C, V_{CC} = 5V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3	V
V _{IL}	Low-level input voltage		- 0.5*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0~V _{CC}			2	μA
I _{OZ}	Off-state output current	V _{I(S)} = V _{IH} , V _O = 0~V _{CC}			10	μA
I _{CC1}	Supply current from V _{CC}	V _{I(S)} = V _{IL} Output open	AC (15ns cycle)		130	mA
			AC (20, 25, 35ns cycle)		120	
			DC		60 75	
I _{CC2}	Stand by current	V _{I(S)} = V _{IH}	AC (15ns cycle)		50	mA
			AC (20, 25, 35ns cycle)		40	
			Other V _I ≥ V _{IH} or ≤ V _{IL}		30	
I _{CC3}	Stand by current	V _{I(S)} = V _{CC} - 0.2V Other V _I ≤ 0.2V or V _I ≥ V _{CC} - 0.2V	-15, -20, -25, -35		1 10	mA
			20L, -25L, -35L		10 100	

Note 1. Current flow into an IC is positive, out is negative.

* - 3.0V in case of AC(Pulse width ≤ 10ns)

CAPACITANCE

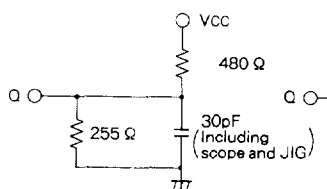
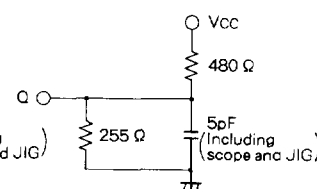
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _i	Input capacitance	V _I = GND, V _I = 25mVrms, f = 1MHz			5	pF
C _o	Output capacitance	V _O = GND, V _O = 25mVrms, f = 1MHz			7	pF

* C_i, C_o are periodically sampled and are not 100 % tested.**AC ELECTRICAL CHARACTERISTICS** (T_a = 0~70 °C, V_{CC} = 5V ± 10 %, unless otherwise noted)**(1) MEASUREMENT CONDITIONS**Input pulse levels V_{IH} = 3V, V_{IL} = 0V

Input rise and fall time 3ns

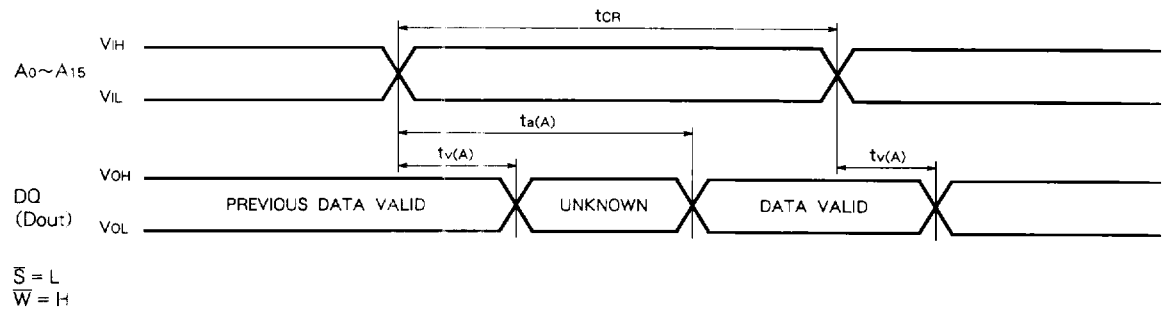
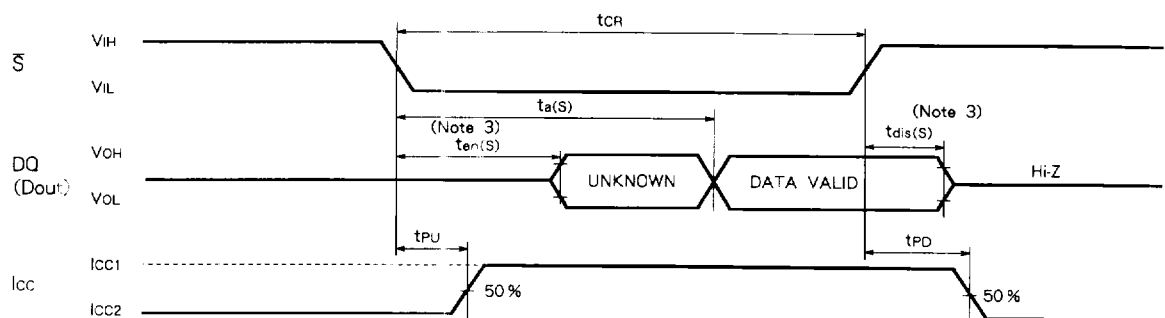
Input timing reference levels V_{IH} = V_{IL} = 1.5VOutput timing reference levels V_{OH} = V_{OL} = 1.5V

Output loads Fig.1, Fig.2

**Fig.1 Output load****Fig.2 Output load for t_{OH}, t_{OL}**

M5M5258CP, J-15, -20, -25, -35, -20L, -25L, -35L**262144-BIT (65536-WORD BY 4-BIT) CMOS STATIC RAM****(2) READ CYCLE**

Symbol	Parameter	Limits								Unit
		M5M5258C-15		M5M5258C-20,-20L		M5M5258C-25,-25L		M5M5258C-35,-35L		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	15		20		25		35		ns
ta(A)	Address access time		15		20		25		35	ns
ta(S)	Chip select access time		15		20		25		35	ns
tv(A)	Data valid time after address	3		3		5		5		ns
ten(S)	Output enable time after $\overline{S}$ low	3		3		5		5		ns
tdis(S)	Output disable time after $\overline{S}$ high	0	7	0	8	0	10	0	10	ns
tPU	Power-up time after chip selection	0		0		0		0		ns
tPD	Power-down time after chip deselection		15		20		25		35	ns

(3) TIMING DIAGRAMS FOR READ CYCLE**Read cycle 1****Read cycle 2 (Note 2)**Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure2.

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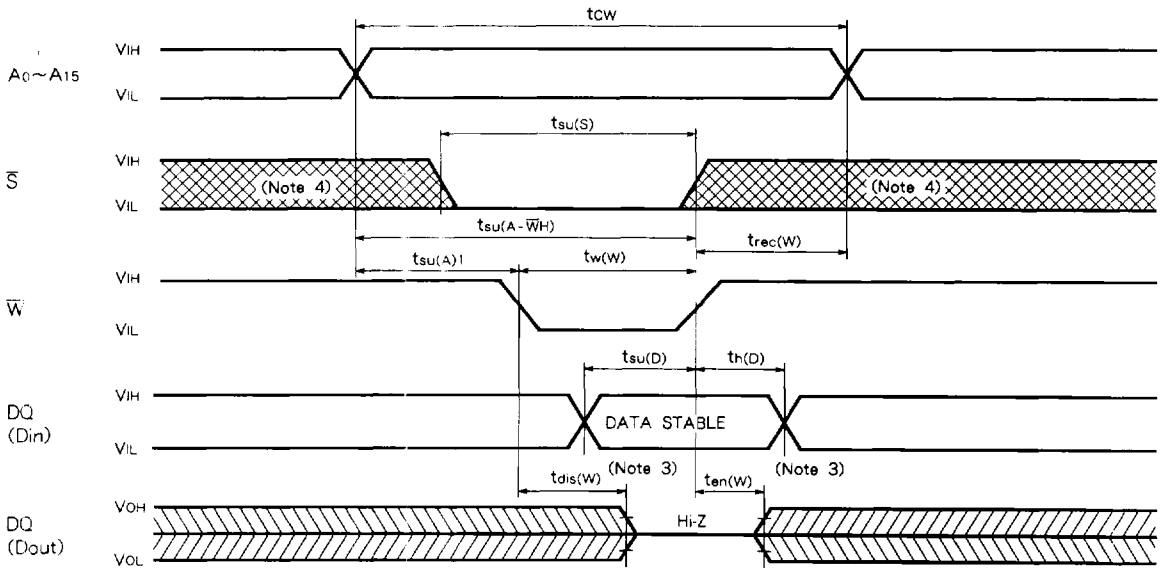
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(4) WRITE CYCLE

Symbol	Parameter	Limits								Unit
		M5M5258C-15		M5M5258C-20,-20L		M5M5258C-25,-25L		M5M5258C-35,-35L		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _W	Write cycle time	15		20		25		35		ns
t _{su} (S)	Chip select setup time	12		15		20		30		ns
t _{su} (A)1	Address setup time 1(W CONTROL)	0		0		0		0		ns
t _{su} (A)2	Address setup time 2(S CONTROL)	0		0		0		0		ns
t _w (W)	Write pulse width	12		15		20		25		ns
t _{rec} (W)	Write recovery time	0		0		0		0		ns
t _{su} (D)	Data setup time	7		8		10		15		ns
t _h (D)	Data hold time	0		0		0		0		ns
t _{dis} (W)	Output disable time after $\overline{\text{W}}$ low	0	7	0	8	0	10	0	10	ns
t _{en} (W)	Output enable time after $\overline{\text{W}}$ high	0		0		0		0		ns
t _{su} (A- $\overline{\text{W}}$ H)	Address to $\overline{\text{W}}$ high	12		15		20		30		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

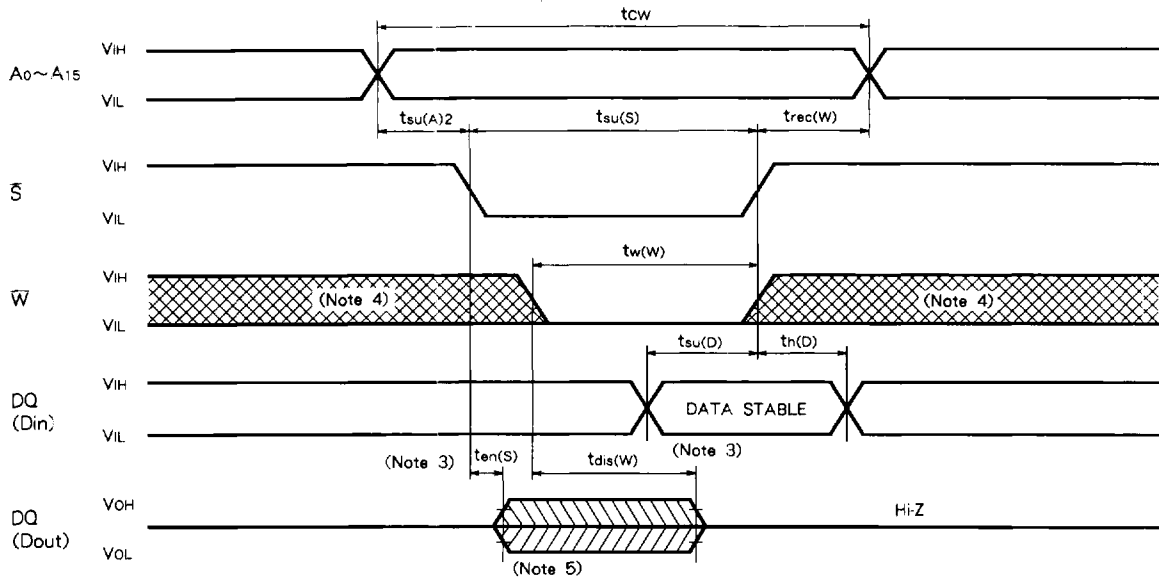
Write cycle 1 ($\overline{\text{W}}$ control mode)



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Write cycle 2 ($\bar{S}$ control mode)



Note 4. Hatching indicates the state is don't care.

5. When the falling edge of $\bar{W}$ is simultaneous or prior to the falling edge of $\bar{S}$, the output is maintained in the high impedance.

6. t_{en} , t_{dis} are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{cc}(PD)$	Power down supply voltage		2			V
$V_i(\bar{S})$	Chip select input voltage		$V_{cc} - 0.2$			V
$t_{su}(PD)$	Power down setup time	$V_i(\bar{S}) \geq V_{cc} - 0.2V$ $V_i \geq V_{cc} - 0.2V$ or $0V \leq V_i \leq 0.2V$	0			ns
$t_{rec}(PD)$	Power down recovery time		-20L	20		ns
			-25L	25		
			-35L	35		
$I_{cc}(PD)$	Power down supply current	$V_{cc} = 3.0V$ $V_{cc} = 5.5V$			50 100	μA

Note 6. This is only M5M5258CP, J-20L, -25L, -35L.

TIMING WAVEFORM FOR POWER DOWN

