=Preliminary= AK8810

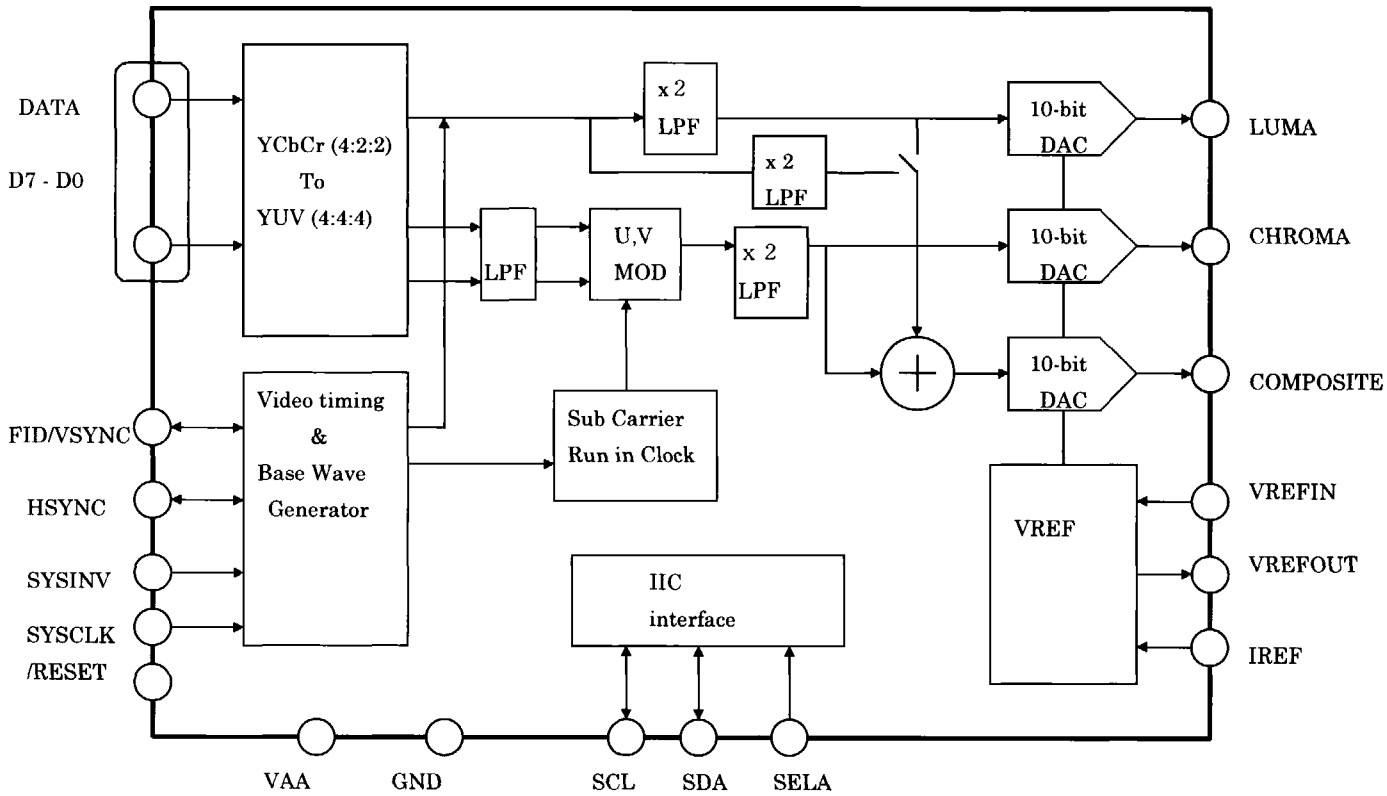
NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

The AK8810 Digital video encoder is suitable for a digital broadcasting STB and a DVD player. ITU-R601 Format Y,Cb,Cr is converted into NTSC or PAL composite signal simultaneously with Y/C (S-video). AK8810 supports Macrovision Copy Protection Rev.7 , Closed Captioning line 21 and 284 and NTSC line 20 Video Blanking ID. These functions are controlled by high speed I2C interface.

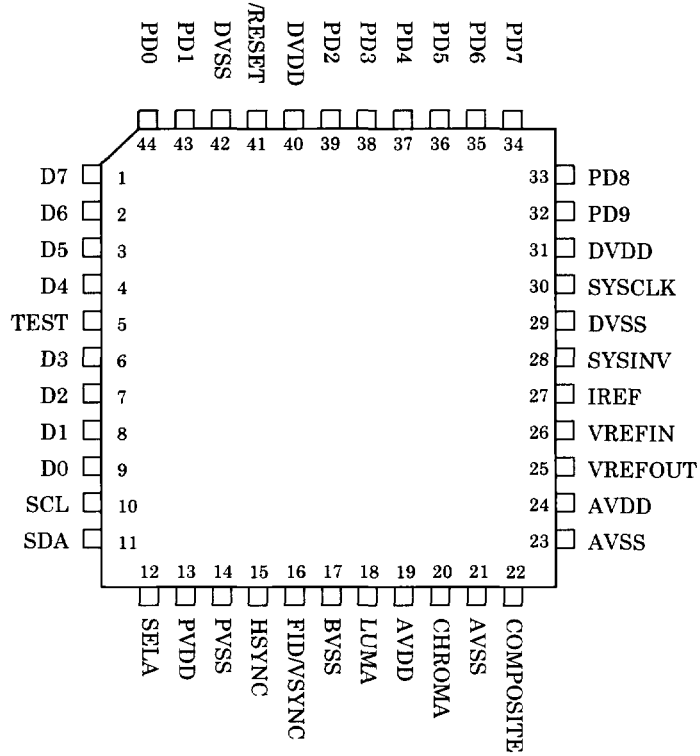
FEATURES

- ○ NTSC-M, PAL-B,D,G,H,I,M,N encoding.
- ○ Simultaneous Composite and S-Video output
- ○ CCIR-656 4:2:2 8-bit Parallel Input
- ○ EAV, SAV Decoding
- ○ Master/Slave Operation
- ○ Digital Field Sync I/O
- ○ Digital Vertical/Horizontal Sync I/O
- ○ Y filtering x2 oversampling
- ○ C filtering x4 oversampling & sin(x)/x correction
- ○ Single 27MHz Clock (The polarity could be inverted by SYSINV pin)
- ○ Triple 10 bit DAC
- ○ IIC Interface (400kHz)
- ○ Closed caption encoding (NTSC: line 21,284-SMPTE PAL: line 21,334-CCIR)
- ○ Supports Macrovision Copy Protection Rev. 7.01 *
- ○ VBID, CGMS (EIAJ CPR-1024:)
- ○ On-chip Color Bar generator
- ○ 5V only, CMOS Monolithic
- ○ 44pin LQFP Package


DATA
D7 - D0
YCbCr (4:2:2)
To
YUV (4:4:4)
x 2
LPF
x 2
LPF
LPF
U,V
MOD
x 2
LPF
10-bit
DAC
10-bit
DAC
10-bit
DAC
LUMA
CHROMA
COMPOSITE
FID/VSYNC
HSYNC
SYSINV
SYSCLK
/RESET
Video timing
&
Base Wave
Generator
Sub Carrier
Run in Clock
IIC
interface
VREF
VREFIN
VREFOUT
IREF
VAA
GND
SCL
SDA
SELA

PIN LAYOUT

44pin LQFP



PIN/FUNCTION

Num	Pin Name	I/O	Description
1,2,3 4,6,7 8,9	D7 - D0	I	27MHz 8-Bit 4:2:2 multiplexed Y,Cb,Cr Data Input. For CCIR-656 format, AK8810 decodes EAV and SAV. For non-CCIR-656 format (without EAV/SAV) AK8810 operates in Master or Slave mode.
30	SYSCLK	I	27MHz Clock Input. The polarity could be inverted by SYSINV.
28	SYSINV	I	Connects to "L "or "H". "L" sets normal clock polarity.
41	/RESET	I	After this pin becomes "L", AK8810 starts the internal initializing sequence at the rising edge of the first SYSCLK. (Width of the reset pulse" L" needs minimum 10 SYSCLK cycles.) After initializing sequence, AK8810 is set NTSC, CCIR-656 decoding mode. All DAC Off.
16	FID /VSYNC	I/O	Show the relation between MPEG stream and data. Either of FID or VSYNC selected by the register. For CCIR-656 decode mode, this pin is output . For non-CCIR-656 decode mode, I/O depends on the device operation mode.(Master or Slave) FID shows that "L" is odd field and "H" is even field.
15	HSYNC	I/O	Show the relation between MPEG stream and data. For CCIR-656 decode mode, this pin is output. For non-CCIR-656 decode mode, I/O depends on the device operation mode.(Master or Slave)
10	SCL	I	Serial interface clock
11	SDA	I/O	Serial interface data
12	SELA	I	Connects to "L "or "H". The slave address is following "L":40H "H":42H
25	VREFOUT	O	Output of the Internal Vref. Terminate with 0.1F or more capacitance.
26	VREFIN	I	Input of the Reference Voltage
27	IREF	O	The currents flow this pin adjusts the full-scale output current of the DAC.
22	COMPOSITE	O	Output of Composite Video signal
20	CHROMA	O	Output of the C signal
18	LUMA	O	Output of Luminance Signal
5	TEST	I	Test pin. Grounded for normal operation
19,24	AVDD	P	Analog +5V
31,40 13	DVDD PVDD	P	Digital +5V
21,23 17	AVSS, BVSS	G	Analog Ground
29,42 14	DVSS, PVSS	G	Digital Ground
*	PD[9:0]	NC	Test pin. Left Open

Test pin * 32,33,34,35,36,37,38,39,43,44

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (VDD) DVDD, PVDD, AVDD	-0.3	6.5	V
Input Pin Voltage (Vin)	-0.3	VDD+0.3	V
Input Pin Current (Iin)	-	±10	mA
Analog Reference Current (IREF)	-	0.35	mA
Analog Output Current	-	11	mA
Power Dissipation		1000	mW
Storage Temperature	-40	125	°C

(Note) When all grand pins (DVSS,PVSS,BVSS,AVSS) are set to 0V.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Supply Voltage (VDD)	4.5	5	5.5	V
Operating Temperature	-10		70	°C

DC Characteristic

<Power Supply:5V Temperature:25°C>

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital Input High Voltage	VIH	2.2			V	Note1)
Digital Input Low Voltage	VIL			0.7	V	Note1)
Digital Input leak Current	IL			±10	μA	Note1)
Digital Output High Voltage	VOH	2.8			V	IOH=-1mA Note2)
Digital Output Low Voltage	VOL			0.4	V	IOL=2mA Note2)
IIC Input High Voltage I2C(SDA,SCL)	VIH	0.7VDD			V	
IIC Input Low Voltage I2C(SDA,SCL)	VIL			0.3VDD	V	
IIC(SDA) Output Voltage	VOL			0.4	V	IOL=4.5mA

Note1) D[9:0],FID/VSYNC, HSYNC, SYSCLK, RESET pin

Note2) FID/VSYNC, HSYNC pin

Analog Characteristic And Dissipation Current

<Power Supply:5V Temperature:25°C>

Parameter	Min	Typ	Max	Units	Conditions
Resolution		10		bit	
Integral linearity error		±0.3	±1.5	LSB	
Differential linearity error		±0.2	±1	LSB	
Output Full Scale Voltage	1.21	1.28	1.38	V	Note1)
Output offset Voltage			5.0	mV	Note2)
DAC Unbalance		±1	±5	%	Note3)
DAC Isolation		50		dB	1MHz Full Scale
Internal Reference Voltage	1.17	1.235	1.33	V	
Internal Reference Drift		50		ppm/°C	
Digital Current		60		mA	
DAC Current		25		mA	Note4)
DAC Current		10		μA	Note5)
Total Current		85	125	mA	Note6)

Note 1) Under the condition of output load 220Ω, IREF pin with 6.8kΩ, using internal reference. The output full-scale current Iout is calculated as Full scale output voltage (typ. 1.28V) /220Ω=typ. 5.8mA.

Note 2) DAC output when feeding code of 0(Decimal).

Note 3) Deviation between the DAC output when feeding 1V generating code of 800(Decimal).

Note 4) All DACs are operating.

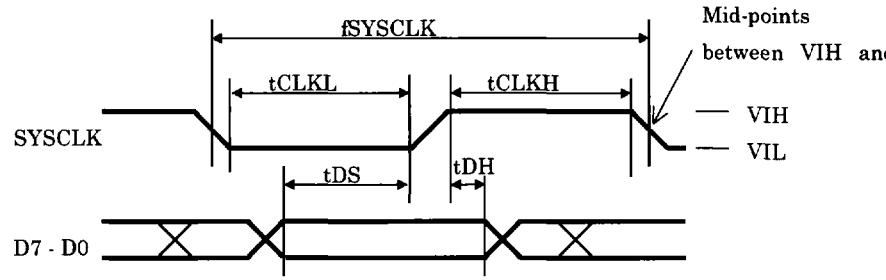
Note 5) All DACs are off with no system clock.

Note 6) NTSC internal color-bar with 3ch DACs operation.

AC Characteristic

1. Pixel Data Input

Pixel Data Input Timing

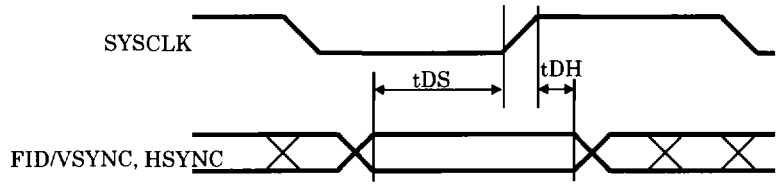


Parameter	Symbol	Min	Typ	Max	Units
SYSCLK	fSYSCLK		27		MHz
SYSCLK Pulse Width H	tCLKH	15			nsec
SYSCLK Pulse Width L	tCLKL	15			nsec
Data Setup Time	tDS	8			nsec
Data Hold Time	tDH	5			nsec

2. Synchronizing Signal(FID/VSYNC, HSYNC)

2-1 [Input Synchronizing Signal]

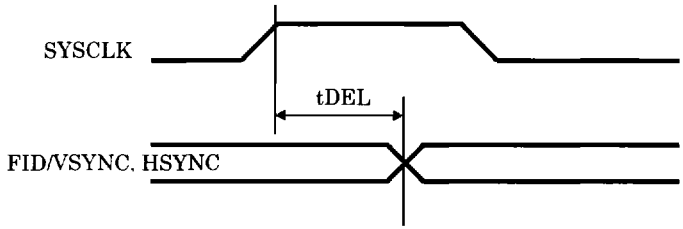
Input Synchronizing Signal Timing



Parameter	Symbol	Min	Typ.	Max	Units
Data Setup Time	tDS	8			nsec
Data Hold Time	tDH	5			nsec

2-2 [Output Synchronizing Signal]

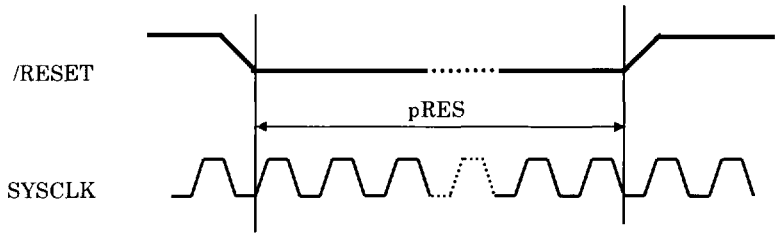
Output Synchronizing Signal Timing



Parameter	Symbol	Min	Typ.	Max	Units
Delay from SYSCLK	tDEL			25	nsec

3. Reset (Initialize)

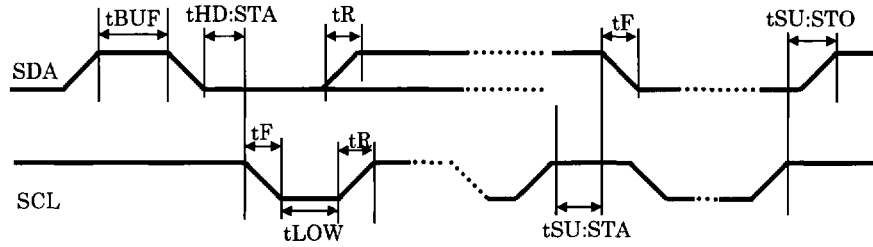
Reset Timing



Parameter	Symbol	Min	Typ.	Max	Units
/RESET Pulse Width	pRES	10			SYSCLK

4 I2C Bus

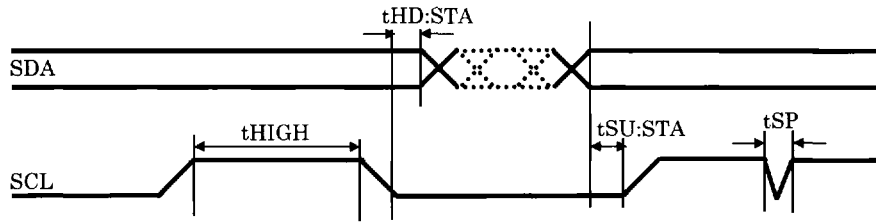
4-1 I2C Bus I/O Timing1 (SCL 400kHz cycle mode)



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		μ sec
Hold Time (Start Condition)	tHD:STA	0.6		μ sec
Clock Pulse Low Time	tLOW	1.3		μ sec
Bus Signal Rise Time	tR	20+0.1Cb*	300	nsec
Bus Signal Fall Time	tF	20+0.1Cb*	300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		μ sec
Setup Time(Stop Condition)	tSU:STO	0.6		μ sec

*Cb is total load capacitance(Units of pF) of the I2C bus line. Minimum values are not tested.

4-2 I2C Bus I/O Timing2 (SCL 400kHz cycle mode)



Parameter	Symbol	Min	Max	Units
Data Setup Time	tSU:DAT	100 Note 1)		μ sec
Hold Time (Start Condition)	tHD:DAT	0.0	0.9 Note 2)	μ sec
Clock Pulse Low Time	tHIGH	0.6		μ sec
Noise Suppression	tSP		50 Note 3)	nsec
SCL Frequency	fSCL		400	kHz

Note 1) When using under standard mode, the condition of tSU:DAT ≧250nsec must be satisfied.

Note 2) When the system does not extend tLOW (tLOW=minimum standard), this condition must be satisfied.

Note 3) Represents typical value. Not tested.

I/O pin Capacitance

Parameter	Symbol	Min	Typ.	Max	Units
Input Pin Capacitance			11		pF
Output Pin Capacitance			11		pF

(Note) Sample value. Not tested. *Condition f=1MHz

Parameter	Symbol	Min	Typ.	Max	Units
I/O Pin Capacitance SDA pin			11		pF
Input Pin Capacitance SCL pin			11		pF

(Note) Sample value. Not tested.

DAC Out Load Capacitance

Parameter	Symbol	Min	Typ.	Max	Units
DAC Load Capacitance				30	pF

(Note) Sample value. Not tested. *Condition f=1MHz

FUNCTIONAL DESCRIPTION

♦ Reset

When the reset pin /RESET set to "L", AK8810 is put in reset state. After the reset, the video outputs are in high-impedance. AK8810 starts in the internal initializing sequence at the rising edge of the first SYSCLK after the reset pin is "L". If there is no SYSCLK, AK8810 does not start in the initializing sequence. All internal registers are set to be default value by this initializing sequence.

♦ Master-Clock

AK8810 requires 27MHz clock at SYSCLK pin for operation. Video input data (CCIR-656) is sampled at the rising edge of this 27MHz . When SYSINV pin is "H" , video input data is sampled at the falling edge of 27 MHz.

♦ Video Signal Interface

AK8810 can interface with the video input data by the following 3 modes.

1. CCIR-656 Format

AK8810 decodes EAV in a data-line and manages an internal synchronization.
In this case, AK8810 outputs FID (odd : "L" even : "H")/ VSYNC and HSYNC.

2. CCIR-656 like Format (4:2:2 YCbCr)

There are MASTER and SLAVE modes, for CCIR-656 like Format which does not include EAV.

<Master Mode>

AK8810 provides FID/VSYNC and HSYNC to an external device according to the AK8810 internal timing counter. AK8810 start to sample the input data at the fixed value on the internal pixel counter.

<Slave Mode>

FID/VSYNC and HSYNC is supplied by an external device. AK8810 samples the data as same manner of Master mode.

♦ Video Signal Conversion

Video reconstruction module converts the multiplexed data (ITU-R601 Y,Cb,Cr) to the interlace format of NTSC, PAL-M, PAL-B,D,G,H,I,N. The video reconstruction format is specified by the register.

The frequency of Color Sub-carrier is changed automatically by the selected format. (cf. : burst signal table) The frequency and the phase of Color Sub-carrier is also adjustable by the register. The Sub-carrier has a free-running mode and a reset-mode. In the reset-mode, the Sub-carrier is re-set automatically to the initial phase for every 4 fields (NTSC) or 8 fields (PAL).

♦ Video Filter

Luminance signal and chroma signal modulated by the Sub-carrier pass through the Type-A filter that corrects the attenuation of the DAC's aperture effect up to 5 MHz.

For the luminance component of composite signal, it is possible to select the narrow-band filter Type-B to ease the Y/C separation.

Chroma signal (Cb,Cr) before modulation passes through the 1.3 MHz Low pass filter.

Fig. 1 Filter Type A

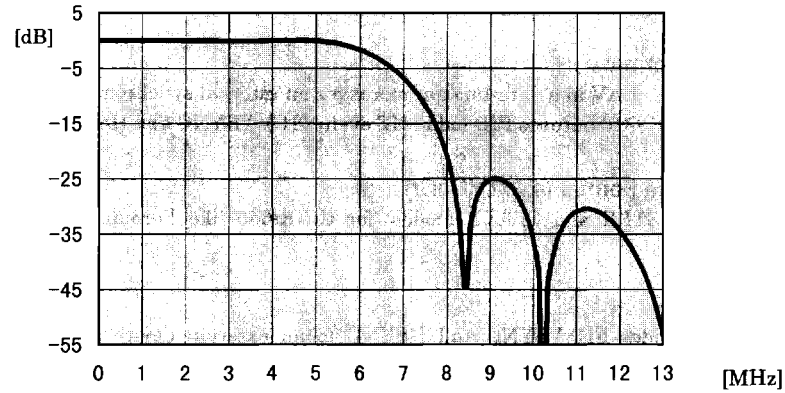
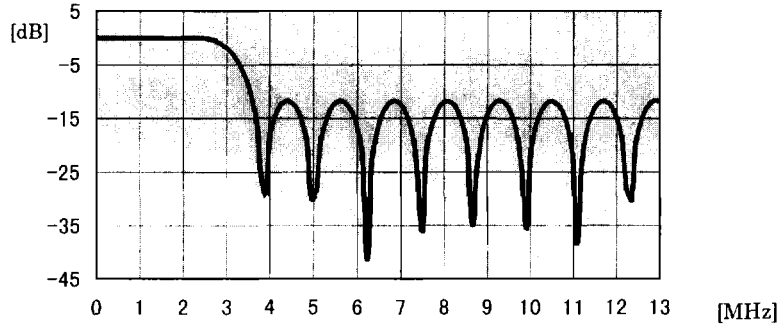


Fig. 2 Filter Type B



♦ Color burst signal

Burst signal is made by the 24bit-adder (Digital Frequency Synthesizer). The Default frequency of the color burst is selected automatically by the video reconstruction format.

Standard	Sub-carrier Freq. (MHz)
NTSC-M	3.57954545
PAL-M	3.57561188
PAL-B,D,G,H,I	4.43361875
PAL-N(Arg.)	3.5820558
PAL-N(non-Arg.)	4.43361875

Burst Signal Table

The burst frequency and initial phase resolution are as follows.

Frequency resolution	0.8046Hz
SCH Phase resolution	360/256°C

♦ Video DAC

AK8810 has the three currents driven 10bits-DACs at 27MHz operation. The full-scale of DAC is determined by the current that flow IREF pin. Typical output voltage is 1.28Vo-p under condition of VREFIN 1.235V, 6.8KΩ at IREF pin and DAC load resistance of 220Ω. This full-scale voltage is adjustable from –10% to +10% by adjusting the outer 6.8k resistance.

Each DAC output can be set individually "ON/OFF" by the register. If the DAC is "OFF", then the output is Hi-impedance. When three DACs are all "OFF", then the internal Vref is also "OFF". When DAC is forced to be "ON", AK8810 needs a delay-time for Vref rising time of several mil-seconds.

♦ Use external Reference Voltage

In order to improve the accuracy of DAC output, external reference voltage is available. In this case, unused Vrefout pin needs to be terminated with more than 0.1uF capacitance.

♦ Copy Protection

Macrovision Copy Protection ver7.01

Information about the Macrovision encoding functions of the AK8810 is available to Macrovision licensees. Macrovision may be contacted at:

Macrovision Corporation
1341 Orleans Drive
Sunnyvale, California 904089
USA

Attention: ACP-PPV Technical Support
FAX: (408) 743 - 8610

♦ Closed Caption and Extended Data

AK8810 supports both Closed Captioning and Extended Data. They are controlled "ON" or "OFF" respectively by the register setting. Each data consists of 2 continuous bytes register, and it is recognized as the data is renewed when the second byte is written in the register. After the data is renewed, AK8810 encodes Closed Captioning and Extended Data at the designated line. If the data isn't renewed, AK8810 outputs "ASCII-NULL" code. The data is supposed as Odd Parity and 7 bit US-ASCII code. Host should provide a parity bit.

*In PAL encoding mode, AK8810 outputs them at the same timing and same pattern as NTSC.

*The line where Closed Captioning data is encoded is as follows.

	525/60 System (SMPTE)	625/50 System (CCIR)
Closed Caption	21 Line default	21 Line default
Extended Data	284 Line default	334 Line default

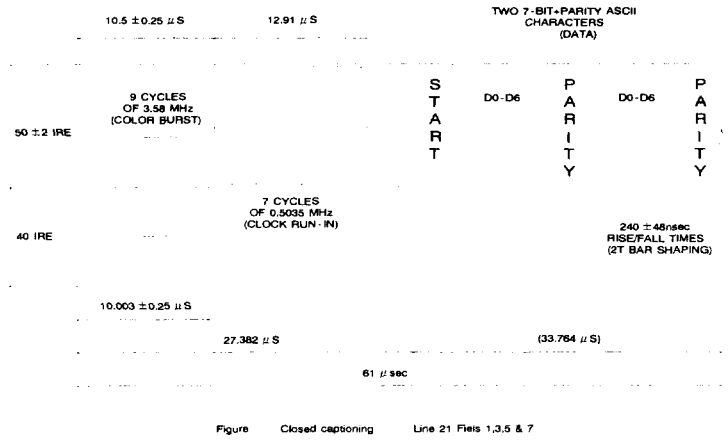


Figure Closed captioning Line 21 Fields 1,3,5 & 7

Fig. 3 Closed Captioning Wave form

♦ Video ID

AK8810 supports Video ID (EIAJ tentative standard, CPR-1204) encoding for the distinction of an aspect ratio, etc.

VBID Data Renewal Timing.

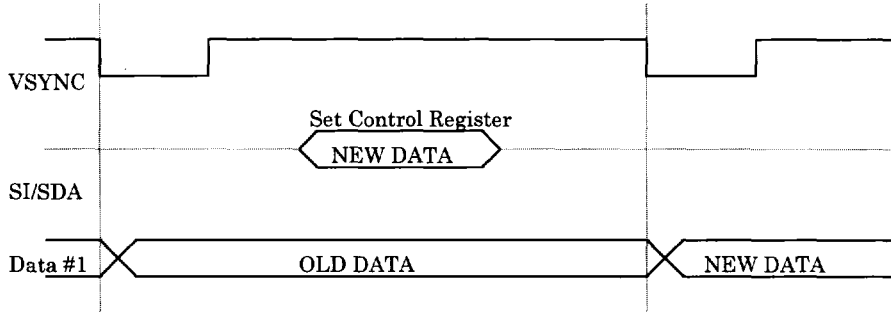


Fig. 4 VBID Data renewal Timing

VBID Data Layout

VBID is consists of 20 bits and its format is as follows.

AK8810 generates CRC code automaticaly and adds it to the data. Initial value of the Polynomial is 1.

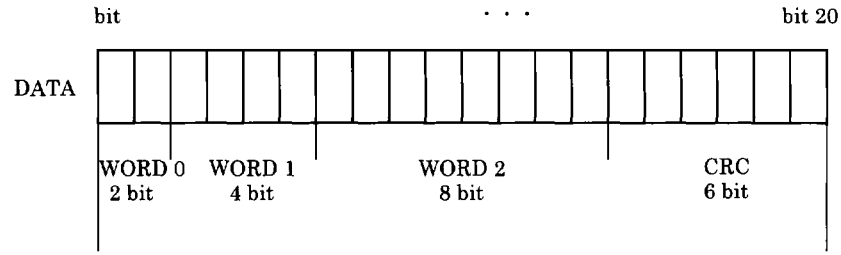


Fig. 5 VBID code assignment

VBID Waveform

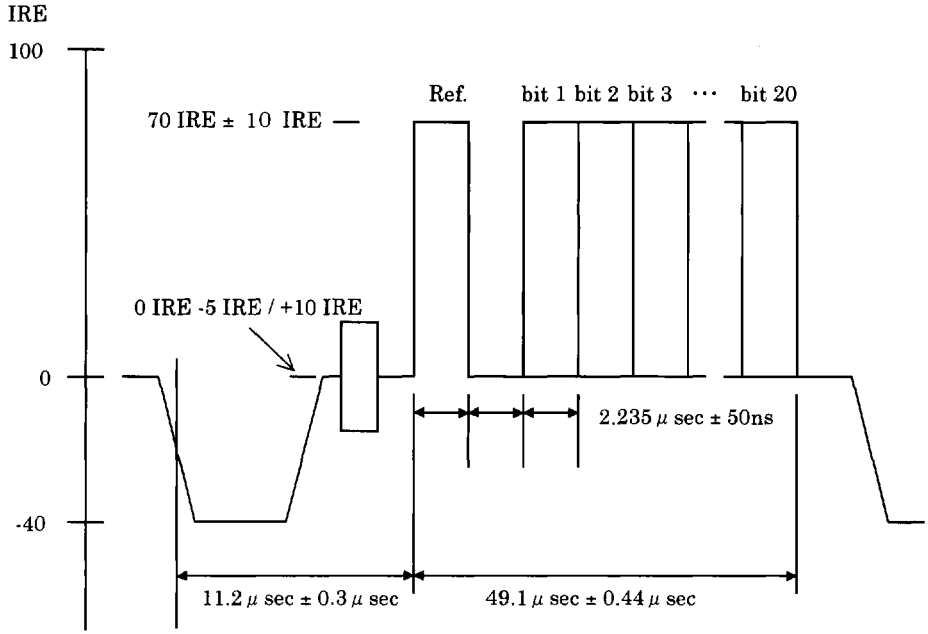


Fig. 6 VBID Wave Form

	525/60 system	625/50 system
Amplitude(10bit code)	400	392
Encode Line	20/283	20/333

VBID parameter table

♦ AK8810 Interface Timing(Part 1) Master mode

On CCIR-656 or master mode operation, AK8810 output HSYNC and FID or VSYNC (selected by register).

When AK8810 receives CCIR-656 signal, the device decodes EAV for synchronization then output the HSYNC. The HSYNC output is SYSCLK ↑ timing of data slot 32(24), which is counted from the EAV start as below.(See also AC Characteristic 2-2[Input Synchronizing Signal])

On master mode, front end device(MPEG Decoder) start to set Cb on 276(288) slot, after start to count HSYNC ↓ as 32(24) slot.

FID/VSYNC is output synchronously with HSYNC at the timing of solid line as in Fig. 9. Video Field.

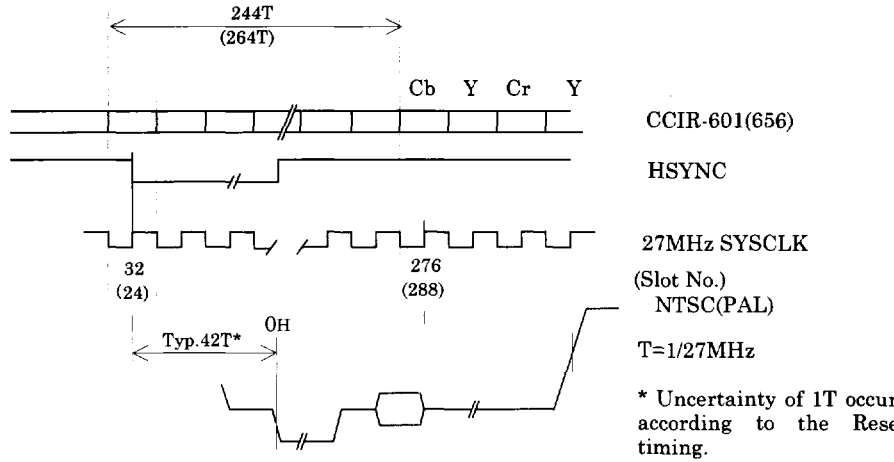


Fig. 7 Interface Timing (CCIR-656 or Master mode)

◆ AK8810 Interface Timing(Part 2) Slave mode

On slave mode operation, HSYNC and FIDorVSYNC (Selected by register) are fed to AK8810.

AK8810 monitor the transition of HSYNC on the SYSCLK ↑ timing. (Refer to AC Characteristic 2-1. [Input Synchronizing Signal]) After confirm HSYNC to Low, AK8810 recognize the 32(24) slot, internally. Then, start to sample the data as Cb on 276(288) slot.

Video field is recognized the transition timing between FID/VSYNC and HSYNC. (Fig.8. Video Field) As in the figure, there is a margin of ±1/4H.

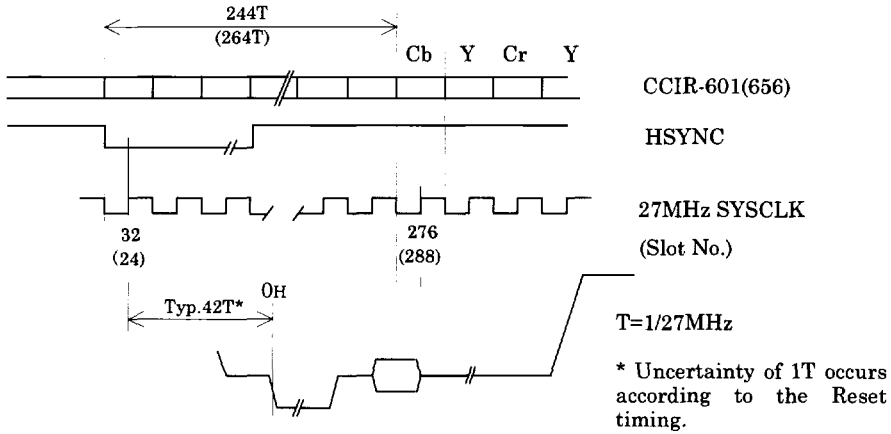


Fig. 8. Interfacing timing (Slave mode)

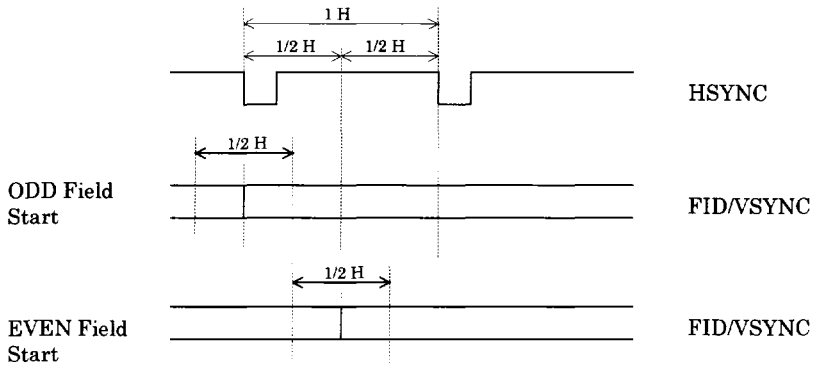


Fig. 9. Video Field

◆ HSYNC FID/VSYNC Timing

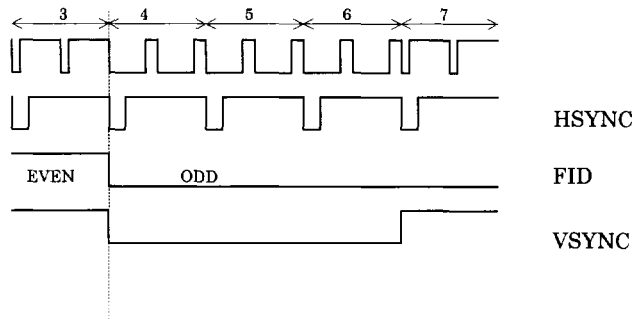


Fig. 10. NTSC / PAL/M

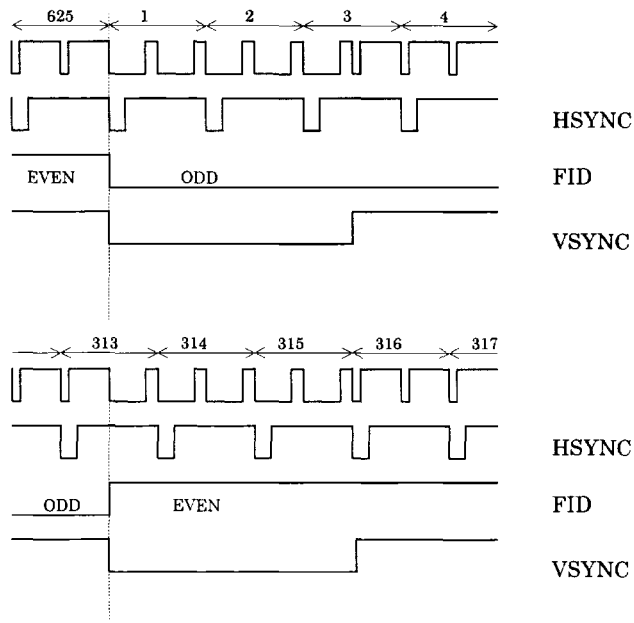
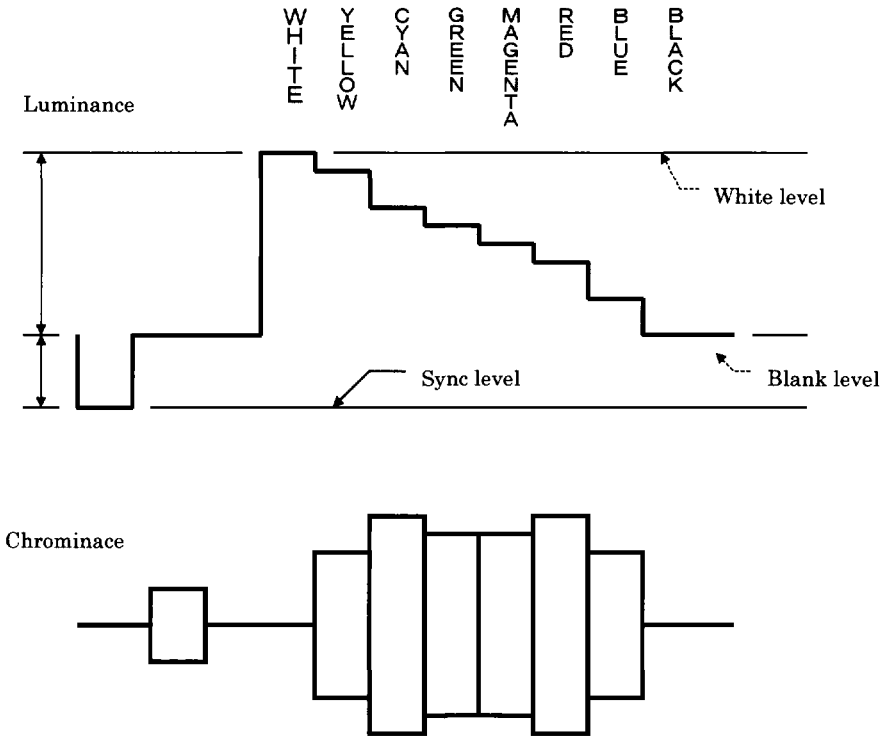


Fig. 11 PAL

◆ Color Bars

AK8810 generates the Common Color Bar signal for NTSC and PAL internally. The generated Color Bar is "100% Amplitude, 100% Saturation".



	WHITE	YELLOW	CYAN	GREEN	MAGENTA	RED	BLUE	BLACK
Cb	128	16	166	54	202	90	240	128
Y	235	210	170	145	106	81	41	16
Cr	128	146	16	34	222	240	110	128

♦ IIC Control Sequence

AK8810 is controlled by IIC bus. The slave address can be selected as 40H or 42H by selecting SELA pin.

SELA pull-down 40H
Pull-up 42H

Operation :

Write Sequence:

S	Slave Address	W	A	Sub Address	A	Data_1	A	...	Data_n	A/$\overline{A}$	Stp

* Continuous data writing is capable for the all registers.

Sequential Read: (Only Sub Address of 24H, 25H, 26H could be read)

S	Slave	W	A	*Sub Address* 24H	A	rS	Slave	R	A

DATA_24H	A	DATA_25H	A	DATA_26H	$\overline{A}$	Stp

S : Start Condition
A : Acknowledge(SDA LOW)
$\overline{A}$: Not Acknowledge(SDA HIGH)
Stp : Stop Condition
R/W:1: Read 0:Write

by Host

by AK8810

- It ignores the general call

AK8810 REGISTER MAP

Sub Address	Name	default
00H	Interface Mode	A4H
01H	Video Process 1	18H
02H	Video Process 2	00H
03H	Video Process 3	00H
04H	RESERVED	
05H	DAC Mode	00H
06H	Sub C. Freq.	00H
07H	Sub C. Phase	00H
08H-15H	RESERVED	
16H	Closed Caption R	00H
17H	Closed Caption R	00H
18H	Closed Caption R	00H
19H	Closed Caption R	00H
1AH	Video ID Data	00H
1BH	Video ID Data	00H
1CH-23H	RESERVED	
24H	STS Data	–
25H	Device ID	21H
26H	Device REV	01H
27H-29H	RESERVED	

Interface Mode Register (W only default A4H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H	BLN4	BLN3	BLN2	BLN1	BLN0	FID	MAS	CCIR

Symbol	Value	Description	
BLN4 – BLN0	*****	Line Blanking No.	default 10100
FID	0	Select VSYNC	
	1	Select FID	default
MAS	0	Slave mode	default
	1	Master mode When CCIR=0,it's valid	
CCIR	0	CCIR656 non-decode	default
	1	CCIR656 decode	

Video Process 1 Register (W only default 18H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01H			CBG	SETUP	SCR	VM2	VM1	VM0

Symbol	Value	Description	
CBG	0	Video Encode	default
	1	Generates color bar	
SETUP	0	No Set-up	
	1	7.5 IRE Set-up	default
SCR	0	Sub C. Phase Reset off	
	1	Standard Field Reset	default
VM2 - VM0	000	NTSC	default
	001	PAL-M	
	100	PAL	
	101	PAL-N-Arg	
	110	PAL-N-*non*Arg	

- When SCR is "ON", resets every 4 fields for NTSC, every 8 fields for PAL.
- Even when SETUP is "ON", there is no Set-up (Pedestal) during the blanking lines.

Video Process 2 Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02H						CC284	CC21	VBID

Symbol	Value	Description	
CC284	0	Extended Data OFF	default
	1	ON	
CC21	0	Closed Caption OFF	default
	1	ON	
VBID	0	Video ID OFF	default
	1	ON	

Video Process 3 Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03H		FLY	SYD2	SYD1	SYD0	CYD2	CYD1	CYD0

Symbol	Value	Description	
FLY	0	Y filter type B (for Composite)	default
	1	Y filter type A	
SYD2 - SYD0		S-Video Y Component delay no. from Chroma: 2's comp.	default 000
CYD2 - CYD0		Composite Y Component delay no. from Chroma: 2's comp.	default 000

- "FLY" bit selects Y signal filter for Composite signal. Type-A filter is also used to chroma signal, it compensates an aperture effect of DAC and keeps flat LPF characteristic up to 5MHz.
- S video and Y component of the composite signal can be shifted for the chroma signal independently at ±3 system clock (27MHz).

DAC Mode Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05H						OUTCP	OUTC	OUTY

Symbol	Value	Description	
OUTCP	0	Comp : OFF	default
	1	Comp : ON	
OUTC	0	C : OFF	default
	1	C : ON	
OUTY	0	Y : OFF	default
	1	Y : ON	

- Video output of AK8810 (DAC) can be forced "OFF" independently.

  The output of DAC which is forced "OFF" is Hi-impedance. When three DACs are forced "OFF", then the internal Vref is also forced "OFF". In this case, it takes several msec for the internal Vref to reach the necessary voltage after any DAC becomes "ON".

SubC Freq. Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06H	SUBF7	SUBF6	SUBF5	SUBF4	SUBF3	SUBF2	SUBF1	SUBF0

Symbol	Value	Description	
SUBF7-SUBF0		Adjustment of frequency: +127~-128 step of 0.8Hz	default 0

- AK8810 generates the necessary sub-carrier frequency from a system clock by DFS (Digital Frequency Synthesizer)
- Frequency of default is adjustable by specifying this bit. This bit adjusts the default frequency.

SubC Phase Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07H	SUBP7	SUBP6	SUBP5	SUBP4	SUBP3	SUBP2	SUBP1	SUBP0

Symbol	Value	description	
SUBP7 – SUBP0		Step: (360° /256°)	default 0

- Sub- carrier phase is adjustable by (360° /256°) step.

Closed Caption Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
16H	CC1[7]	CC1[6]	CC1[5]	CC1[4]	CC1[3]	CC1[2]	CC1[1]	CC1[0]
17H	CC2[7]	CC2[6]	CC2[5]	CC2[4]	CC2[3]	CC2[2]	CC2[1]	CC2[0]
18H	CC3[7]	CC3[6]	CC3[5]	CC3[4]	CC3[3]	CC3[2]	CC3[1]	CC3[0]
19H	CC4[7]	CC4[6]	CC4[5]	CC4[4]	CC4[3]	CC4[2]	CC4[1]	CC4[0]

Symbol	Description	
CC1[7] - CC1[0]	Line 21 –1	Closed Caption
CC2[7] - CC2[0]	Line 21 –2	
CC3[7] - CC3[0]	Line 284 -1	Extended Data
CC4[7] - CC4[0]	Line 284 -2	

- When the 2nd byte of Closed Caption Data and Extended Data is written in, AK8810 judges as the data is renewed and encodes data in the video line. NULL is output automatically in the line which is not renewed.

Video ID Data Register (W only default 00H)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1AH			bit 1	bit 2	bit 3	bit 4	bit 5	bit 6
1BH	bit 7	bit 8	bit 9	bit 10	bit 11	bit 12	bit 13	bit 14

- Bit numbers correspond to Fig. 5 VBID code assignment. (p.15)
- AK8810 generates CRC 6 bit data automatically.

Followings are read only register

STATUS REGISTER (R only)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
24H			EN284	EN21	SYNC	STS2	STS1	STS 0

Symbol	Value	Description
EN284	0	Wait for the appointed video line to encode.
	1	Ready for the C.C. data input to the register.
EN21	0	Wait for the appointed video line to encode.
	1	Ready for the C.C. data input to the register.
SYNC	0	Missing synchronization in slave mode.
	1	Synchronization was achieved.
STS2 - STS 0	***	Shows the processing field No.

- Status Register become effective when SYNC bit turns to "1". When in master mode operation, this bit is "1".
- STS2-STS2 holds the field number of processing. Some time lag is inevitable for the IIC acquisition.
- Closed caption data should be renewed after firm that the EN* flag is "1". EN* flag bit is cleared after the second byte(Sub address 17H,19H) was accessed.

Device ID (R only default 21H)

	bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
25H	0	0	1	0	0	0	0	1

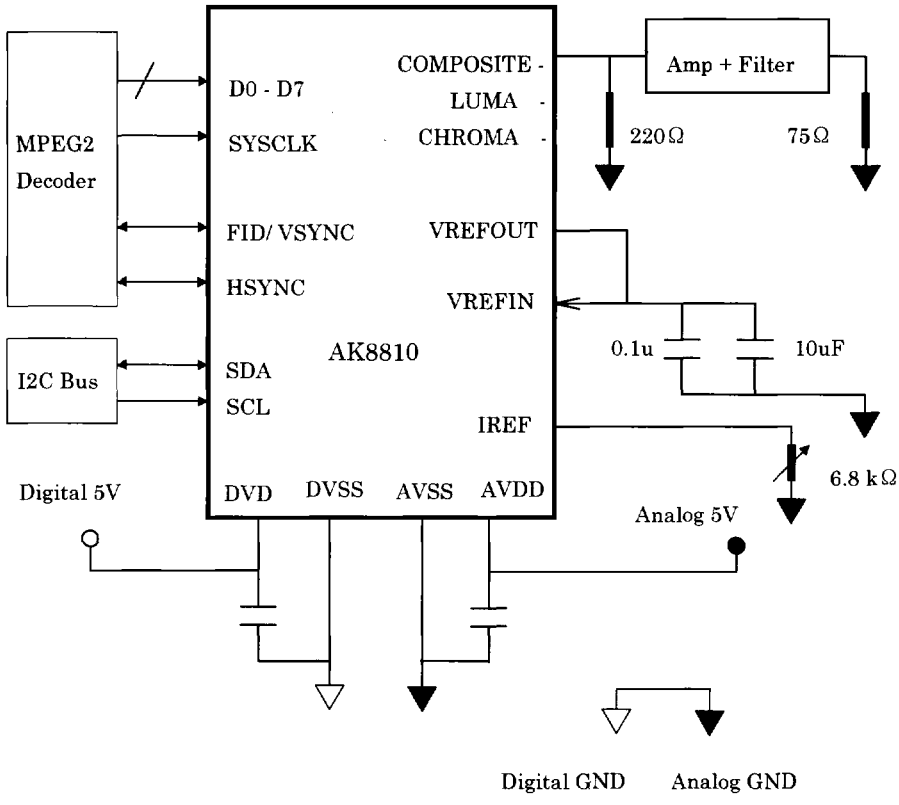
- Represents device ID. AK8810 is assigned 21H.

Device REV (R only default 01H)

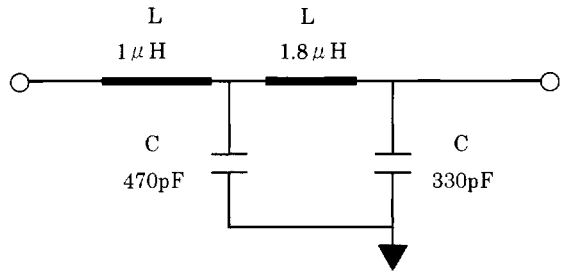
	bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
26H	0	0	0	0	0	0	0	1

- Represents device revision. Initial is 01H.

SYSTEM CONNECTION EXAMPLE

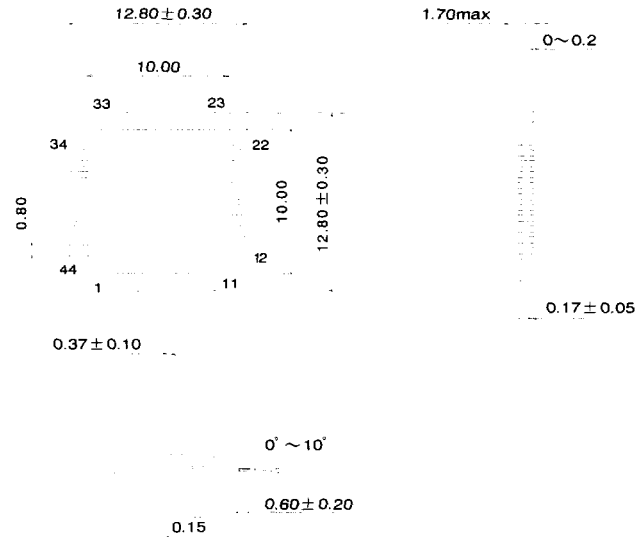


Analog filter example



PACKAGE

44pin LQFP (Unit:mm)

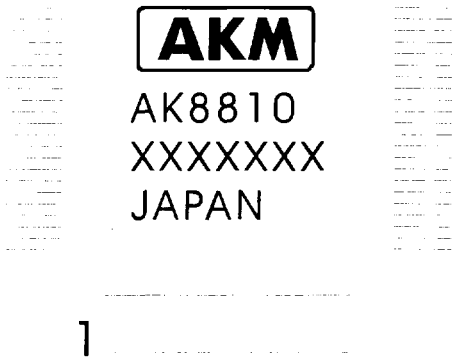


(Units : mm)

Package & Lead frame material

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code : XXXXXXX (7 digits)
3) Marketing Code : AK8810
4) Country of Origin
5) Asahi Kasei Logo