μPD77C30
ADPCM Speech Encoder/Decoder

Description

The μPD77C30 is a large-scale integration (LSI) single-chip digital processor, which compresses and decompresses digitized speech signals. It is a speech encoder/decoder that converts pulse code modulated audio to and from adaptive differential pulse code modulation (ADPCM). The μPD77C30 encodes pulse coded modulation (PCM) data into ADPCM data, and decodes ADPCM data into PCM data. The μPD77C30 is ideal for office automation applications, such as voice store and forward systems, and for various telecommunication applications. It reduces voice transmission bandwidth and voice storage requirements by half (from 64 kb/s to 32 kb/s). Its robust ADPCM algorithm makes it well qualified for transmission applications and the fact that it compresses speech by half makes it suitable for store and forward applications.

The maximum clock (CLK) frequency for the μPD77C30 is 8.33 MHz, which corresponds to a CLK cycle time of 120 ns.

The μPD77C30 accepts PCM data through its serial interface. The serial interface can be connected directly to a single-chip coder/decoder (codec) for digital μ-law PCM input/output or to a general purpose A/D or D/A converter for linear PCM code. This programmable serial interface supports both 8-bit logarithmic (μ-law) and 16-bit linear formats. The μPD77C30 interfaces to the host CPU through a standard microprocessor bus interface.

If a clock frequency of 8.33 MHz is used to encode PCM data, then the μPD77C30 requires 116 μs to process each sample, thus limiting the sampling frequency to 8.59 kHz. This implies that if the sample frequency is 8.0 kHz and the CLK is 8.33 MHz, then the internal algorithm will take approximately 93% of the time between samples. Serial data being shifted in or out has the full time between samples to accomplish the transfer of the data. This is because there is an internal buffer that is separate from the shift register and the serial input is internally read at the rising edge of the sample clock, while the next value is starting to be shifted in.

When the μPD77C30 operates in the sample 4-bit encode mode, it never outputs the value 00H. However, when it is in the sample 4-bit decode mode, it can accept 00H as an input value and interpret it the same as an input value of 88H.

The μPD77C30 performs as an intelligent peripheral device and is controlled and programmed from the host processor. The μPD77C30 offers toll quality (equivalent quality to 56 kb/s μ-law PCM) speech meeting the CCITT recommendations G.712.

The μPD77C30 has an A-law version designated the μPD77C31, which is available for products marketed in Europe.

Features

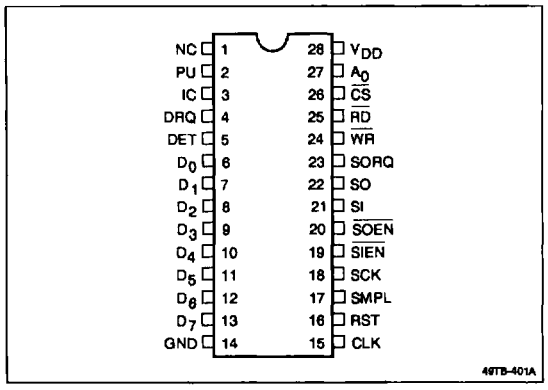
- Half-duplex ADPCM encoder or decoder
- Compression data rate
  - 32 kb/s/8 kHz sampling/4-bit data
  - 24 kb/s/8 kHz sampling/3-bit data
- Byte data (2 x ADPCM data) handling
- Robust adaptation scheme for quantizer and predictors
- Selectable functions
  - Encoder/decoder operating mode
  - ADPCM data length 3 or 4 bit
  - A/D and D/A conversion μ-law or linear
- Presentable voice detection threshold
- Standard microprocessor interface to the host CPU
- Easy interface to PCM combo
- Toll quality speech at 32 kb/s (meets CCITT recommendations G.712)
- Single +5-volt power supply
- Low-power CMOS technology
- Clock frequency 8.192 MHz maximum
- Packages: 28-pin plastic DIP and 44-pin PLCC

Ordering Information

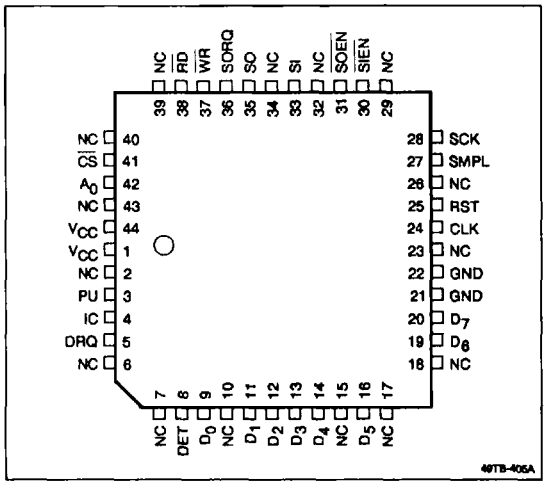
Part Number	Type	Package
μPD77C30C	CMOS	28-pin plastic DIP (600 mil)
L	CMOS	44-pin PLCC

Pin Configuration

28-Pin Plastic DIP



44-Pin PLCC



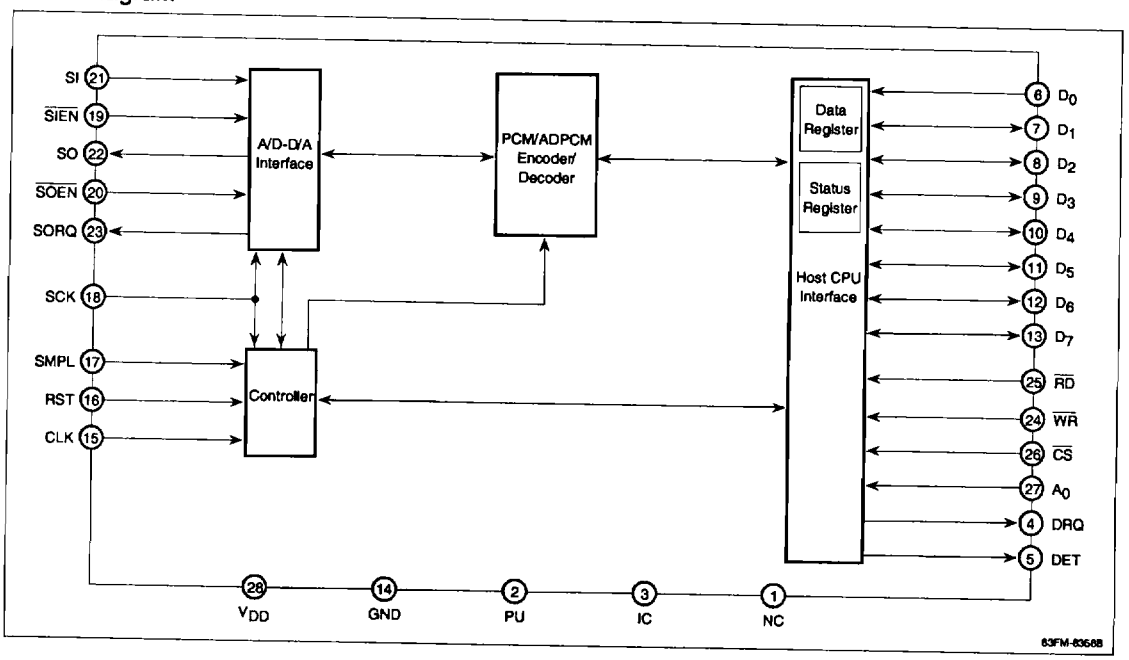
Pin Identification

Symbol	I/O	Function
Host System Interface		
A_0	In	Address 0 (register select): This input selects internal registers. A high input selects the status registers. A low input selects the data registers.
D_7 - D_0	I/O	Data bus: This three-state bidirectional data bus interfaces with the host CPU data bus.
$\overline{CS}$	In	Chip select: This input enable the $\overline{RD}$ and $\overline{WR}$ signals.

Pin Identification

Symbol	I/O	Function
DET	Out	Signal detect: This output is asserted when the input audio signal level exceeds the threshold level specified.
DRQ	Out	Data request: This output requests data transfer between the μPD77C30 and host CPU. In encoder mode, an ADPCM data read is requested. In decoder mode, an ADPCM data write is requested. (DRQ will not work unless encoder or decoder mode is specified). The data request status can also be checked by polling the RQM bit of the status register.
$\overline{RD}$	In	Read signal: This input controls data transfer from the μPD77C30 to the host CPU.
$\overline{WR}$	In	Write signal: This input controls data transfer from the host CPU to the μPD77C30.
A/D-D/A Interface		
SCK	In	Serial clock: This input provides timing for transfer of serial data to/from the A/D and D/A converter.
SI	In	Serial input: serial data input.
$\overline{SIEN}$	In	Serial input enable: This input enables data transfer on the SI pin. If not used, tie to $\overline{SOEN}$. $\overline{SIEN}$ must be asserted for the μPD77C30 to recognize an operation command.
SO	Out	Serial output: Serial data output.
$\overline{SOEN}$	In	Serial output enable: This input enables data transfer on the SO pin. If not used, tie to $\overline{SIEN}$.
SORQ	Out	Serial output request: This output indicates that serial request output data is ready for transfer at the SO pin.
Circuit Control		
CLK	In	Clock: 8.192 MHz TTL clock input.
GND	In	Ground.
IC	—	Internal connection: This pin is connected internally and should be left open.
NC	—	No connection: This pin is not connected.
PU	—	Pullup: Pull this pin up to V_{DD}.
RST	In	Reset: A high input to this pin initializes the μPD77C30.
SMPL	In	Sample: This input determines the rate at which the μPD77C30 processes ADPCM data. This rate must equal the sampling clock of the A/D and D/A converter. SMPL must be active for the μPD77C30 to recognize an operation command.
V_{DD}	In	+5-volt power supply

Block Diagram



FUNCTIONAL DESCRIPTION

The μPD77C30 has the following functional units:

- A/D-D/A interface
- PCM/ADPCM encoder/decoder
- Controller
- Data register
- Status register
- Host CPU interface

The ADPCM method is a medium bandwidth coding technique that represents speech waveforms. The specific ADPCM used employs a robust adaptation scheme for a quantizer and predictor to withstand transmission bit errors. Figure 1 shows the block diagram of the algorithm. The algorithm uses a backward adaptive quantizer and a fixed predictor so it never generates unstable poles in a decoder transfer function. This approach guarantees the stability of the decoder even with transmission errors.

The μPD77C30 can operate in either encoder or decoder mode, but it only be set to one of the two modes at a time; it cannot handle simultaneous encoding and decoding. In encoder mode, the μPD77C30 accepts either linear or μ-law PCM data from its serial voice interface, encodes it to ADPCM data format, and passes the ADPCM data through the parallel data bus to the host system. In decoder mode, the μPD77C30 receives ADPCM data from the host CPU, decodes it to either linear or μ-law format, and sends it to the output port of the serial interface.

The μPD77C30 has serial interfaces that can connect directly to a single-chip PCM codec. It interfaces easily to a host CPU through its parallel bus. With its standard microprocessor bus interface, the μPD77C30 can be viewed as a complex peripheral circuit. Figure 2 shows a typical system configuration.

Figure 1. Algorithm Block Diagram

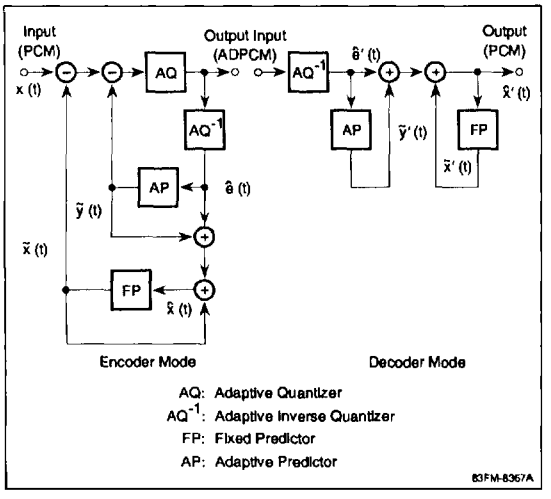
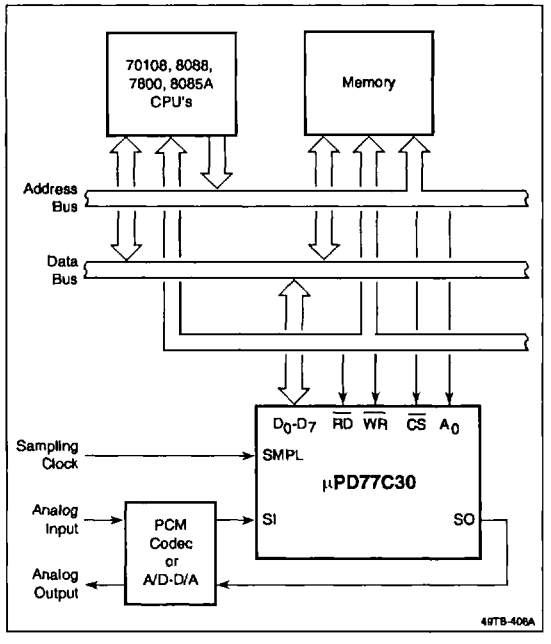


Figure 2. Typical System Configuration



OPERATIONAL DESCRIPTION

Host PCU Interface

In order to transfer ADPCM data, commands, and status, the μPD77C30 interfaces with the host CPU via D_0 - D_7 and through control lines $\overline{CS}$, A_0, $\overline{WR}$, and $\overline{RD}$. $\overline{CS}$ enables $\overline{RD}$ and $\overline{WR}$. A_0 selects either the data or status register. A low input to A_0 selects the data register. This read/write register handles both commands and ADPCM data transfer. A high input to A_0 selects the status register, a read-only register that the CPU reads to determine the state of the μPD77C30.

Parallel I/O Operation

Table 1 shows the status of the $\overline{CS}$, A_0, $\overline{WR}$, and $\overline{RD}$ pins during parallel I/O operation. Figures 3 and 4 are timing diagrams that show the read and write operations for the host CPU interface with the μPD77C30.

The RQM bit in the status register and the DRQ pin are the principal handshake signals. Their characteristics follow.

Table 1. Control Line States

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Function
1	x	x	x	No effects on internal operation.
x	x	1	1	D_0 - D_7 are high impedance.
0	0	0	1	Data from D_0 - D_7 is latched to the data register.
0	0	1	0	Contents of the data register are output to D_0 - D_7 .
0	1	0	1	Illegal operation.
0	1	1	0	Contents of the status register are output to D_0 - D_7.

x = don't care.

RQM characteristics:

- The μPD77C30 requests a data transfer to or from a host CPU by setting the RQM signal to a high level.
- After ADPCM data has transferred, the RQM goes low at the rising edge of $\overline{WR}$ or $\overline{RD}$ pulse.
- After the threshold data has transferred, RQM goes low at the second rising edge of the $\overline{WR}$ pulse.
- Reading the status register via the data bus does not reset RQM.

Figure 3. ADPCM Data Read Timing

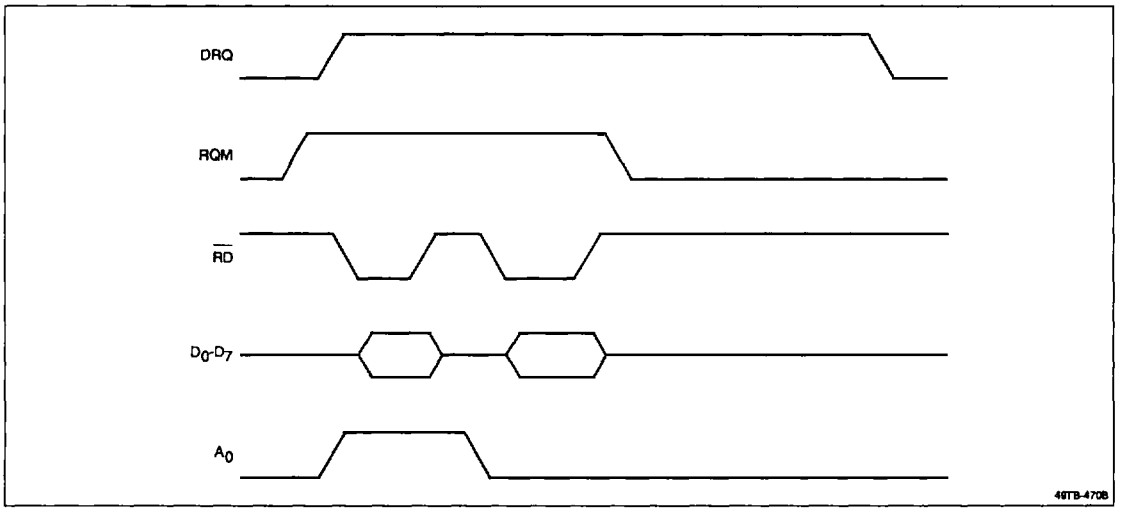
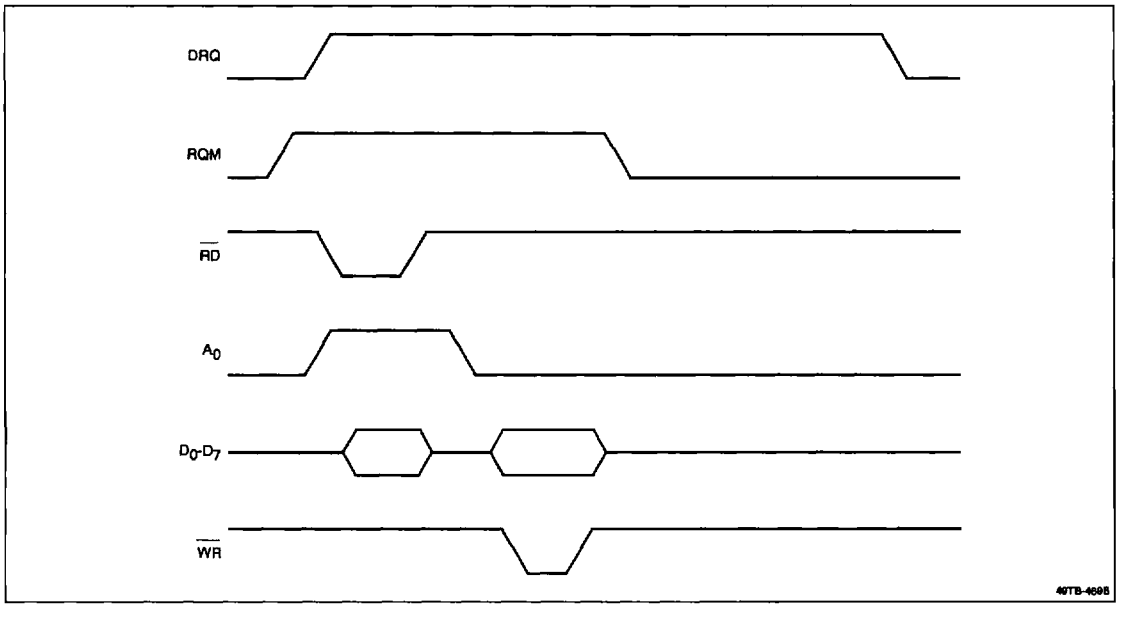


Figure 4. ADPCM Data Write Timing



DRQ characteristics:

- Except during initialization, the μPD77C30 DRQ signal is high, when the status register bit RQM is set to indicate that an ADPCM data transfer to or from the host CPU is required.
- DRQ goes low after each encoding or decoding operation is completed.
- Because DRQ remains low throughout initialization, it cannot be used for handshaking during initialization.
- The DRQ signal may be connected to an interrupt pin of a host CPU.

Two different approaches can be used for servicing ADPCM I/O request by the μPD77C30. The first approach is for the host CPU to repeatedly poll the status register until RQM = 1 is found. The second approach is for the DRQ pin to go high, forcing an interrupt of the host CPU. In either case the host CPU then reads the data register to capture the ADPCM data.

Status Register

Figure 5 shows the format of the status register.

Figure 5. Status Register Format

7	6	5	4	3	2	1	0
RQM	0	DET	DRS	0	DRC	SOL	SIL

RQM	Request for Master
0	PCM input data is 16-bit (linear)
1	PCM input data is 8-bit (μ-law)
DET	**Speech Detect**
0	Silence interval
1	Speech detected
DRS	**Data Register Status**
0	Data register is 16-bit (for threshold data)
1	Data register is 8-bit (for all other data)
DRC*	**Data Register Control**
0	Second byte transferred
1	First byte transferred
SOL	**Serial Output Data Length**
0	PCM output data is 16-bit (linear)
1	PCM ouput data is 8-bit (μ-law)
SIL	**Serial Input Data Length**
0	PCM input data is 16-bit (linear)
1	PCM input data is 8-bit (μ-law)

* DRS indicates the status of data transfers when the data register is configured as 16-bit (DRC 0)

Operation Command

Following a power-on reset, the host CPU polls the RQM bit in the status register. When the RQM bit is set, the host CPU can send an operation command to the data register, as shown in figure 6.

Figure 6. Operation Command

7	6	5	4	3	2	1	0
D_7	D_6	D_5	0	0	0	0	0

Encoder Mode D_7 - D_5	PCM Data Format	ADPCM Data Length/Sample (bits)
1 1 1	μ-law 8-bit codec (MSB first)	4
1 0 1		3
1 1 0	16-bit A/D-D/A (LSB first)	4
1 0 0		3
Decoder Mode D_7 - D_5	**PCM Data Format**	**ADPCM Data Length/Sample (bits)**
0 1 1	μ-law 8-bit codec (MSB first)	4
0 0 1		3
0 1 0	16-bit A/D-D/A (LSB first)	4
0 0 0		3

Power-on and Reset

The μPD77C30 operates on a single-phase, 50-50 duty cycle clock at 8 MHz. At power-on, asserting the RST pin for at least 3 clock cycles initializes the device, making it ready for an operation command from the host CPU. After the μPD77C30 receives the command, it stays in the specified operational mode until the next hardware reset (high level on RST). Thus, to change the μPD77C30 into different modes, reset it before writing an operation command.

Initialization and Threshold Data

See figure 7 for the initialization sequence for the encoder mode. See figure 8 for the initialization sequence for the decoder mode. During initialization signal SMPL is ignored, but the SCK and $\overline{SIEN}$ signals must be active. This is because the μPD77C30 internal code checks that the serial data is being transferred in before it accepts the mode byte. Also, it is of no consequence whether or not serial input data is valid during initialization. This is true whether the μPD77C30 is placed in encoder or decoder mode.

A hardware reset must be issued before a mode byte can be sent, even when the μPD77C30 is being powered up. A hardware reset signal also must be issued to

change modes (i.e., encoder to decoder mode). In either of the above cases, the reset signal must be held active for a minimum of 3 clock cycles to guarantee that the mode byte will be accepted. As explained below, the RQM bit of the status register should be used for data transfer handshaking, especially during initialization. The status register at a clock frequency of 8.192 MHz is not valid until 190 μs after the trailing edge of the reset pulse, and it should not be read until after that time interval.

The DRQ signal does not always follow the state of the RQM bit in the status register. In particular, the DRQ signal remains low throughout initialization. Therefore, it is essential during initialization to use the RQM bit of the status register for handshaking. The DRQ signal is intended for interrupting the host CPU so that it will transfer ADPCM data after initialization. The DRQ signal remains high until the encoding or decoding operation of the μPD77C30 is complete. The RQM bit, in contrast, is intended for data transfer handshaking and is reset after each data port transfer is complete.

When the μPD77C30 first enters the decoder mode the RQM bit is already set and the first byte of data sent to the μPD77C30 will not be decoded properly. To avoid losing the first speech sample, a dummy first byte of ADPCM should be sent.

If the operation command places the μPD77C30 in encoder mode, the next two bytes sent to the data register are the threshold data. The RQM bit establishes the data transfer signaling. In decoder mode, no threshold data is expected. The threshold data sets the level of the audio signal at which the DET pin is asserted. Figure 9 shows the format for the threshold data. Figure 10 shows how to determine the threshold data.

The μPD77C30 asserts DET when the serial input audio signal exceeds the threshold level specified by the threshold data. Many silent segments exist in normal speech signals; memory storage can be used more efficiently if these segments are omitted. The host CPU can perform silent segment compression by using DET. The energy levels of 16 previous audio samples determine the state of DET. Thus DET changes at a 2 ms (16 x 8 kHz sampling) time frame. Bit 5 of the status register reflects the state of DET.

Figure 7. Encoder Mode Initialization Sequence

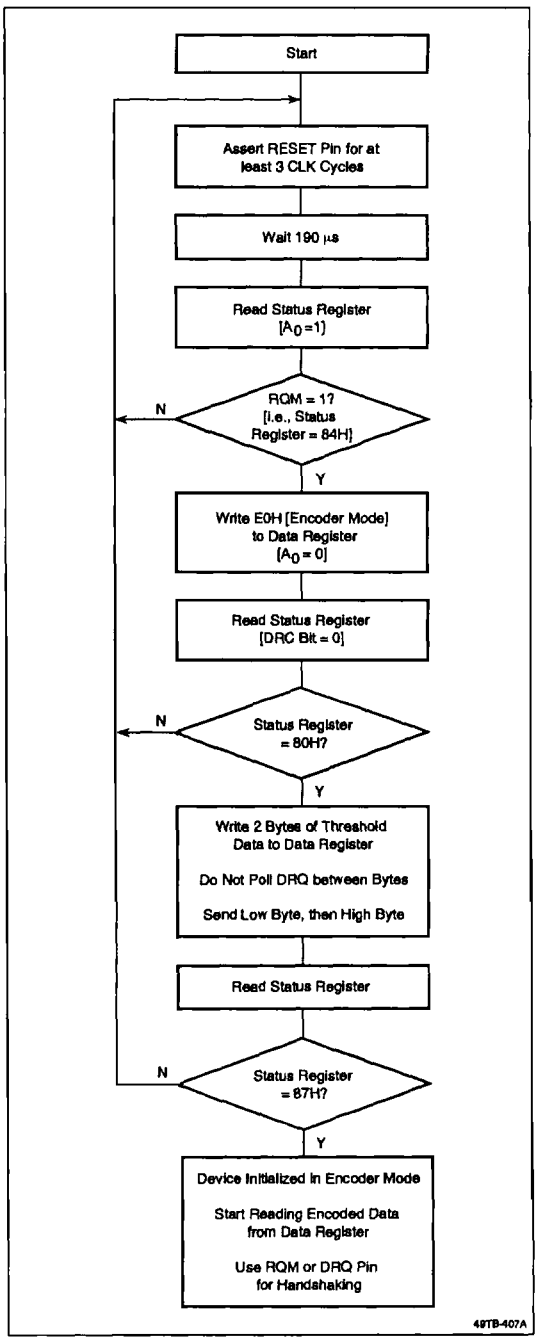


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Figure 8. Decoder Mode Initialization Sequence

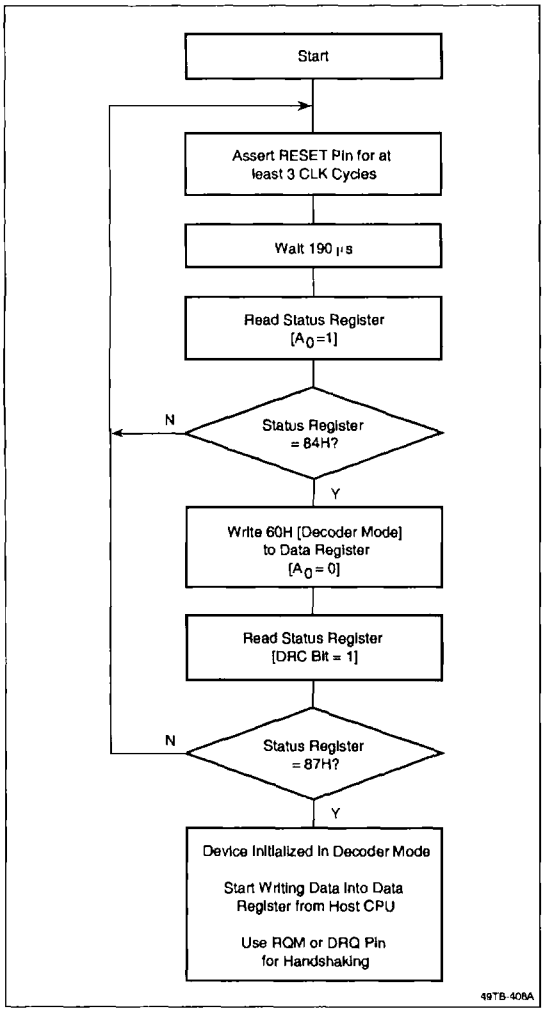


Figure 9. Threshold Data

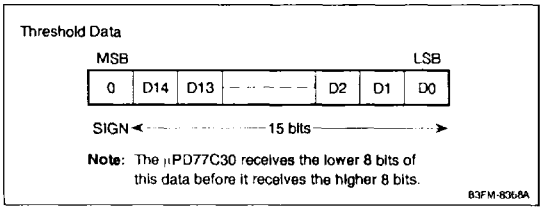
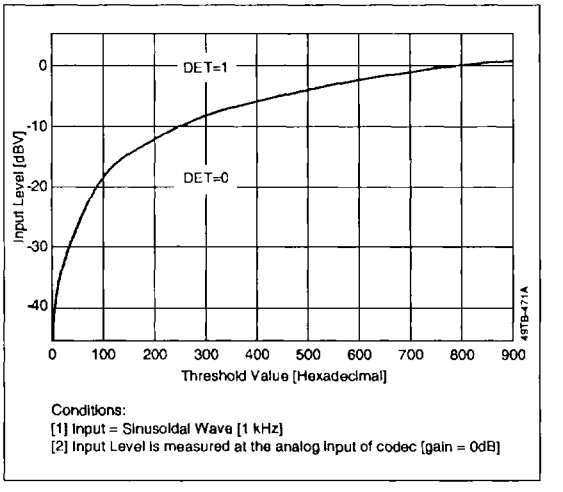


Figure 10. Typical Relationship Between Input Level and Threshold Value



ADPCM Data

In encoder mode, the μPD77C30 generates one ADPCM sample (3 or 4 bits long) each PCM sample input (8 or 16 bits long). In decoder mode, the reverse operation is performed: the μPD77C30 generates one PCM sample for each ADPCM sample input. To allow efficient data transfer to and from the host CPU, two ADPCM samples are packed into one byte and transferred at the rate of 1 byte per every 2 samples. Figure 11 illustrates the ADPCM data formats for 3 bits/sample and 4 bits/sample.

The DRQ pin initiates ADPCM data transfer. In encoder mode, this pin is asserted when ADPCM data in the data register is ready to be read by the CPU. This pin is cleared after the host CPU reads the data, and is reasserted when the next byte of ADPCM data becomes available. In decoder mode, this pin serves as the data request to the host for the next byte of ADPCM data to be sent to the data register. After the host CPU writes the ADPCM data, this pin is cleared. The host CPU cannot send another byte to the μPD77C30 until this pin is set again. (Note that the DRQ pin will not work until the μPD77C30 is placed in encoder or decoder mode.)

The ADPCM data transfer is acknowledged by the RQM bit in the status register. The RQM bit is set when transfer to the host is requested for ADPCM data, and is reset when the host read/write is complete.

Serial PCM Interface

The serial PCM interface can be connected directly to a codec. SMPL, SCK, $\overline{SIEN}$, SI, SORQ, $\overline{SOEN}$, and SO control the PCM interface.

SMPL is the sampling clock input. This signal must equal the frequency of the sampling clock of the codec or the A/D-D/A interface. SMPL is asserted after the completion of serial data transfers. Thus SMPL signals the μPD77C30 firmware to initiate processing of the next byte of ADPCM data. SMPL is rising-edge triggered, but must be held high for at least 8 clock cycles. Since it is edge-triggered, SMPL does not need to be released until the next sampling cycle.

SCK determines the timing of the serial input and output. When the μPD77C30 has data to send to the serial interface, SORQ goes high. The data is then clocked out to the SO pin serially at the falling edge of SCK, to be valid for the next rising edge. When serial data is ready to be sent to the μPD77C30 $\overline{SIEN}$ is asserted externally, and data at the SI pin is clocked in at the rising edge of SCK.

Figure 11. ADPCM Data Format

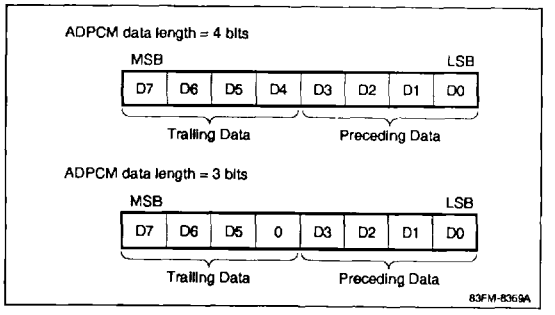


Figure 12 illustrates an example of the serial interface using a combined filter and codec (combo) chip, the μPD9514. This chip provides both the low pass filtering function and the conversion from an analog signal to digital PCM μ-law representation. The timing controller provides the proper timing relationship between the combo and the μPD77C30.

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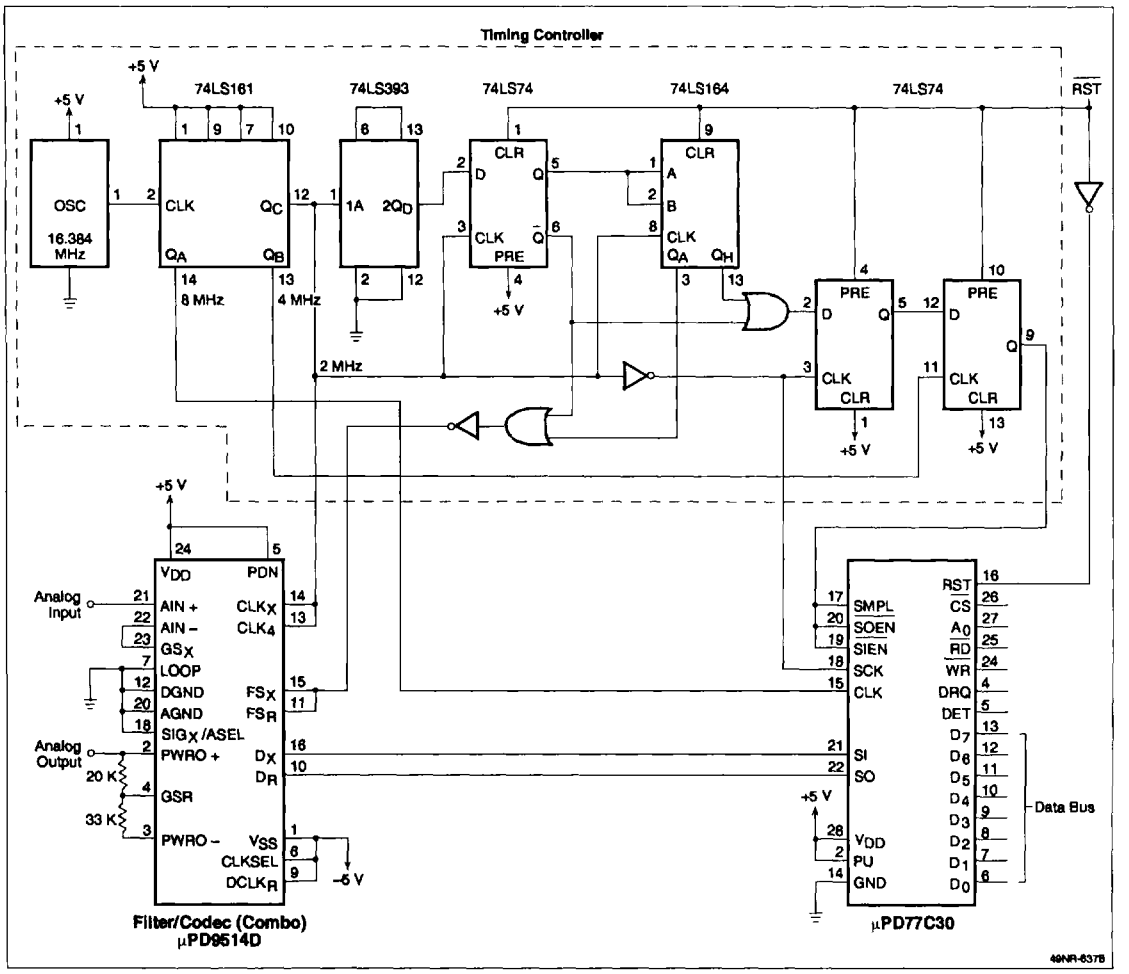
Figure 12. Serial Interface Using a Combo



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.5 V to +7.0 V
Input voltage, V_I	−0.5 V to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 V to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage

Capacitance

T_A = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CLK, SCK capacitance	C_ϕ			20	pF	
Input capacitance	C_I			10	pF	fc = 1 MHz
Output capacitance	C_O			20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	−0.3		0.8	V	
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
CLK input low voltage	V_{ILC}	3.5		0.45	V	
CLK input high voltage	V_{IHC}	−0.3		V_{CC} + 0.3	V	
Output low voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input leakage high current	I_{LIL}			−10	μA	V_I = 0 V
Input leakage high current	I_{LIH}			10	μA	V_I = V_{DD}
Output leakage low current	I_{LOL}			−10	μA	V_O = 0.47 V
Output leakage high current	I_{LOH}			10	μA	V_O = V_{DD}
Supply current	I_{DD}	24		40	mA	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CLK cycle time	ϕ_{CY}	120		2000	ns	
CLK pulse width	ϕ_D	60			ns	
CLK rise time	ϕ_r			10	ns	(Note 1)
CLK fall time	ϕ_f			10	ns	(Note 1)
A_0, $\overline{CS}$ set time for $\overline{RD}$	t_{AR}	0			ns	
A_0, $\overline{CS}$ hold time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	250			ns	
A_0, $\overline{CS}$ set time for $\overline{WR}$	t_{AW}	0			ns	
A_0, $\overline{CS}$ hold time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	250			ns	
Data set time for $\overline{WR}$	t_{DW}	150			ns	
Data hold time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$ recovering time	t_{RV}	250			ns	
SCK cycle time	t_{SCY}	480		DC	ns	

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AC Characteristics (cont)

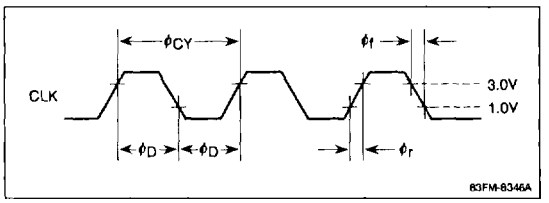
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCK pulse time	t_{SCK}	230			ns	
SCK rise time	t_{rSC}			20	ns	
SCK fall time	t_{fSC}			20	ns	
$\overline{SOEN}$ set time for SCK	t_{SOC}	50		t_{SCY} − 30	ns	
$\overline{SOEN}$ hold time for SCK	t_{CSO}	30		t_{SCY} − 50	ns	
$\overline{SIEN}$, SI set time for SCK	t_{DC}	55		t_{SCY} − 30	ns	
$\overline{SIEN}$, SI hold time for SCK	t_{CD}	30		t_{SCY} − 55	ns	
$\overline{SIEN}$, $\overline{SOEN}$ pulse width high	t_{HS}	122			ϕ_{CY}	
RST pulse width	t_{RST}	4			ϕ_{CY}	
SMPL pulse width	t_{SMPL}	8			ϕ_{CY}	
Delay time between SMPL and $\overline{SIEN}$ ($\overline{SOEN}$)	t_{DX}	−1	0	1	μs	
Data access time for $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Data float time for $\overline{RD}$	t_{DF}	10		100	ns	C_L = 100 pF
SORQ delay	t_{DRQ}	30		150	ns	C_L = 50 pF
SO delay time	t_{DCK}			150	ns	
SO delay time for SORQ	t_{DZRQ}	20		300	ns	
SO delay time for SCK	t_{DZSC}	20		300	ns	
SO delay time for $\overline{SOEN}$	t_{DZE}	20		180	ns	
SO float time for $\overline{SOEN}$	t_{HZE}	20		200	ns	
SO float time for SCK	t_{HZSC}	20		300	ns	
SO float time for SORQ	t_{HZRQ}	70		300	ns	

Note:

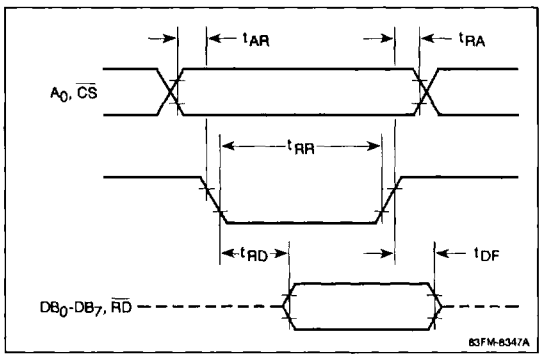
(1) AC timing measuring point voltage = 1.0 V and 3.0 V.

Timing Waveforms

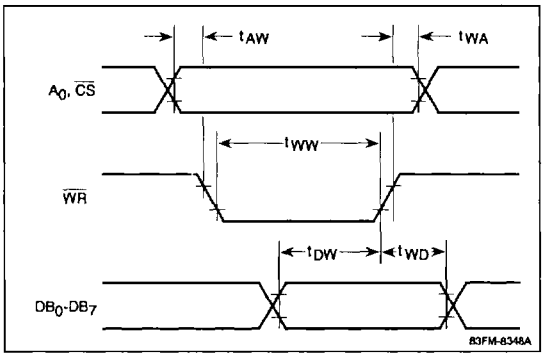
Clock



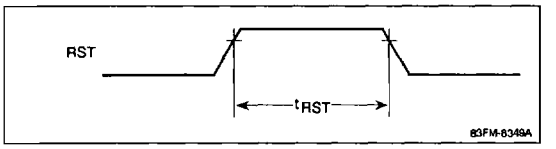
Read Operation



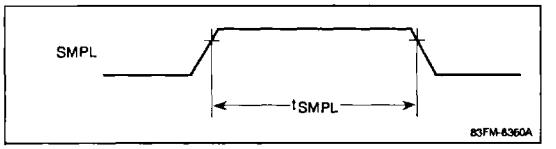
Write Operation



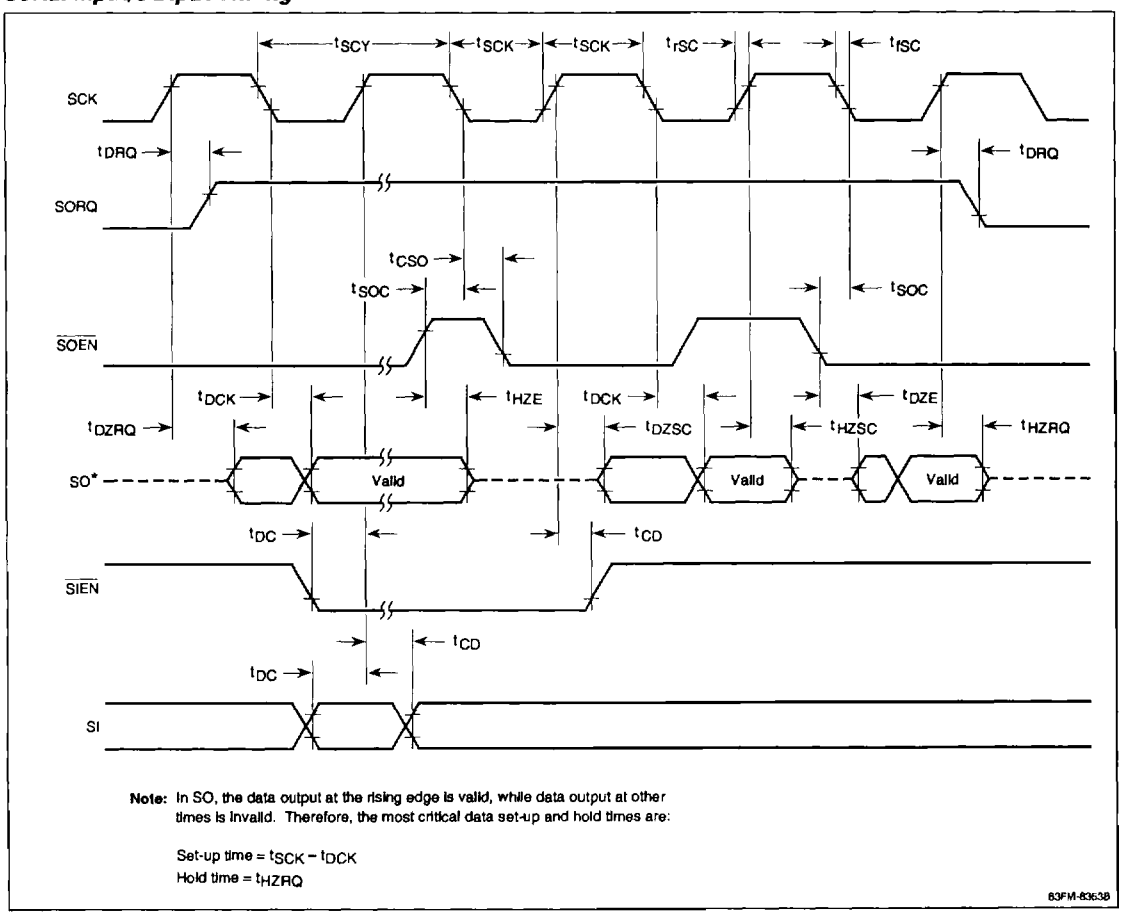
Reset



Sample



Serial Input/Output Timing



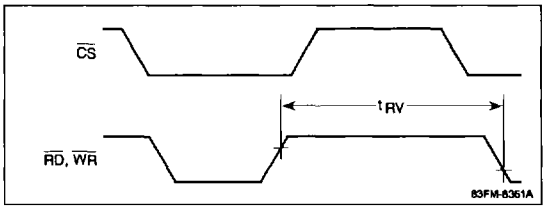
Note: In SO, the data output at the rising edge is valid, while data output at other times is invalid. Therefore, the most critical data set-up and hold times are:

Set-up time = $t_{SCK} - t_{DCK}$
Hold time = t_{HZRQ}

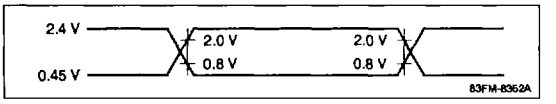
83FM-8363B

4a

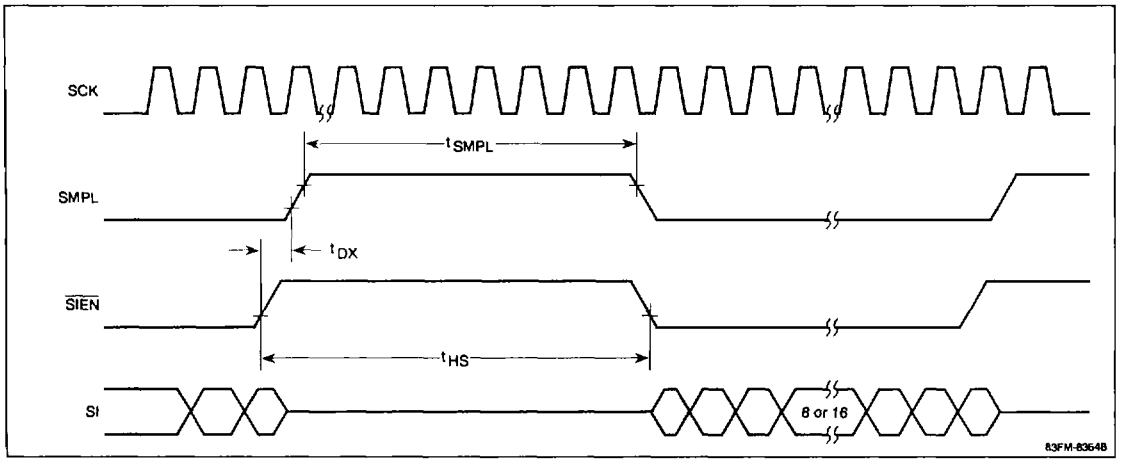
Read/Write Cycle Timing



AC Waveform Measurement Point (except CLK)



Serial Input Timing



Serial Output Timing