To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

μ PA1764

SWITCHING
DUAL N-CHANNEL POWER MOS FET
INDUSTRIAL USE

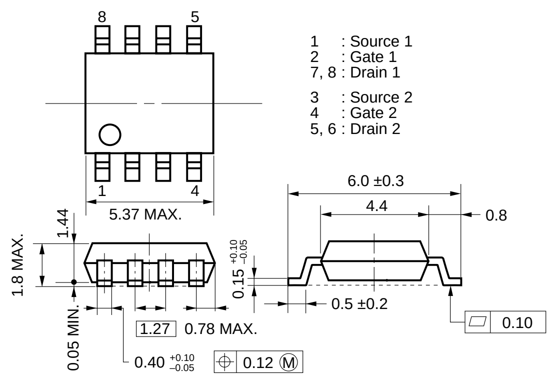
DESCRIPTION

The μ PA1764 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Dual chip type
- Low on-state resistance
  $R_{DS(on)1}$ = 27 mΩ TYP. (V_{GS} = 10 V, I_D = 3.5 A)
  $R_{DS(on)2}$ = 32 mΩ TYP. (V_{GS} = 4.5 V, I_D = 3.5 A)
  $R_{DS(on)3}$ = 34 mΩ TYP. (V_{GS} = 4.0 V, I_D = 3.5 A)
- Low input capacitance
  C_{iss} = 1300 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1764G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±7	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±28	A
Total Power Dissipation (1 unit) Note2	P_T	1.7	W
Total Power Dissipation (2 unit) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note3	I_{AS}	7	A
Single Avalanche Energy Note3	E_{AS}	98	mJ

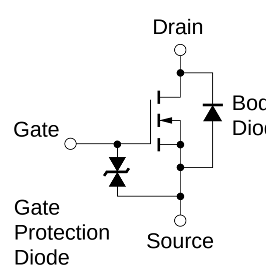
Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. T_A = 25°C, Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm

3. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 $\rightarrow$ 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

EQUIVALENT CIRCUIT
(1/2 Circuit)



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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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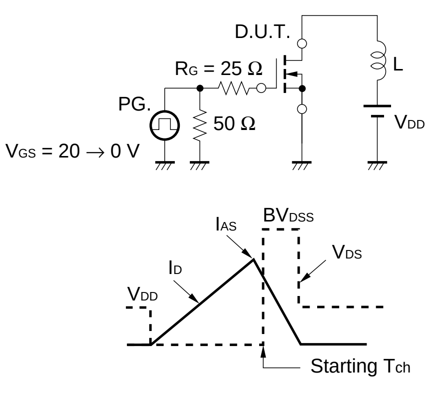
Date Published May 2001 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

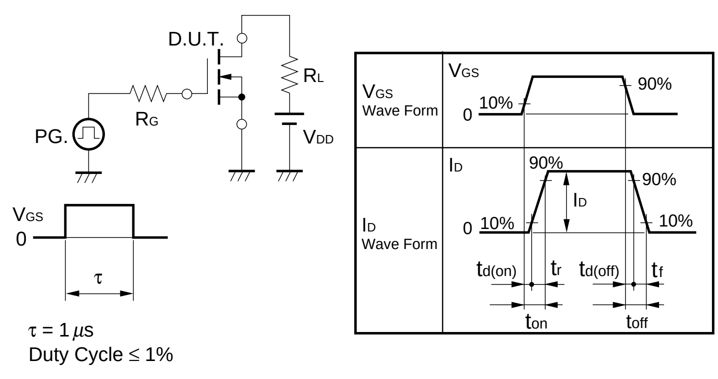
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\vert y_{fs} \vert$	V_{DS} = 10 V, I_D = 3.5 A	5.0	9.0		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.5 A		27	35	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 3.5 A		32	42	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 3.5 A		34	46	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		1300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		110		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 3.5 A		15		ns
Rise Time	t_r	V_{GS} = 10 V		69		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		65		ns
Fall Time	t_f			27		ns
Total Gate Charge	Q_G	V_{DD} = 48 V		29		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		3.6		nC
Gate to Drain Charge	Q_{GD}	I_D = 7.0 A		7.4		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0 V		0.84		V
Reverse Recovery Time	t_{rr}	I_F = 7.0 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		66		nC

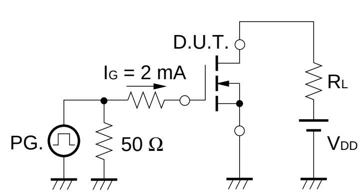
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

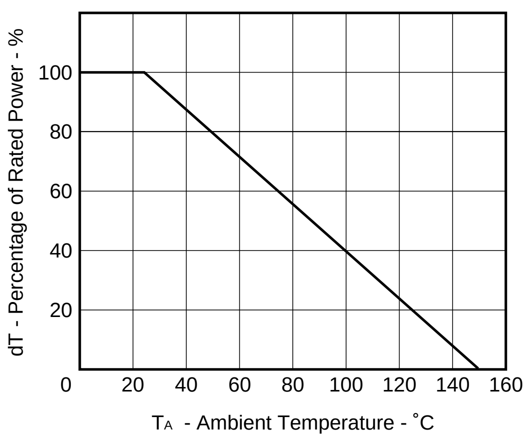


TEST CIRCUIT 3 GATE CHARGE

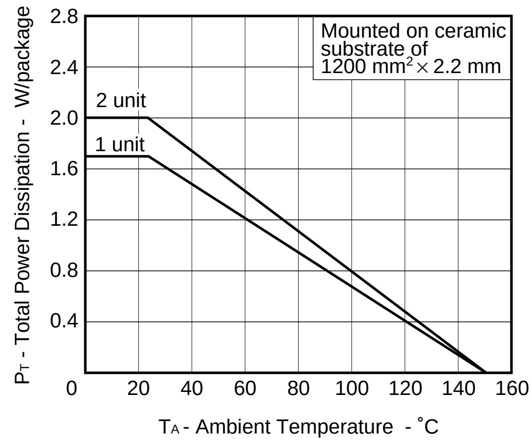


TYPICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

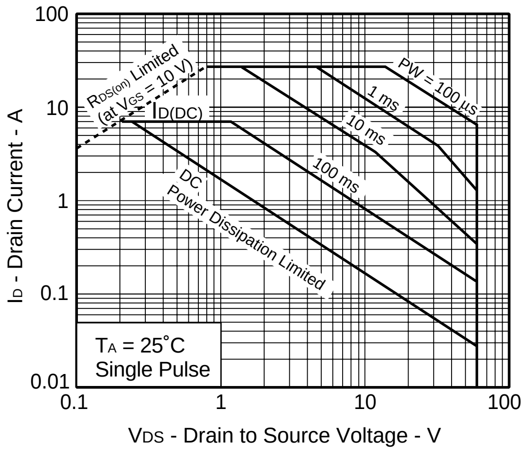
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



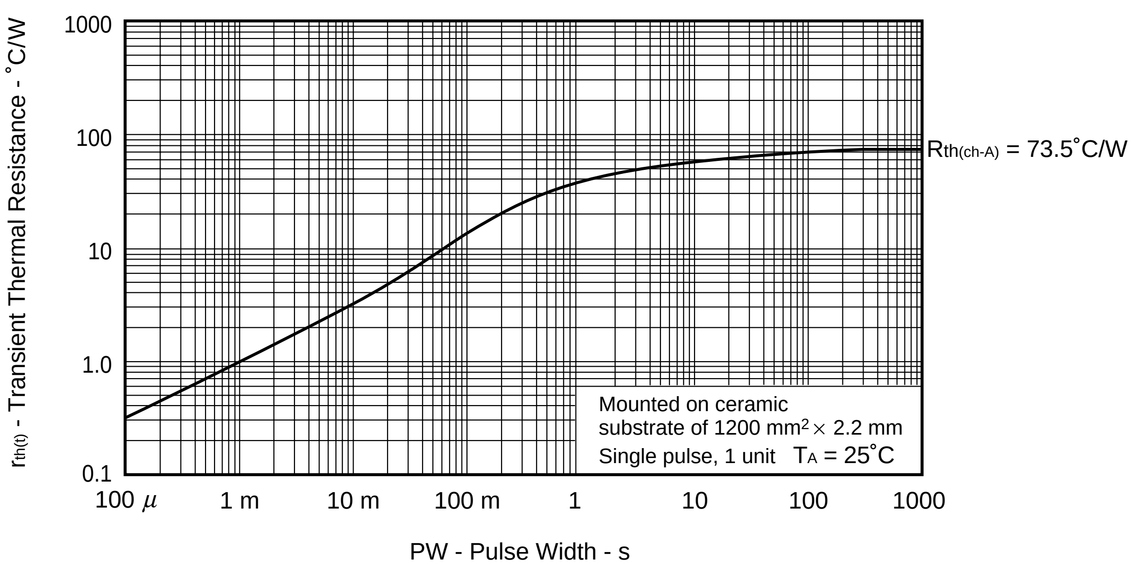
★ FORWARD BIAS SAFE OPERATING AREA

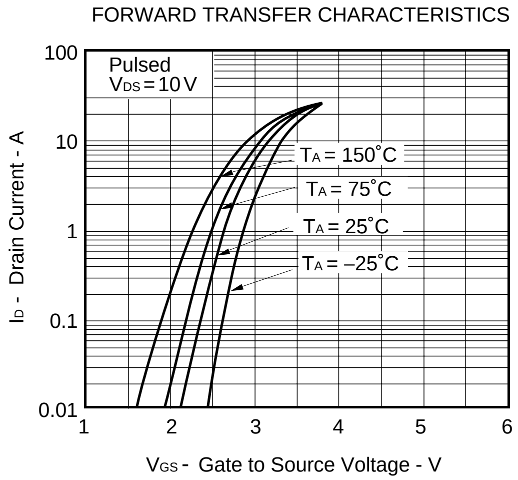


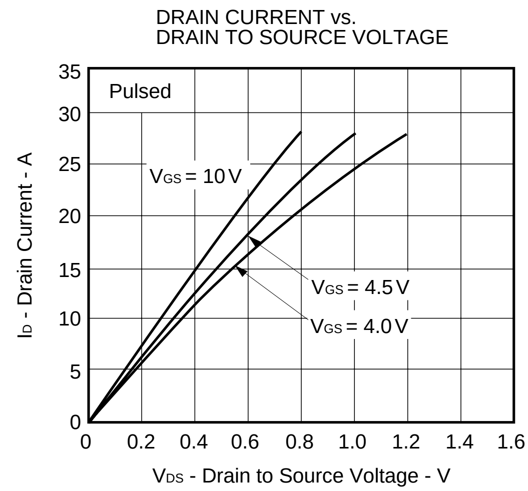
Remark

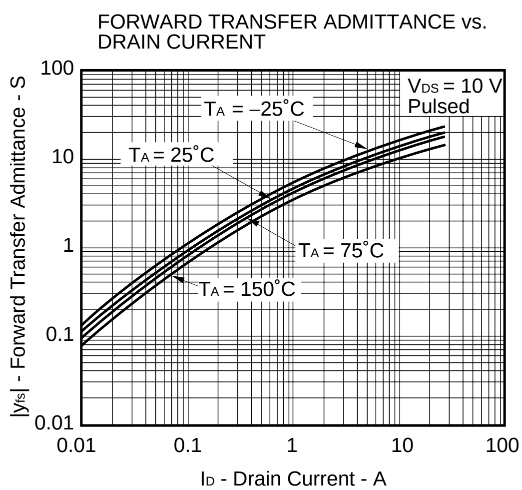
Mounted on ceramic substrate of 1200 mm^2 × 2.2 mm

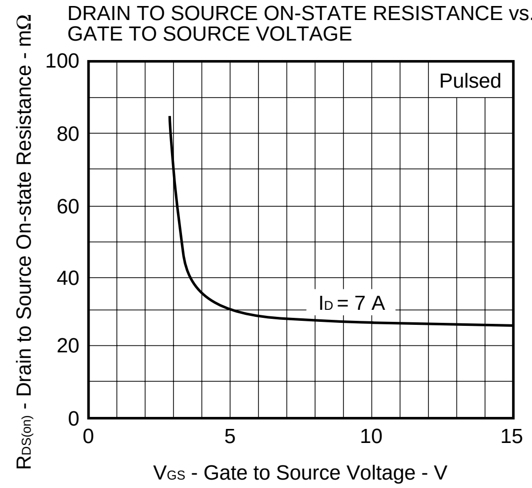
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

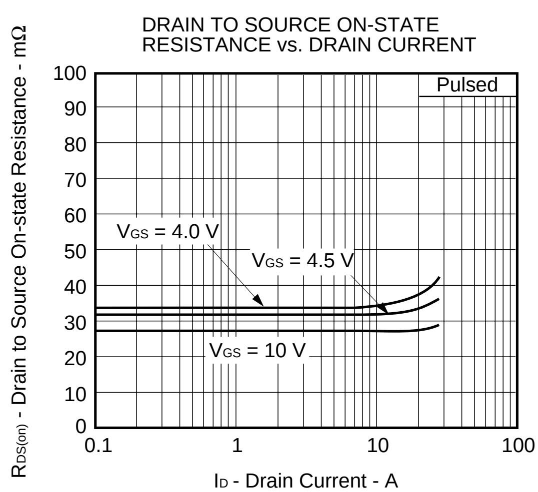


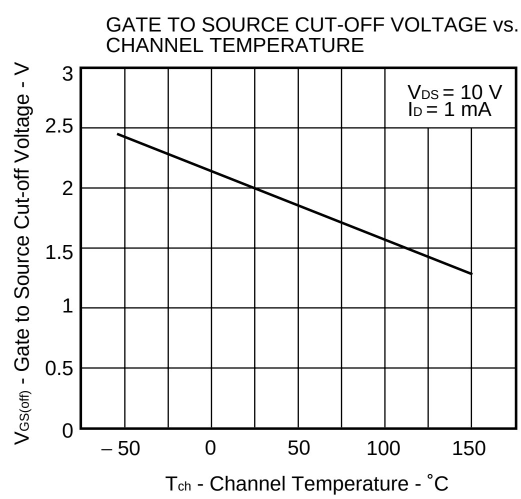

FORWARD TRANSFER CHARACTERISTICS
Pulsed
VDS = 10 V
TA = 150˚C
TA = 75˚C
TA = 25˚C
TA = –25˚C
ID - Drain Current - A
VGS - Gate to Source Voltage - V


DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE
Pulsed
VGS = 10 V
VGS = 4.5 V
VGS = 4.0 V
ID - Drain Current - A
VDS - Drain to Source Voltage - V

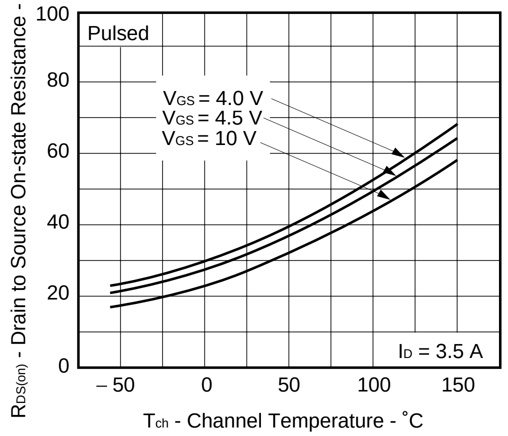

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT
VDS = 10 V
Pulsed
TA = –25˚C
TA = 25˚C
TA = 75˚C
TA = 150˚C
|yfs| - Forward Transfer Admittance - S
ID - Drain Current - A


DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE
Pulsed
ID = 7 A
RDS(on) - Drain to Source On-state Resistance - mΩ
VGS - Gate to Source Voltage - V

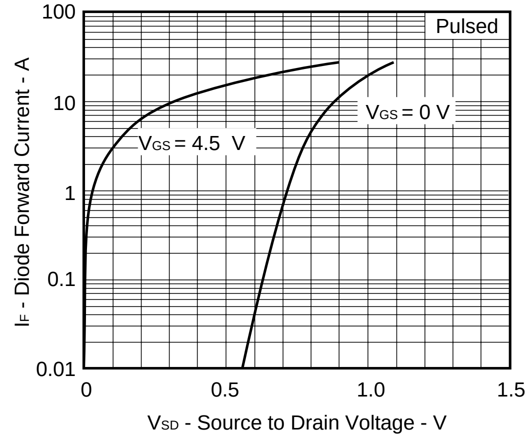

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT
Pulsed
VGS = 4.0 V
VGS = 4.5 V
VGS = 10 V
RDS(on) - Drain to Source On-state Resistance - mΩ
ID - Drain Current - A


GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE
VDS = 10 V
ID = 1 mA
VGS(off) - Gate to Source Cut-off Voltage - V
Tch - Channel Temperature - ˚C

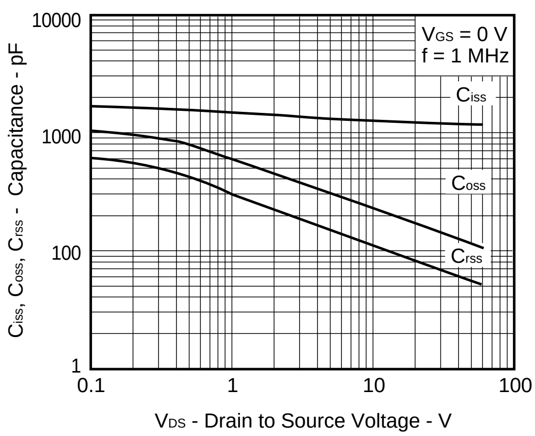
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



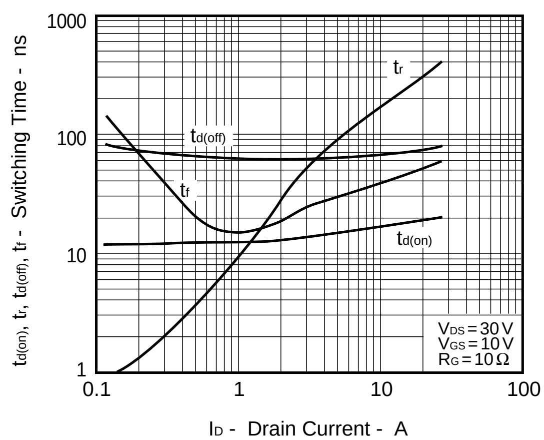
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



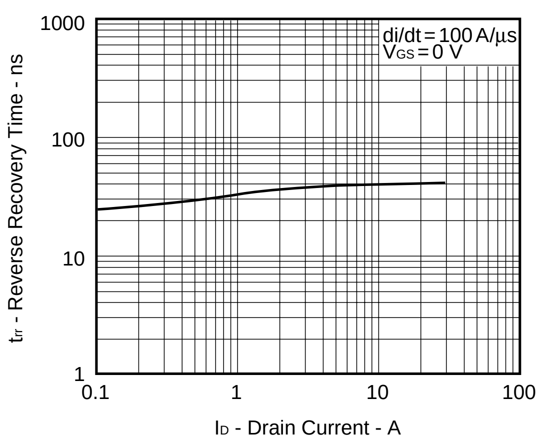
CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



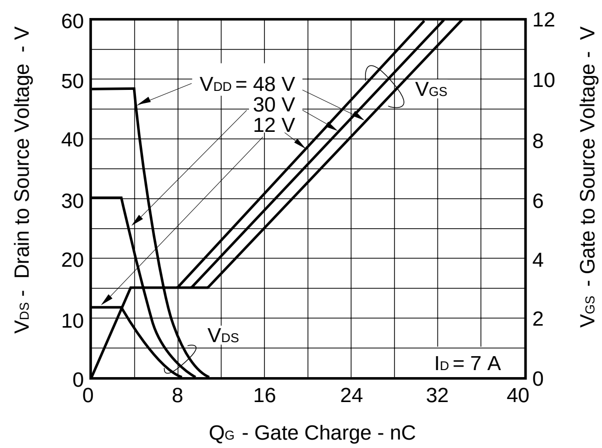
SWITCHING CHARACTERISTICS



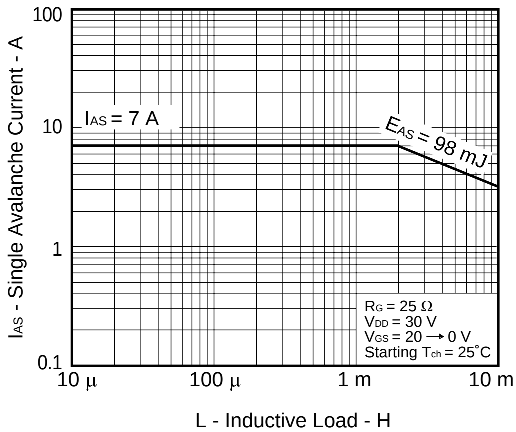
REVERSE RECOVERY TIME vs.
DRAIN CURRENT



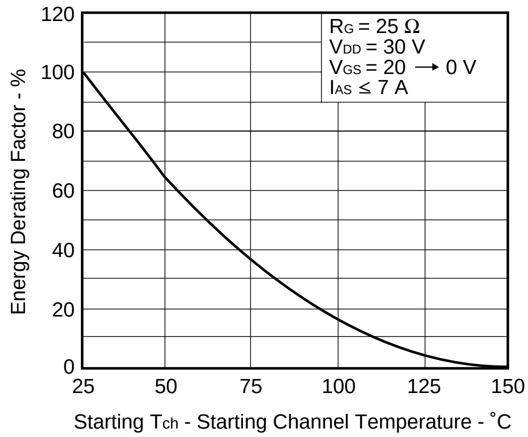
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



[MEMO]