SP8680A

550MHz÷10/11

The SP8680A is an ECL variable modulus divider, with ECL and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. It divides by 10 when either of the ECL control inputs, PE1 or PE2, is in the high state and by 11 when both are low (or open circuit). The divider can be set asynchronously to the eleventh state by applying a high level to the master set (MS) input.

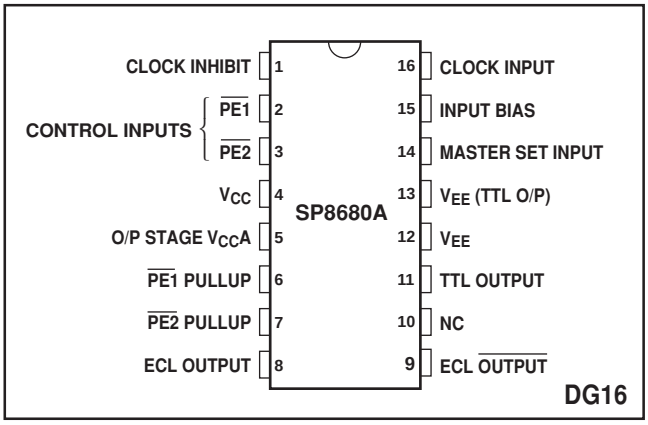


Fig. 1 Pin connections - top view

FEATURES

- Very High Speed – 650MHz (Typ.)
- ECL and TTL Compatible Inputs/Outputs
- DC or AC Clocking
- Clock Inhibit
- Asynchronous Master Set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: −4·75V to −5·5V (ECL), 4·75V to 5·5V (TTL)
- Power Consumption: 420mW
- Temperature Range: −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\|V_{CC}-V_{EE}\|$	8V
ECL output source current	50mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8680 A DG

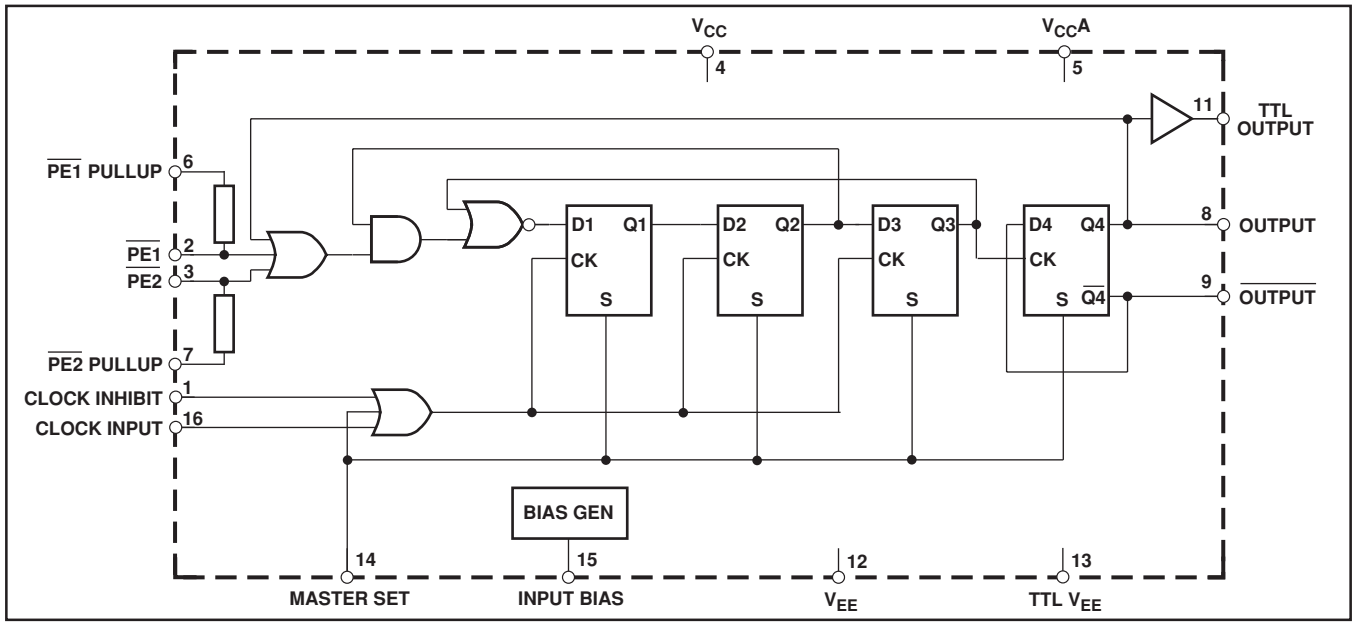


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{EE} = −4·75V to − 5·5V, V_{CC} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	550		MHz	AC coupled clock = 350mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	6
Power supply current	I_{EE}		105	mA	V_{EE} = −5·5V, pins 6, 7, 13 o/c	5
ECL output high voltage	V_{OH}	−0·93	−0·78	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
ECL output low voltage	V_{OL}	−1·85	−1·62	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
Input high voltage	V_{INH}	−0·095	−0·81	V	V_{EE} = −5·2V (25°C)	
Input low voltage	V_{INL}	−1·85	−1·475	V	V_{EE} = −5·2V (25°C)	
Input low currents	I_{IL}	0·5		µA	25°C	
Input high current, clock and MS	I_H		400	µA	V_{IN} = −1·85V (25°C)	
Input high current, PE1 and PE2	I_H		250	µA	V_{IN} = −0·8V (25°C)	
Propagation delay, clock to Q4 low	t_{pHL}		4	ns	R_L = 100Ω to −2V (25°C)	6
Propagation delay, clock to Q4 high	t_{pLH}		3	ns	R_L = 100Ω to −2V (25°C)	6
Propagation delay, MS to Q4 high	t_{pLH}		6	ns	25°C	6
Modulus control set-up time	t_s	4		ns	25°C	3, 6
Modulus control release time	t_r	4		ns	25°C	4, 6
ECL output rise time (20% - 80%)	t_{ELH}		2	ns	25°C	6
ECL output fall time (80% - 20%)	t_{EHL}		2	ns	25°C	6

TTL OPERATION

Supply voltage, V_{CC} = V_{CC}A = 4·75V to 5·5V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	550		MHz	AC coupled clock = 350mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	6
Power supply current	I_{CC}		111	mA	V_{CC} = 5·5V, pins 6, 7 o/c, pin 13 to pin 12	5
TTL output high voltage	V_{OH}	2·3		V	V_{CC} = 4·75V, I_{OH} = −640µA	5
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5·5V, I_{OL} = −20µA	5
Input high voltage, PE1 and PE2	V_{INH}	3·9		V	V_{CC} = 5·0V (25°C)	
Input low voltage, PE1 and PE2	V_{INL}		3·5	V	V_{CC} = 5·0V (25°C)	
Input low current, PE1 and PE2	I_{IL}	−4		mA	V_{CC} = 5·5V (25°C), pins 6, 7 = V_{CC}, V_{IN} = 0·4V	
Propagation delay, clock to TTL low	t_{pHL}	6	14	ns	V_{CC} = 5·0V (25°C)	6
Propagation delay, clock to TTL high	t_{pLH}	6	14	ns	V_{CC} = 5·0V (25°C)	6
Propagation delay, MS to TTL high	t_p		17	ns	V_{CC} = 5·0V (25°C)	6
Modulus control set-up time	t_s	4		ns	V_{CC} = 5·0V (25°C)	3, 6
Modulus control release time	t_r	4		ns	V_{CC} = 5·0V (25°C)	4, 6
TTL output rise time (20% - 80%)	t_{TLH}		5	ns	V_{CC} = 5·0V (25°C)	6
TTL output fall time (80% - 20%)	t_{THL}		5	ns	V_{CC} = 5·0V (25°C)	6

NOTES

1. The temperature coefficients of V_{OH} = +1·2mV/°C, V_{OL} = +0·24mV/°C and of V_{IN} = +0·8mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_S is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Tested at +25°C and +125°C only.
6. Guaranteed but not tested.

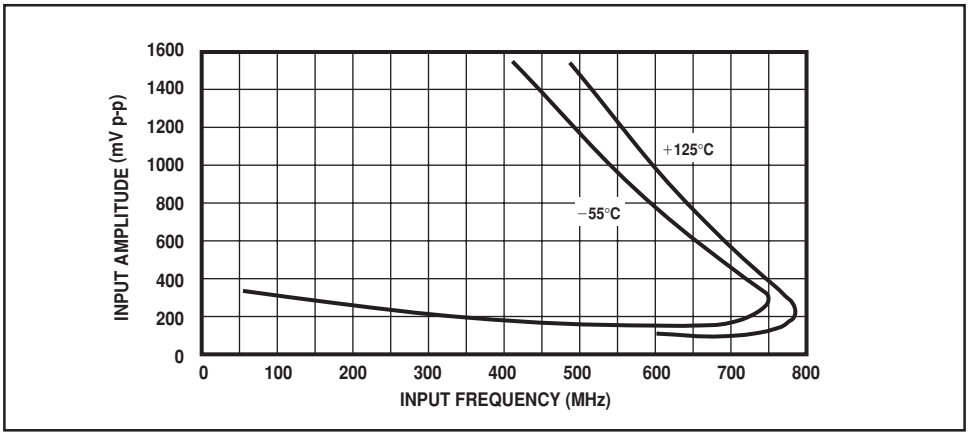
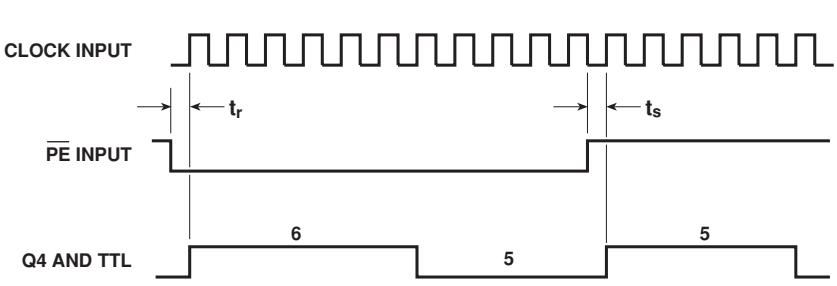


Fig. 3 Typical input sensitivity



MS	Clock inhibit	PE1	PE2	Output response
H	X	X	X	All outputs set high
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

Fig. 4 Truth table and timing diagram

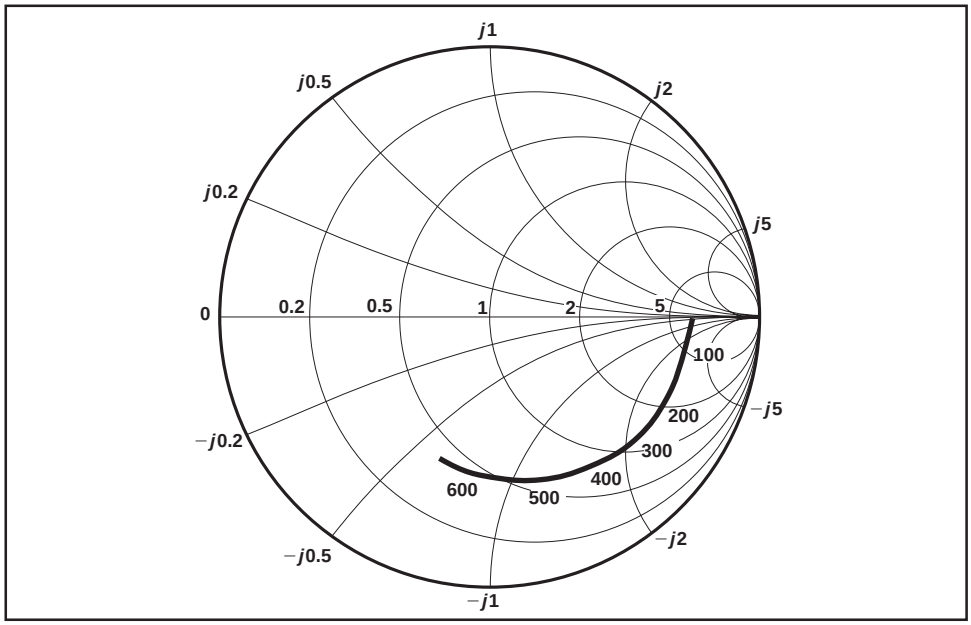


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

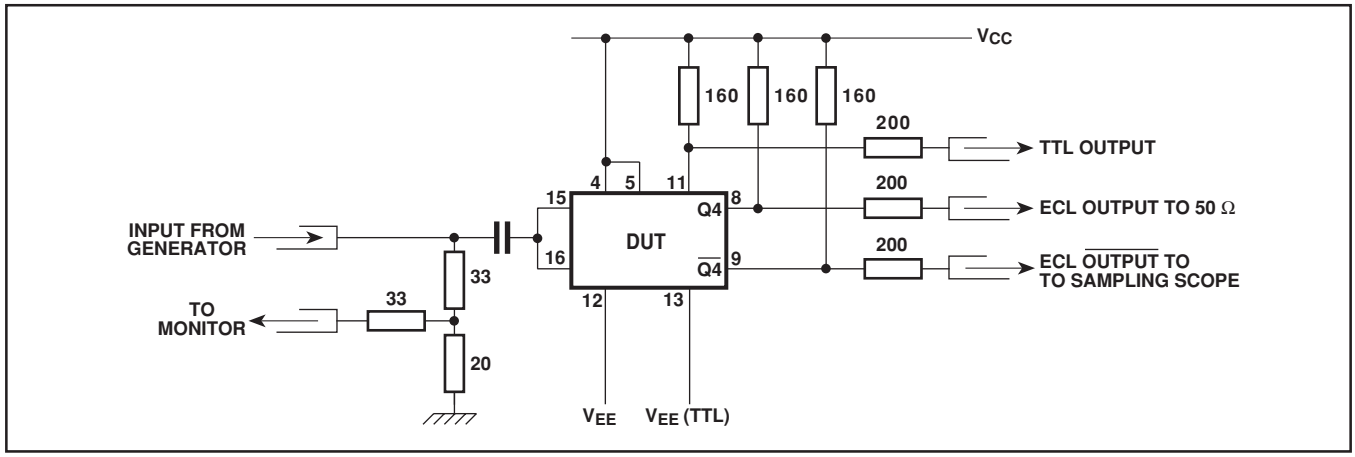


Fig. 6 Test circuit

OPERATING NOTES

1. The clock input, which is ECL10K compatible throughout the temperature range −55°C to +125°C, can also be coupled to TTL as shown in Fig. 9. The clock can also be capacitively coupled to the signal source (see Fig, 7). Connecting the internally-generated bias voltage to the clock input i.e., pin 15 to pin 16, centres the clock input about the switching threshold (see Fig. 8).
2. The two complementary outputs are ECL10K compatible but internal pulldown resistors are not included and therefore external pulldown resistors to V_{EE} are required.

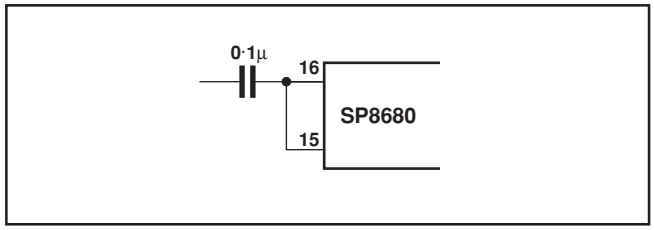


Fig. 7. AC coupled input

3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} pin should be left open circuit, reducing the power consumption by 20mW, typically.
4. Both control inputs (PE1 and PE2) are ECL10K compatible throughout the temperature range. Each control input is provided with a pullup resistor, the remote ends of which are connected to pins 6 and 7, respectively. This allows the pullup resistors to be unused if so desired or to be used to interface from TTL (see Fig. 9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit; alternatively, they can be connected to V_{EE} to act as pulldown resistors. When high, the master set input sets the divider to the eleventh state, is asynchronous and overrides the clock input.
5. All the inputs have internal 50kΩ pulldown resistors.
6. The circuit will operate down to DC but inputslew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig. 5.

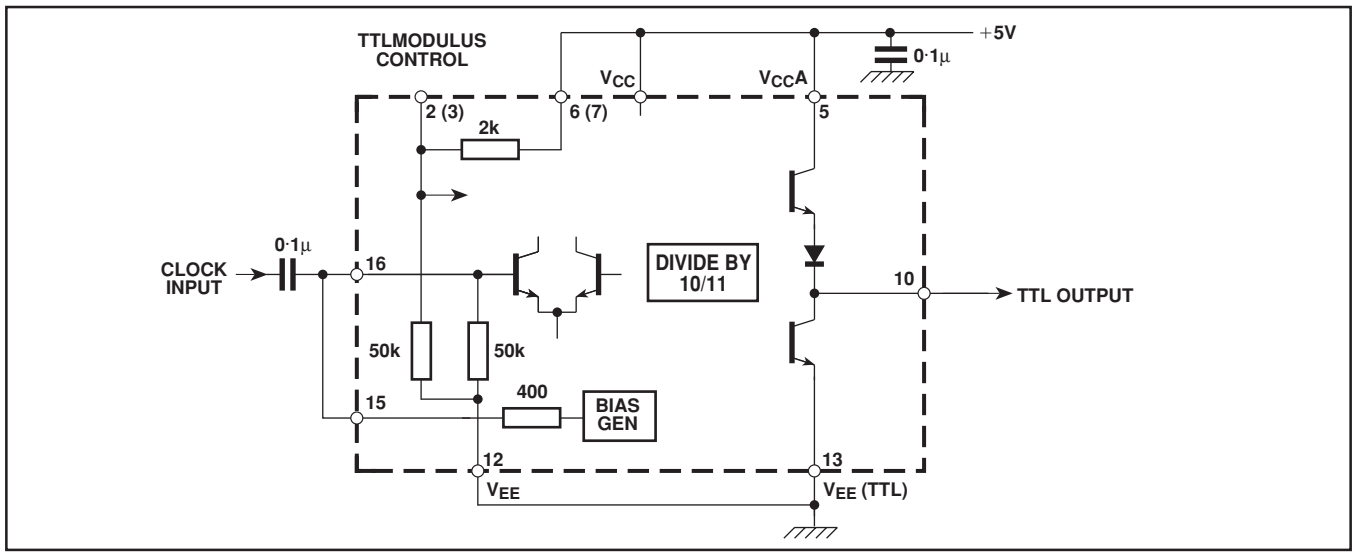


Fig. 8 Typical application showing TTL interfacing.

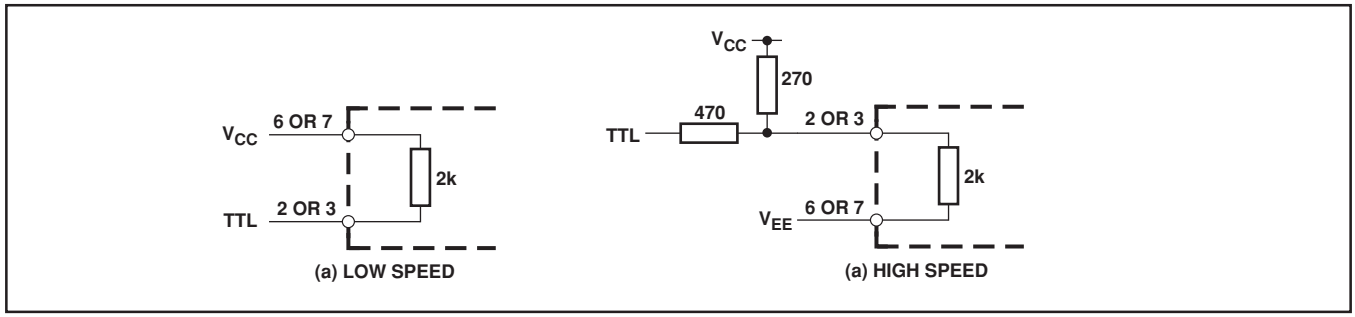


Fig. 9 TTL interface to PE1 and PE2

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