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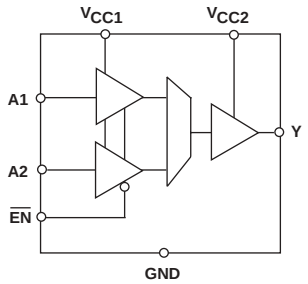
Low Voltage 2-1 Mux Level Translator

Preliminary Technical Data — ADG3232*

FEATURES
Operates from 1.65 V to 3.6 V Supply Rails
Uni-Direction Level Translation, Bidirectional Signal Path
Tiny 8 Lead SOT23 Package
Short Circuit Protection*
LVTTL/CMOS-Compatible Inputs

APPLICATIONS
Level Translation
Low Voltage ASIC translation
Low Voltage Clock Switching
Serial interface Translation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3232 is a Level Translator 2-1 Mux designed on a sub micron process which operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages allowing bi-directional level translation, i.e. it translates low voltages to higher voltages and vice versa. The signal path is uni-directional, data may only flow from A to Y.

This type of device may be used in applications requiring communication between devices operating from different supply levels.

The level translator mux is packaged in one of the smallest footprints available for its pin count. The 8 lead SOT23 package requires only 8.26mm^2 board space.

PRODUCT HIGHLIGHTS

1. Uni-Directional (Up/Down) Level Translation.
2. The device offers high performance and is fully guaranteed over a wide supply range; 1.65 V to 3.6 V.
3. Short Circuit Protection*
4. Tiny SOT23 package.

***Patent Pending**

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ADG3232–SPECIFICATIONS[1]

(V_{CC1} = V_{CC2} = +1.65 V to 3.6 V, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Units
LOGIC INPUTS/OUTPUTS[3]						
Input High Voltage	V_{IH}	V_{CC1} = 3.0 V to 3.6 V	1.35			V
		V_{CC1} = 2.3 V to 2.7 V	1.35			V
		V_{CC1} = 1.65 V to 1.95 V	0.65V_{CC}			V
Input Low Voltage	V_{IL}	V_{CC1} = 3.0 V to 3.6 V	-0.5		0.8	V
		V_{CC1} = 2.3 V to 2.7 V	-0.5		0.7	V
		V_{CC1} = 1.65 V to 1.95 V	-0.5		0.35V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = -100 µA, V_{CC2} = 3.0 V to 3.6 V	2.4			V
		V_{CC2} = 2.3 V to 2.7 V	2.0			V
		V_{CC2} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -4 mA, V_{CC2} = 2.3 V to 2.7 V	2.0			V
		V_{CC2} = 1.65 V to 1.95 V	V_{CC} - 0.45			V
		I_{OH} = -8 mA, V_{CC2} = 3.0 V to 3.6 V	2.4			V
Output Low Voltage	V_{OL}	I_{OH} = 100 µA, V_{CC2} = 3.0 V to 3.6 V	-0.5		0.4	V
		V_{CC2} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC2} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OH} = 4 mA, V_{CC2} = 2.3 V to 2.7 V	-0.5		0.4	V
		V_{CC2} = 1.65 V to 1.95 V	-0.5		0.45	V
		I_{OH} = 8 mA, V_{CC2} = 3.0 V to 3.6 V	-0.5		0.4	V
SWITCHINGS CHARACTERISTICS[4,5]						
Propagation Delay, t_{PD}						
A1 to Y	t_{PHL}, t_{PLH}	3.3 V ±0.3 V, C_L = 30 pF, V_T = V_{CC}/2			5	ns
A2 to Y	t_{PHL}, t_{PLH}	3.3 V ±0.3 V, C_L = 30 pF, V_T = V_{CC}/2			5	ns
A1 to Y	t_{PHL}, t_{PLH}	2.5 V ±0.2 V, C_L = 30 pF, V_T = V_{CC}/2			6	ns
A2 to Y	t_{PHL}, t_{PLH}	2.5 V ±0.2 V, C_L = 30 pF, V_T = V_{CC}/2			6	ns
A1 to Y	t_{PHL}, t_{PLH}	1.8 V ±0.15 V, C_L = 30 pF, V_T = V_{CC}/2			10	ns
A2 to Y	t_{PHL}, t_{PLH}	1.8 V ±0.15 V, C_L = 30 pF, V_T = V_{CC}/2			10	ns
ENABLE Time *EN* to Y	t_{EN}	3.3 V ±0.3 V, C_L = 30 pF, V_T = V_{CC}/2			6	ns
DISABLE Time *EN* to Y	t_{DIS}	3.3 V ±0.3 V, C_L = 30 pF, V_T = V_{CC}/2			6	ns
ENABLE Time *EN* to Y	t_{EN}	2.5 V ±0.2 V, C_L = 30 pF, V_T = V_{CC}/2			8	ns
DISABLE Time *EN* to Y	t_{DIS}	2.5 V ±0.2 V, C_L = 30 pF, V_T = V_{CC}/2			7	ns
ENABLE Time *EN* to Y	t_{EN}	1.8 V ±0.15 V, C_L = 30 pF, V_T = V_{CC}/2			12	ns
DISABLE Time *EN* to Y	t_{DIS}	1.8 V ±0.15 V, C_L = 30 pF, V_T = V_{CC}/2			11	ns
Input Leakage Current	I_I	0 ≤ V_{IN} ≤ 3.6 V			±1	µA
Output Leakage Current	I_O	0 ≤ V_{IN} ≤ 3.6 V			±1	µA
Input Capacitance[4]	C_{IN}	f = 1 MHz, V_{IN} = V_{CC} or GND		5		pF
Output Capacitance[4]	C_O	f = 1 MHz, V_{IN} = V_{CC} or GND		5		pF
Max Data Rate				TBD		Mbps
Jitter				TBD		ps
POWER REQUIREMENTS						
Power Supply Voltages	V_{CC1}		1.65		3.6	V
	V_{CC2}		1.65		3.6	V
Quiescent Power Supply Current	I_{CC1}	Digital Inputs = 0 V or V_{CC}			5	µA
	I_{CC2}	Digital Inputs = 0 V or V_{CC}			5	µA
Increase in I_{CC} per input	ΔI_{CC12}	V_{CC} = + 3.6 V, One input at 3.0 V; Others at V_{CC} or GND			100	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2] All typical vlaues are at V_{CC1} = V_{CC2}, T_A = +25°C unless otherwise stated.

[3] V_{IL} and V_{IH} levels are specified with respect to V_{CC1}, while V_{OH} and V_{OL} levels are with respect to V_{CC2}.

[3] Guaranteed by design, not subject to production test.

[4] See Test Circuits and Waveforms.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

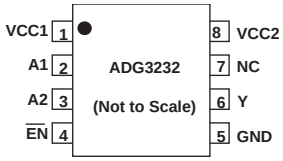
V_{CC} to GND ..... -0.5 V to +4.6 V
DC Input Voltage ..... -0.5 V to +4.6 V
DC Output Current 50mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
8 Lead SOT23,
θ_{JA} Thermal Impedance ..... 211°C/W
Lead Temperature, Soldering (10seconds) ..... 300°C
IR Reflow, Peak Temperature (<20 seconds) ... +235°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this speci•cation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PIN CONFIGURATIONS

8 Lead SOT23 Package (RJ-8)



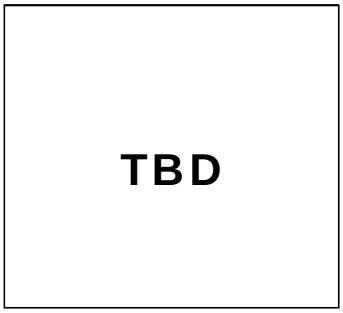
ORDERING GUIDE

Model	Temperature Range	Package Description	Branding	Package Option
ADG3232BRJ	–40°C to +85°C	SOT23	W3B	RJ-8

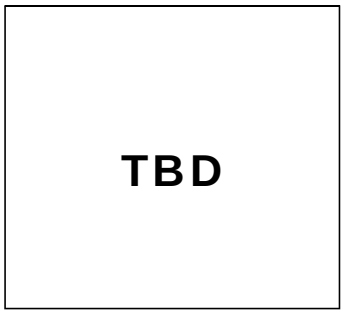
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3232 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

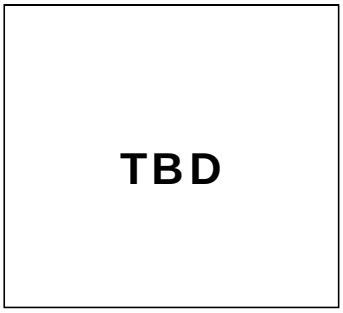
TYPICAL PERFORMANCE CHARACTERISTICS



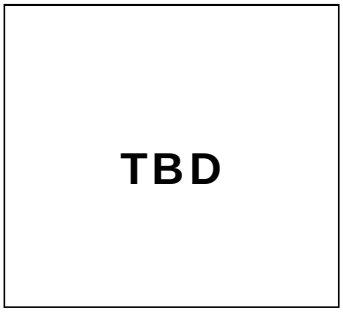
TPC 1. I_{CC} vs. Input Signal Frequency.



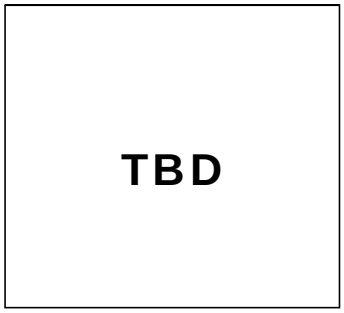
TPC 2. V_{CC} Supply vs temperature



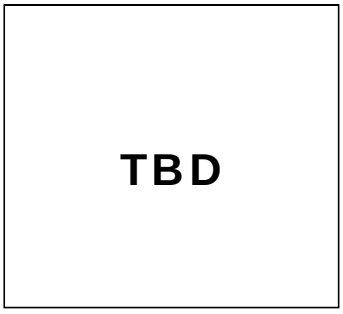
TPC 3. Rise/Fall time vs capacitive load



TPC 4. Propagation Delay vs Temperature



TPC 5. Propagation Delay vs Split Supply.



TPC 6. Propagation delay vs capacitive load

TEST CIRCUITS

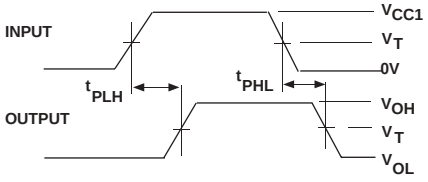


Figure 1. Propagation Delay

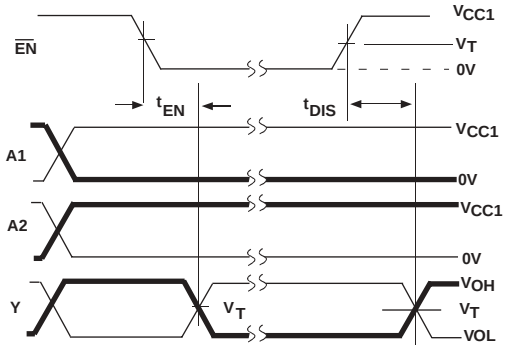


Figure 2. Enable & Disable Times

DESCRIPTION

The ADG3232 is a mux level translating device designed on a sub micron process which operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages allowing uni-directional level translation. The ADG3232 can translates low voltages to higher voltages and vice versa.

A1 & *EN* Input

The A1 and enable (*EN*) inputs have V_{IL}/V_{IH} logic levels so that it can accept logic levels of V_{OL}/V_{OH} from Device 0 or the controlling device independent of the value of the supply being used by the controlling device.

Operation

Figure 3 shows the ADG3232 in a typical application, the signal paths are from A1 or A2 to Y. The device will level translate the signal applied to A1/A2 from a V_{CC1} logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y output, which will have standard V_{OL}/V_{OH} levels for V_{CC2} supplies.

The supplies in Figure 3 may be any combination of supplies, i.e. V_{CC0}, V_{CC1} and V_{CC2} may be any combination of supplies, for example: 1.8, 2.5, 3.3V.

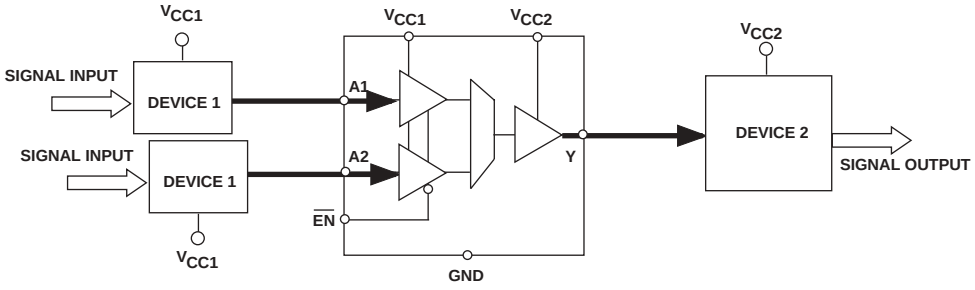


Figure 3. Typical Operation Circuit of the ADG3233

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8 Lead SOT23
(RJ-8)