MT6260 GSM/GPRS/EDGE-RX SOC Processor Technical Brief (Draft)

Version: 0.10
Release date: 2012-12-27

Document Revision History

Revision	Date	Author	Description
0.10	2012-12-27	Alisa Huang	Draft version

Table of Contents

Document Revision History **2**
Table of Contents **3**
Preface **5**
1 System Overview **6**
1.1 Platform Features 10
1.2 MODEM Features 11
1.3 GSM/GPRS/EDGE RF Features 12
1.4 Multimedia Features 13
1.5 Bluetooth Features 15
1.6 FM Features 16
1.7 General Descriptions 17
2 Product Descriptions **19**
2.1 Pin Description 19
2.2 Electrical Characteristics 40
2.3 Package Information 52
2.4 Ordering Information 56

Lists of Tables and Figures

Table 1. Pin coordinates 19
Table 2. Acronym for pin types 21
Table 3. PIN function description and power domain 21
Table 4. Acronym for state of pins 27
Table 5. State of pins 27
Table 6. Acronym for pull-up and pull-down types 31
Table 7. Capability of PU/PD, driving and Schmitt trigger 32
Table 8. Absolute maximum ratings for power supply 40
Table 9. Absolute maximum ratings for voltage input 41
Table 10. Absolute maximum ratings for storage temperature 41
Table 11. Recommended operating conditions for power supply 41
Table 12. Recommended operating conditions for voltage input 42
Table 13. Recommended operating conditions for operating temperature 42
Table 14. Electrical characteristics 42

Figure 1. Typical application of MT6260 9
Figure 2 MT6260 block diagram 18
Figure 3. Ball diagram and top view 19

Figure 4. IO types in state of pins 31
Figure 5. Outlines and dimension of TFBGA 9.6mm*8.6mm, 199-ball, 0.5 mm pitch package 55
Figure 6. Mass production top marking of MT6260 56

Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

1 System Overview

MT6260 is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT6260 is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS and EDGE-Rx capability. Based on the 32-bit ARM7EJ-S™ RISC processor, MT6260's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance GPRS/EDGE-Rx Class 12 MODEM application and leading-edge multimedia applications.

MT6260 also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in Figure 1.

Platform

MT6260 is capable of running the ARM7EJ-S™ RISC processor, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT6260 also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Memory

MT6260 supports serial flash interface with various operating frequencies.

Multimedia

The MT6260 multimedia subsystem provides conventional parallel interface and 2-bit serial interface for CMOS sensors. The camera resolution is up to 2M pixels. The software-based codec can be used to process various video types. Besides, MT6260 provides fancy UI capabilities through its hardware 2D accelerator. The 2D accelerator performs high-speed linear transformations with filtering. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT6260 is implemented with a high-performance audio synthesis technology, as well as a high-quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT6260 supports UART, USB 1.1 FS/LS , SDIO, HIF interface and MMC/SD storage systems. These interfaces provide MT6260 users with the highest level of flexibility in implementing high-end solutions.

To achieve a complete user interface, MT6260 also brings together all the necessary peripheral blocks for a multimedia GSM/GPRS/EDGE-RX phone. The peripheral blocks include the keypad scanner with the capability to detect multiple key presses, SIM controller, real-time clock, PWM, serial/parallel LCD controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT6260 architecture provides easy audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice band.

MT6260 supports AMR codec to adaptively optimize the quality of speech and audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

In addition, a 850mW class-AB amplifier is also embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS/EDGE-Rx radio

MT6260 integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6260 achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT6260 embeds a high-performance and completely integrated single-ended SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing one RF receiver and a fully integrated channel filter. With ultra-high dynamic range, the off-chip balun and SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

Bluetooth radio

MT6260 offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT6260 provides superior sensitivity and class 1 output power and thus ensures the quality of the connection with a wide range of Bluetooth devices.

MT6260 is fully compliant with Bluetooth v3.0 and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT6260 supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM radio subsystem provides a completely integrated FM Rx receiver supporting 87.5 ~ 108MHz FM bands with 50kHz tuning step. It also performs fast channel seek/scan algorithm to validate 200 carrier frequencies in 6 seconds. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which is usually an earphone, and auto-calibrated short antenna, which is usually a FPC short antenna or shared antenna with GSM for different application scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT6260 provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT6260 to provide rich features a high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT6260 offers various low-power features to help reduce the system power consumption. MT6260 is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT6260 device is offered in a 9.6mm×8.6mm, 199-ball, 0.5mm pitch, TFBGA package.

Figure 1. Typical application of MT6260

1.1 Platform Features

General

- Integrated voice-band, audio-band and base-band analog front-end
- Integrated full-featured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 15 DMA channels
- On-chip boot ROM for factory flash programming
- Watchdog timer for system crash recovery
- 4 sets of general-purpose timers
- Circuit switch data coprocessor
- Division coprocessor

Serial flash interfaces

- Supports various operating frequency combinations for serial flash
- Supports QPI and SPI serial flash

User interfaces

- 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 1 sets of Pulse Width Modulation (PWM) output
- 10 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 2 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications
- I2C master interface for peripheral management including image sensors
- SPI master interface for peripheral management including digital TV chips

Power management

- Li-ion battery charger
- 14 LDOs for the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 4 open-drain output switches to supply/control the LED
- LDO type vibrator
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out protection
- Over-voltage protection
- Different levels of power-down modes with sophisticated software control enables excellent power saving performance.

Test and debugging

- Built-in digital and analog loop back modes for both audio and baseband front-end
- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

1.2 MODEM Features

Radio interface and baseband front-end

- Digital PM data path with baseband front-end
- High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 4-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- Supports GSM/GPRS/EDGE-Rx modem
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS/EDGE-Rx GEA1, GEA2 and GEA3 ciphering
- GPRS packet switched data with CS1/CS2/CS3/CS4 coding schemes
- EDGE-Rx with MCS1-9 receiver coding schemes
- GSM circuit switch data
- GPRS/EDGE-Rx Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Two microphone inputs share one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2^{nd} order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

1.3 GSM/GPRS/EDGE RF Features

Receiver

- Quad band single-ended input LNAs
- Quadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 24dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs support quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS/EDGE-Rx applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

1.4 Multimedia Features

LCD/ WiFi interface

- Dedicated parallel interface supports 3 external devices with 8-bit for WiFi interface and 8-/9-bit for parallel LCD interface.

LCD controller

- Supports simultaneous connection to 2 parallel and 2 serial LCD modules
- LCM formats supported: RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 480x320
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- Motion JPEG encoder for video encoding
- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Hybrid MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
- ISO/IEC 14496-2 advanced simple profile:
- Supports visual tools for decoder: I-VOP, P-VOP, B-VOP, AC/DC prediction, 4-MV, unrestricted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports visual tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short header

H.264

- ISO/IEC 14496-10 baseline profile

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.
- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types
- Alpha blending with 7 rotation types, per-pixel alpha and pre-multiplied alpha
- Font drawing: Normal font and anti-aliasing font

- Linear transformation: Supports perspective transform, truncate/nearest/bi-linear sample filter.

Audio CODEC

- Supports HE-AAC codec decoding
- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter with digital MIC input support
- Stereo to mono conversion

1.5 Bluetooth Features

Radio features

- Fully compliant with Bluetooth specification 3.0 + EDR
- Low out-of-band spurious emissions support simultaneous operation with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 10dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

1.6 FM Features

- 76-108MHz worldwide FM bands with 50kHz tuning step
- Supports RDS/RBDS radio data system
- Supports long/short antenna
- 40ms seek time per channel, and 9sec search time for all channels(87.5~108MHz)
- Superior stereo noise reduction
- Soft mute volume control
- Supports short antenna, auto calibration for different FM channels
- 60dB SINAD with 22.5kHz FM deviation
- 3dBuVemf FM RX sensitivity with superior interference rejection
- 20dBuVemf RDS sensitivity (dev: 2kHz)
- More than 55dBc rejection capability against -200kHz ACI

1.7 General Descriptions

Figure 2**Error! Reference source not found.** is the block diagram of MT6260. Based on a multi-processor architecture, MT6260 integrates an ARM7EJ-S™ core, the main processor running high-level GSM/EDGE-Rx protocol software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control protocol and the Bluetooth radio control.

MT6260 consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S™ RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS/EDGE-Rx channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT6260.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

Details of the individual subsystems and blocks are described in the following chapters.

Figure 2 MT6260 block diagram

2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT6260, an TFBGA 9.6mm*8.6mm, 199-ball, 0.5mm pitch package is offered. Pin-outs and the top view are illustrated in **Figure 3** for this package.

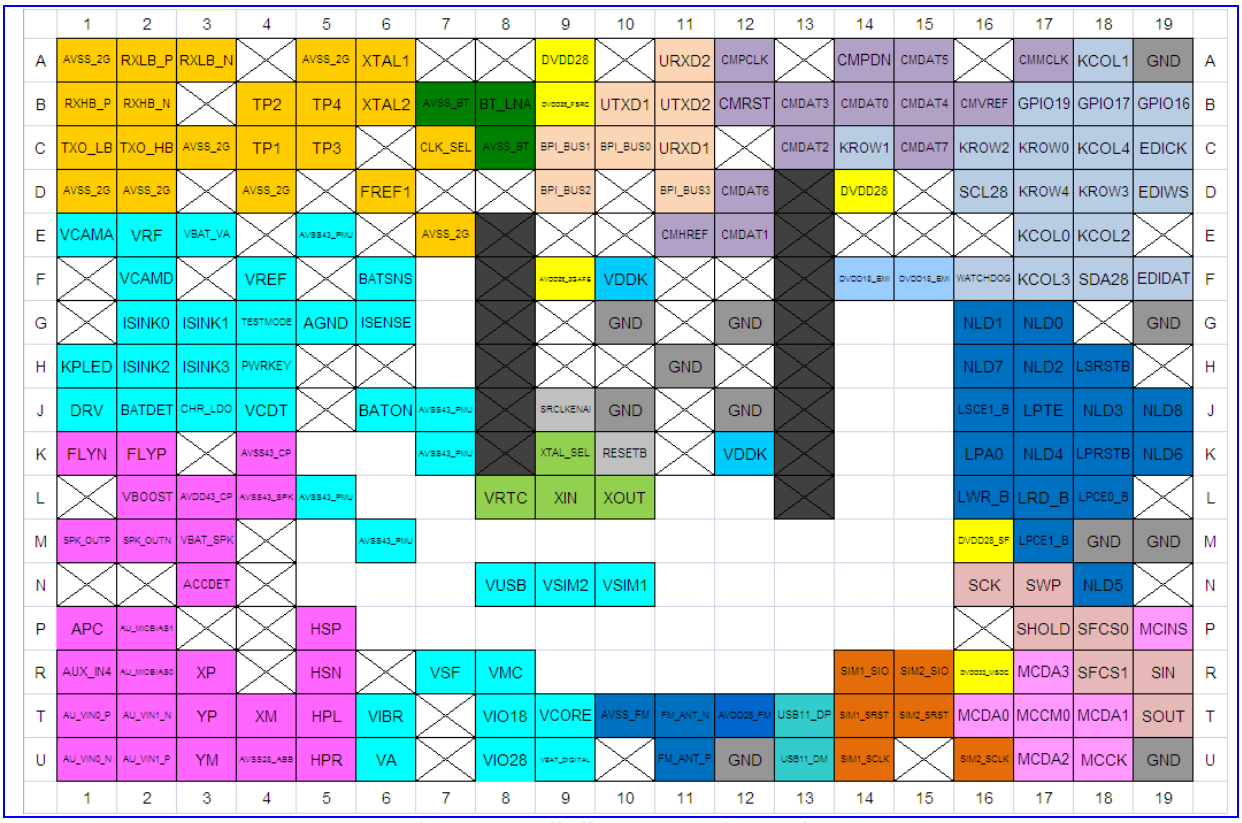


Figure 3. ***Ball diagram and top view***

2.1.2 Pin Coordination

Table 1. Pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	AVSS_2G	E5	AVSS43_PMU	M17	LPCE1_B
A11	URXD2	E7	AVSS_2G	M18	GND
A12	CMPCLK	F10	VDDK	M19	GND
A14	CMPDN	F14	DVDD18_EMI	M2	SPK_OUTN
A15	CMDAT5	F15	DVDD18_EMI	M3	VBAT_SPK
A17	CMMCLK	F16	WATCHDOG	M6	AVSS43_PMU
A18	KCOL1	F17	KCOL3	N10	VSIM1
A19	GND	F18	SDA28	N16	SCK
A2	RXLB_P	F19	EDIDAT	N17	SWP
A3	RXLB_N	F2	VCAMD	N18	NLD5

Pin#	Net name	Pin#	Net name	Pin#	Net name
A5	AVSS_2G	F4	VREF	N3	ACCDET
A6	XTAL1	F6	BATSNS	N8	VUSB
A9	DVDD28	F9	AVDD28_2GAFE	N9	VSIM2
B1	RXHB_P	G10	GND	P1	APC
B10	UTXD1	G12	GND	P17	SHOLD
B11	UTXD2	G16	NLD1	P18	SFCS0
B12	CMRST	G17	NLD0	P19	MCINS
B13	CMDAT3	G19	GND	P2	AU_MICBIAS1
B14	CMDAT0	G2	ISINK0	P5	HSP
B15	CMDAT4	G3	ISINK1	R1	AUX_IN4
B16	CMVREF	G4	TESTMODE	R14	SIM1_SIO
B17	GPIO19	G5	AGND	R15	SIM2_SIO
B18	GPIO17	G6	ISENSE	R16	DVDD33_MSDC
B19	GPIO16	H1	KPLED	R17	MCDA3
B2	RXHB_N	H11	GND	R18	SFCS1
B4	TP2	H16	NLD7	R19	SIN
B5	TP4	H17	NLD2	R2	AU_MICBIAS0
B6	XTAL2	H18	LSRSTB	R3	XP
B7	AVSS_BT	H2	ISINK2	R5	HSN
B8	BT_LNA	H3	ISINK3	R7	VSF
B9	DVDD28_FSRC	H4	PWRKEY	R8	VMC
C1	TXO_LB	J1	DRV	T1	AU_VIN0_P
C10	BPI_BUS0	J10	GND	T10	AVSS_FM
C11	URXD1	J12	GND	T11	FM_ANT_N
C13	CMDAT2	J16	LSCE1_B	T12	AVDD28_FM
C14	KROW1	J17	LPTE	T13	USB11_DP
C15	CMDAT7	J18	NLD3	T14	SIM1_SRST
C16	KROW2	J19	NLD8	T15	SIM2_SRST
C17	KROW0	J2	BATDET	T16	MCDA0
C18	KCOL4	J3	CHR_LDO	T17	MCCM0
C19	EDICK	J4	VCDT	T18	MCDA1
C2	TXO_HB	J6	BATON	T19	SOUT
C3	AVSS_2G	J7	AVSS43_PMU	T2	AU_VIN1_N
C4	TP1	J9	SRCLKENAI	T3	YP
C5	TP3	K1	FLYN	T4	XM
C7	CLK_SEL	K10	RESETB	T5	HPL
C8	AVSS_BT	K12	VDDK	T6	VIBR
C9	BPI_BUS1	K16	LPA0	T8	VIO18
D1	AVSS_2G	K17	NLD4	T9	VCORE
D11	BPI_BUS3	K18	LPRSTB	U1	AU_VIN0_N
D12	CMDAT6	K19	NLD6	U11	FM_ANT_P
D14	DVDD28	K2	FLYP	U12	GND
D16	SCL28	K4	AVSS43_CP	U13	USB11_DM
D17	KROW4	K7	AVSS43_PMU	U14	SIM1_SCLK
D18	KROW3	K9	XTAL_SEL	U16	SIM2_SCLK
D19	EDIWS	L10	XOUT	U17	MCDA2

Pin#	Net name	Pin#	Net name	Pin#	Net name
D2	AVSS_2G	L16	LWR_B	U18	MCCK
D4	AVSS_2G	L17	LRD_B	U19	GND
D6	FREF1	L18	LPCE0_B	U2	AU_VIN1_P
D9	BPI_BUS2	L2	VBOOST	U3	YM
E1	VCAMA	L3	AVDD43_CP	U4	AVSS28_ABB
E11	CMHREF	L4	AVSS43_SPK	U5	HPR
E12	CMDAT1	L5	AVSS43_PMU	U6	VA
E17	KCOL0	L8	VRTC	U8	VIO28
E18	KCOL2	L9	XIN	U9	VBAT_DIGITAL
E2	VRF	M1	SPK_OUTP		
E3	VBAT_VA	M16	DVDD28_SF		

2.1.3 Detailed Pin Description

Table 2. Acronym for pin types

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. PIN function description and power domain

Pin name	Type	Description	Power domain
System			
RESETB	DIO	System reset	DVDD18
SRCLKENAI	DIO	26MHz clock request by external devices	DVDD18
GPIO16	DIO	General purpose input /output 16	DVDD18
GPIO17	DIO	General purpose input /output 17	DVDD18
GPIO19	DIO	General purpose input /output 19	DVDD18
EDI interface			
EDICK	DIO	I2S clock	DVDD18
EDIDATA	DIO	I2S data	DVDD18
EDIWS	DIO	I2S word sync	DVDD18
RF control circuitro			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28

Pin name	Type	Description	Power domain
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
BPI_BUS3	DIO	RF hard-wire control bus bit 3	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
URXD2	DIO	UART2 receive data	DVDD28
UTXD2	DIO	UART2 transmit data	DVDD28
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	Keypad column 1	DVDD28
KCOL2	DIO	Keypad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad column 4	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28
CMPDN	DIO	CMOS sensor power down control	DVDD28
CMVREF	DIO	CMOS sensor vertical reference signal input	DVDD28
CMHREF	DIO	CMOS sensor horizontal reference signal input	DVDD28
CMDAT0	DIO	CMOS sensor data input 0	DVDD28
CMDAT1	DIO	CMOS sensor data input 1	DVDD28
CMDAT2	DIO	CMOS sensor data input 2	DVDD28
CMDAT3	DIO	CMOS sensor data input 3	DVDD28
CMDAT4	DIO	CMOS sensor data input 4	DVDD28
CMDAT5	DIO	CMOS sensor data input 5	DVDD28
CMDAT6	DIO	CMOS sensor data input 6	DVDD28
CMDAT7	DIO	CMOS sensor data input 7	DVDD28
CMPCLK	DIO	CMOS sensor master clock output	DVDD28
CMMCLK	DIO	CMOS sensor master clock output	DVDD28
MS/SD card interface			
MCINS	DIO	SD card detect Input	DVDD18_EMI
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA1	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA2	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC

Pin name	Type	Description	Power domain
MCDA3	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data input/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card clock output	VSIM2
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
LCD interface			
LSRSTB	DIO	Serial display interface reset signal	DVDD18_EMI
LSCE1_B	DIO	Serial display interface chip select 1 output	DVDD18_EMI
LPCE1_B	DIO	Parallel display interface chip select 1 output	DVDD18_EMI
LPCE0_B	DIO	Parallel display interface chip select 0 output	DVDD18_EMI
LPTE	DIO	Parallel display interface tearing effect	DVDD18_EMI
LPRSTB	DIO	Parallel display interface reset signal	DVDD18_EMI
LRD_B	DIO	Parallel display interface read strobe	DVDD18_EMI
LPA0	DIO	Parallel display interface address output	DVDD18_EMI
LWR_B	DIO	Parallel display interface write strobe	DVDD18_EMI
NLD8	DIO	Parallel LCD data 8	DVDD18_EMI
NLD7	DIO	Parallel LCD data 7	DVDD18_EMI
NLD6	DIO	Parallel LCD data 6	DVDD18_EMI
NLD5	DIO	Parallel LCD data 5	DVDD18_EMI
NLD4	DIO	Parallel LCD data 4	DVDD18_EMI
NLD3	DIO	Parallel LCD data 3	DVDD18_EMI
NLD2	DIO	Parallel LCD data 2	DVDD18_EMI
NLD1	DIO	Parallel LCD data 1	DVDD18_EMI
NLD0	DIO	Parallel LCD data 0	DVDD18_EMI
Watchdog reset			
WATCHDOG	DIO	Reset external memory device	DVDD18_EMI
General purpose I/O interface			
SFCS1	DIO	General purpose input/output 66	DVDD28_SF

Pin name	Type	Description	Power domain
SFCS0	DIO	General purpose input/output 68	DVDD28_SF
SFIN	DIO	General purpose input/output 70	DVDD28_SF
SFOUT	DIO	General purpose input/output 71	DVDD28_SF
SFSHOLD	DIO	General purpose input/output 72	DVDD28_SF
SFWP	DIO	General purpose input/output 67	DVDD28_SF
SFCK	DIO	General purpose input/output 69	DVDD28_SF
FM			
RXLNA_INN_LA	AI	FM input from long antenna	AVDD28_FM
RXLNA_INP_LA	AI	FM input from long antenna	AVDD28_FM
RXLNA_INN_SA	AI	FM input from short antenna	AVDD28_FM
RXLNA_INP_SA	AI	FM input from short antenna	AVDD28_FM
Bluetooth			
BTRF2P4G_N	AIO	Bluetooth RF single-ended input	-
BTREXT	AIO	Bluetooth external reference resistor	-
2G RF			
RXHB_P	AIO	Differential RF input for highband Rx (DCS/PCS)	-
RXHB_N	AIO	Differential RF input for highband Rx (DCS/PCS)	-
RXLB_P	AIO	Differential RF input for lowband Rx (GSM900/GSM850)	-
RXLB_N	AIO	Differential RF input for lowband Rx (GSM900/GSM850)	-
TXO_HB	AIO	RF output for highband Tx (DCS/PCS)	-
TXO_LB	AIO	RF output pin for lowband Tx (GSM900/GSM850)	-
FREF1	AIO	DCXO reference clock output	-
FREF2	AIO	DCXO reference clock output	
XTAL1	AIO	Input 1 for DCXO crystal	-
XTAL2	AIO	Input 2 for DCXO crystal	-
TP1	AIO	Test pin 1	-
TP2	AIO	Test pin 2	-
TP3	AIO	Test pin 3	-
TP4	AIO	Test pin 4	-
CLK_SEL	AIO	DCXO mode selection	-
USB			
USB11_DM	AIO	D- data input/output	-
USB11_DP	AIO	D+ data input/output	-
Analog baseband			
HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
HSP	AIO	Voice handset output (positive)	AVDD28_ABB
HSN	AIO	Voice handset output (negative)	AVDD28_ABB

Pin name	Type	Description	Power domain
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	AVDD28_ABB
SPK_OUTN	AIO	Speaker negative output	AVDD28_ABB
APC	AIO	Automatic power control DAC output	AVDD28_ABB
XP	AIO	Touch panel X-axis positive input	AVDD28_ABB
XM	AIO	Touch panel X-axis negative input	AVDD28_ABB
YP	AIO	Touch panel Y-axis positive input	AVDD28_ABB
YM	AIO	Touch panel Y-axis negative input	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
AU_MICBIAS1	AIO	Microphone bias source 1	AVDD28_ABB
ACCDET	AIO	Accessory detection	AVDD28_ABB
Real-time clock			
XIN	AIO	Input pin for 32K crystal	VRTC
XOUT	AIO	Input pin for 32K crystal	VRTC
XTAL_SEL	DIO	Pin option for external 32K crystal	VRTC
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VBT	AIO	LDO output for BTRF - VBT	VBAT_RF
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_ANALOG
VCAMD	AIO	LDO output for sensor - VCAMD	VBAT_DIGITAL
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_DIGITAL
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VTCXO	AIO	LDO output for DCXO - VTCXO	VBAT_ANALOG
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS

Pin name	Type	Description	Power domain
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHR_LDO	AIO	2.8V shunt-regulator output	BATSNS
BATDET	AIO	Battery detection pin	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_SPK
ISINK1	AIO	Backlight driver channel 1	VBAT_SPK
ISINK2	AIO	Backlight driver channel 2	VBAT_SPK
ISINK3	AIO	Backlight driver channel 3	VBAT_SPK
KPLED	AIO	Keypad led driver	VBAT_SPK
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
Analog power			
AVDD28_FM	P	FM power	-
AVDD28_VRF	P	2.8V power supply for 2G RF	-
AVDD28_TCXO	P	2.8V power supply for 2G TCXO	-
AVDD28_2GAFE	P	2.8V power supply for 2G AFE	-
AVDD28_ABB	P	ABB 2.8V power	-
AVDD28_DBT	P	2.8V power supply for DBT	-
AVDD28_ABT	P	2.8V power supply for ABT	-
VBAT_RF	P	RF LDOs used battery voltage input	-
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_ANALOG	P	Analog LDOs used battery voltage input	-
VBAT_SPK	P	VBAT input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_BT	G	BT ground	-
AVSS_BT1	G	BT1 ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-
AVSS43_PMU	G	PMU ground	-
AVSS43_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
Digital power			
DVDD28	P	2.8V power supply for digital macros in transceiver	-
DVDD18	P	1.8V power supply for digital macros in transceiver	-
DVDD28_FSRC	P	E-FUSE blowing power control	-
DVDD33_MSDC	P	3.3V memory card power	-
DVDD18_EMI	P	1.8V EMI IO power	-
DVDD28_SF	P	2.8V IO power	-

Pin name	Type	Description	Power domain
DVDD28_SFP	P	2.8V IO power	-
VDDK	P	1.2V core power	
Digital ground			
GND	G	Ground	-

Table 4. Acronym for state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 5. State of pins

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
System						
RESETB	O	1	-	DIOH6/DIOL6	No need	IO Type 6
SRCLKENAI	I	7	PD	DIOH6/DIOL6	No need	IO Type 6
GPIO16	I	1	PD	DIOH2/DIOL2	No need	IO Type 1
GPIO17	I	1	PD	DIOH2/DIOL2	No need	IO Type 1
GPIO19	I	1	PD	DIOH2/DIOL2	No need	IO Type 1
EDI interface						
EDICK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EDIDAT	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EDIWS	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
RF control circuitry						
BPI_BUS0	O	1	-	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS1	I	1	PD	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS2	O	1	-	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS3	I	1	PD	DIOH1/DIOL1	No need	IO Type 1

[1] The column “State” of “Reset” shows the pin state during reset. (Input, High Output, Low Output, etc)

[2] The column “Aux” for “Reset” means the default aux function number, shown in the table “Pin Multiplexing, Capability and Settings”.

[3] The column “PU/PD” for “Reset” means if there is internal pull-up or pull-down when the pin is input in the reset state.

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type 3
UTXD1	O	1	-	DIOH1/DIOL1	No need	IO Type 1
URXD2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
UTXD2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL1	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL2	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL3	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL4	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KROW0	O	0	-	DIOH5/DIOL5	No need	IO Type 5
KROW1	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW2	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW3	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW4	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
Camera interface						
CMRST	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMPDN	O	0	-	DIOH1/DIOL1	No need	IO Type 1
CMVREF	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GMHREF	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT0	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT1	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT3	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT4	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT5	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT6	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT7	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMPCLK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMMCLK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
MS/SD card interface						
MCINS	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA2	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA3	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCCM	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCMM0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
I2C interface						
SCL28	I	0	PD	DIOH1/DIOL1	No need	IO Type 1

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
SDA28	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
LCD interface						
LSRSTB	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LSCE1B	O	1	-	DIOH2/DIOL2	No need	IO Type 2
LPCE0B	O	1	-	DIOH2/DIOL2	No need	IO Type 7
LPCE1B	O	1	-	DIOH2/DIOL2	No need	IO Type 2
LPTE	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LPRSTB	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LRD_B	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
LPA0	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
LWR_B	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
NLD8	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD7	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD6	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD5	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD4	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD3	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD2	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD1	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
NLD0	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
Watchdog reset						
WATCHDOG	O	1	-	DIOH1/DIOL1	No need	IO Type 1
General purpose I/O interface						
SFCS0	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SFCS1	I	0	PD	DIOH7/DIOL7	No need	IO Type 7
SFIN	I	1	PU	DIOH7/DIOL7	No need	IO Type 7
SFOUT	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SFSHOLD	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SFWP	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SFCK	O	1	-	DIOH7/DIOL7	No need	IO Type 7

Figure 4. ***IO types in state of pins***

2.1.4 Pin Multiplexing, Capability and Settings

Table 6. ***Acronym for pull-up and pull-down types***

Abbreviation	Description
PU	Pull-up, not controllable

Abbreviation	Description
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7. Capability of PU/PD, driving and Schmitt trigger

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
EDICK	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDICK	O	-	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT0	I	-	4, 8, 12, 16mA	0
EDIDAT	0	GPIO61	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDIDAT	IO	CU, CD	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT8	I	-	4, 8, 12, 16mA	0
EDIWS	0	GPIO18	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDIWS	O	-	4, 8, 12, 16mA	0
GPIO16	0	GPIO16	IO	CU, CD	4, 8, 12, 16mA	0
	1	GPSFSYNC	O	-	4, 8, 12, 16mA	0
GPIO17	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS5	O	-	4, 8, 12, 16mA	0
GPIO19	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS4	O	-	4, 8, 12, 16mA	0
SCL28	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPISCK0	O	-	4, 8, 12, 16mA	0
	5	D1_ICK	I	PD	4, 8, 12, 16mA	0
SDA28	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPICS0	O	-	4, 8, 12, 16mA	0
	5	D1_IMS	I	CU, CD	4, 8, 12, 16mA	0
KCLO4	0	GPIO5	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	CU, CD	4, 8, 12, 16mA	0
	3	EINT1	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	5	JDI	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJDI	I	CU, CD	4, 8, 12, 16mA	0
KCOL3	0	GPIO6	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2CK	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
KCOL2	0	GPIO7	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0
KCOL1	0	GPIO8	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL1	IO	CU, CD	4, 8, 12, 16mA	0
KCOL0	0	GPIO9	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCLO0	IO	CU, CD	4, 8, 12, 16mA	0
KROW4	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2WS	O	-	4, 8, 12, 16mA	0
	3	EINT3	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
KROW3	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2DAT	O	-	4, 8, 12, 16mA	0
	4	FMJTDO	O	-	4, 8, 12, 16mA	0
	5	JTDO	O	-	4, 8, 12, 16mA	0
	6	BTJTDO	O	-	4, 8, 12, 16mA	0
KROW2	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	CU, CD	4, 8, 12, 16mA	0
	5	JTRCK	O	-	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	-	4, 8, 12, 16mA	0
KROW1	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	5	DI_IDA	IO	PU, CD	4, 8, 12, 16mA	0
	6	BTDBGIN	I	CU, CD	4, 8, 12, 16mA	0
KROW0	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	CU, CD	4, 8, 12, 16mA	0
	2	LSDI0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO6	O	-	4, 8, 12, 16mA	0
	5	LSCK0	O	-	4, 8, 12, 16mA	0
URXD2	0	GPIO20	IO	CU, CD	4, 8, 12, 16mA	0
	1	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	2	U1RTS	O	-	4, 8, 12, 16mA	0
	3	BTPRI	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPIMISI0	O	-	4, 8, 12, 16mA	0
UTXD2	0	GPIO24	IO	CU, CD	4, 8, 12, 16mA	0
	1	U2TXD	O	-	4, 8, 12, 16mA	0
	2	U1CTS	I	PU	4, 8, 12, 16mA	0
	3	CLKO0	O	-	4, 8, 12, 16mA	0
	4	SPIMISO0	I	PD	4, 8, 12, 16mA	0
URXD1	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	4	EINT4	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	-	4, 8, 12, 16mA	0
MCINS	0	GPIO24	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	EINT5	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
MCCK	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	IO	CU, CD	4, 8, 12, 16mA	0
	5	JRTCK	O	-	4, 8, 12, 16mA	0
MCDA0	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	CU, CD	4, 8, 12, 16mA	0
MCDA1	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
MCDA2	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	5	JTDI	I	CU, CD	4, 8, 12, 16mA	0
MCDA3	0	GPIO4	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDO	O	-	4, 8, 12, 16mA	0
	5	JTDO	O	-	4, 8, 12, 16mA	0
NLD8	0	GPIO28	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD8	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMMCLK	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD7	0	GPIO29	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD7	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSK	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD6	0	GPIO30	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD6	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMRST	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD5	0	GPIO31	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD5	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSD0	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD4	0	GPIO32	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD4	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMPDN	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD3	0	GPIO33	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD3	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSDI3	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSD1	I	CU,CD	2,4,6,8,10,12 ,14,16mA	0
NLD2	0	GPIO34	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD2	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD1	0	GPIO35	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD1	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	SFWP	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD0	0	GPIO36	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD0	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSA0DA0	O	-	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	3	SFCS0	O	-	2,4,6,8,10,12 ,14,16mA	0
LWR_B	0	GPIO37	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LWRB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LSCK0	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	SFCK	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LRD_B	0	GPIO38	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LRDB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LSDA0	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	SFIN	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPA0	0	GPIO39	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPA0	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LSDI0	I	PD	2,4,6,8,10,12 ,14,16mA	0
	3	SFOUT	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPCE0_B	0	GPIO40	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE0B	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSCE0B1	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	SFHOLD	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSCE1_B	0	GPIO41	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	DAISYNC	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	SCL	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPCE1_B	0	GPIO42	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LPTE1	I	CU,CD	2,4,6,8,10,12 ,14,16mA	0
	3	SDA	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSRSTB	0	GPIO43	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
WATCHDOG	0	GPIO44	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	WATCHDOG	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LPCE2B	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	EINT6	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPTE	0	GPIO45	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	CLKO1	O	-	2,4,6,8,10,12 ,14,16mA	0
LPRSTB	0	GPIO46	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	2	LPSRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
	4	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	LPCE3B	O	-	2,4,6,8,10,12 ,14,16mA	0
CMDAT0	0	GPIO47	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT0	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
CMDAT1	0	GPIO48	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT1	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
CMDAT2	0	GPIO49	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT2	I	CU, CD	4, 8, 12, 16mA	0
	2	SCL	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0
CMDAT3	0	GPIO50	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT3	I	CU, CD	4, 8, 12, 16mA	0
	2	LRSTB	O	-	4, 8, 12, 16mA	0
	3	MC3DA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	DAICLK	O	-	4, 8, 12, 16mA	0
	5	JTRCK	O	-	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	-	4, 8, 12, 16mA	0
CMDAT4	0	GPIO51	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT4	I	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA1	O	-	4, 8, 12, 16mA	0
	3	MC3DA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTRST_B	I	CU, CD	4, 8, 12, 16mA	0
CMDAT5	0	GPIO52	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	CMDAT5	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCK5	O	-	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	-	4, 8, 12, 16mA	0
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND48	I	PD	4, 8, 12, 16mA	0
CMDAT6	0	GPIO53	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT6	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA1	IO	PU, CD	4, 8, 12, 16mA	0
	3	MC2DA2	O	-	4, 8, 12, 16mA	0
	4	DAIPCMIN	I	-	4, 8, 12, 16mA	0
CMDAT7	0	GPIO54	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT7	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDI1	I	CU, CD	4, 8, 12, 16mA	0
	3	MCDA3	O	-	4, 8, 12, 16mA	0
	4	DAIPCMOUT	I	CU, CD	4, 8, 12, 16mA	0
CMHREF	0	GPIO55	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMHREF	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCE0B1	I	CU, CD	4, 8, 12, 16mA	0
	3	MC3CK	I	CU, CD	4, 8, 12, 16mA	0
	4	DAISYNC	O	-	4, 8, 12, 16mA	0
CMVREF	0	GPIO56	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMVREF	I	CU, CD	4, 8, 12, 16mA	0
	2	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	3	EINT7	I	PD	4, 8, 12, 16mA	0
	4	DAIRST	I	PD	4, 8, 12, 16mA	0
	5	LPTE0	I	PD	4, 8, 12, 16mA	0
CMPDN	0	GPIO57	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	-	4, 8, 12, 16mA	0
CMMCLK	0	GPIO58	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMMCLK	O	-	4, 8, 12, 16mA	0
CMPCLK	0	GPIO59	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPCLK	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
CMRST	0	GPIO60	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	-	4, 8, 12, 16mA	0
EDIDAT	0	GPIO61	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	EDIDAT	IO	CU,CD	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT8	I	CU,CD	4, 8, 12, 16mA	0
BPI_BUS3	0	GPIO62	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS3	O	-	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO63	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS2	O	-	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO64	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS1	O	-	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO65	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS0	O	-	4, 8, 12, 16mA	0
SFSCK	0	GPIO69	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSCK	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2DA1	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSWP	0	GPIO67	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSWP	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2CK	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSHOLD	0	GPIO72	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSHOLD	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2DA3	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSCS0	0	GPIO68	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSCS0	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2DA1	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSCS1	0	GPIO66	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSCS1	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSIN	0	GPIO70	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSIN	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2DA2	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSOUT	0	GPIO71	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSOUT	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	MC2MC0	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SIM1_SIO	0	GPIO73	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSIO	IO	CU, CD	2, 4, 6, 8mA	0
SIM1_SRST	0	GPIO74	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSRST	IO	CU, CD	2, 4, 6, 8mA	0
SIM2_SIO	0	GPIO75	IO	CU, CD	2, 4, 6, 8mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	SIM2SIO	IO	CU, CD	2, 4, 6, 8mA	0
SIM1_SCLK	0	GPIO76	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSCLK	IO	CU, CD	2, 4, 6, 8mA	0
SIM2_SCLK	0	GPIO77	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2SCLK	IO	CU, CD	2, 4, 6, 8mA	0
SIM2_SRST	0	GPIO78	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2SRST	IO	CU, CD	2, 4, 6, 8mA	0
SRCLKENAI	0	GPIO105	IO	CU, CD	4, 8, 12, 16mA	0
	1	SRCLKENAI	I	CU, CD	4, 8, 12, 16mA	0
RESETB	0	GPIO106	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND70	I	PD	4, 8, 12, 16mA	0
EINT12	0	GPIO107	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT12	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND71	I	PD	4, 8, 12, 16mA	0

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 8. ***Absolute maximum ratings for power supply***

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.3	V
VBAT_ANALOG	Analog used battery voltage input	-0.3	+4.3	V
VBAT_SPK	VBAT input for loud speaker driver	-0.3	+4.3	V
VBAT_RF	RF used battery voltage input	-0.3	+4.3	V
VUSB	LDO output for USB-VUSB	+3.0	+3.6	V
AVDD28_FM	2.8V power supply for FM	+2.52	+3.08	V
AVDD28_VRF	2.8V power supply for 2G RF	+2.52	+3.08	V
AVDD28_TCXO	2.8V power supply for 2G TCXO	+2.52	+3.08	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	+2.52	+3.08	V
AVDD28_ABB	2.8V power supply for ABB	+2.52	+3.08	V
AVDD28_DBT	2.8V power supply for DBT	+2.52	+3.08	V
AVDD28_ABT	2.8V power supply for ABT	+2.52	+3.08	V
DVDD28	2.8V power supply for digital macros in transceiver	+2.52	+3.08	V
DVDD18	1.8V power supply for digital macros in transceiver	+1.62	+1.98	V

Symbol or pin name	Description	Min.	Max.	Unit
DVDD28_SF	2.8V IO power	+2.7	+3.6	V
	1.8V IO power	+1.7	+1.98	V
DVDD33_MSDC	3.3V memory card power	+3.0	+3.6	V
DVDD18_EMI	1.8V EMI IO power	+1.62	+1.98	V
DVDD28_FSRC	E-FUSE blowing power control	+2.52	+3.08	V
VDDK	1.3v core power	+1.17	+1.43	V

Table 9. ***Absolute maximum ratings for voltage input***

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.08	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V

Table** 10.* ***Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	^{o}C

2.2.2 Recommended Operating Conditions

Table 11. ***Recommended operating conditions for power supply***

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_ANALOG	Analog used battery voltage input	3.4	3.8	4.2	V
VBAT_SPK	VBAT input for loud speaker driver	3.4	3.8	4.2	V
VBAT_RF	RF used battery voltage input	3.4	3.8	4.2	V
VUSB	LDO output for USB-VUSB	3.0	3.3	3.6	V
AVDD28_FM	2.8V power supply for FM	2.6	2.8	3.0	V
AVDD28_VRF	2.8V power supply for 2G RF	2.65	2.8	2.95	V
AVDD28_TCXO	2.8V power supply for 2G TCXO	2.65	2.8	2.95	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	2.65	2.8	2.95	V
AVDD28_ABB	2.8V power supply for ABB	2.6	2.8	3.0	V
AVDD28_DBT	2.8V power supply for DBT	2.6	2.8	3.0	V
AVDD28_ABT	2.8V power supply for ABT	2.6	2.8	3.0	V
DVDD28	2.8V power supply for digital macros in transceiver	2.7	2.8	2.9	V

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18	1.8V power supply for digital macros in transceiver	1.62	1.8	1.98	V
DVDD28_SF	2.8V IO power	2.7	3.3	3.6	V
	1.8V IO power	1.7	1.8	1.98	
DVDD33_MSDC	3.3V memory card power	3.0	3.3	3.6	V
DVDD18_EMI	1.8V EMI IO power	1.62	1.8	1.98	V
DVDD28_FSRC	E-FUSE blowing powr control	2.7	2.8	3.08	V
VDDK	1.2v core power	1.17	1.3	1.43	VDDK

Table 12. ***Recommended operating conditions for voltage input***

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital input voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digital input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V
VIN7	Digital input voltage for IO Type 7	-0.3	-	DVDIO+0.3	V

Table 13. ***Recommended operating conditions for operating temperature***

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	^{o}C

2.2.3 Electrical Characteristics under Recommended Operating Conditions

Table 14. ***Electrical characteristics***

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-5	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN2<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down	DVDIO = 2.8V	40	85	190	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	resistance for IO Type 2	DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0.8	-	35	
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital high output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-0.8	-	35	
DIIL4	Digital low input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-9.3	-	11.4	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU4 200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DRPD4 200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH5	Digital high input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-5	-	5	μA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-0.8	-	35	
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-9.3	-	11.4	
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU5 2K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	2	kΩ
DRPD5 2K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	2	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL5	Digital output low	DVDIO = 2.8V			0.42	V

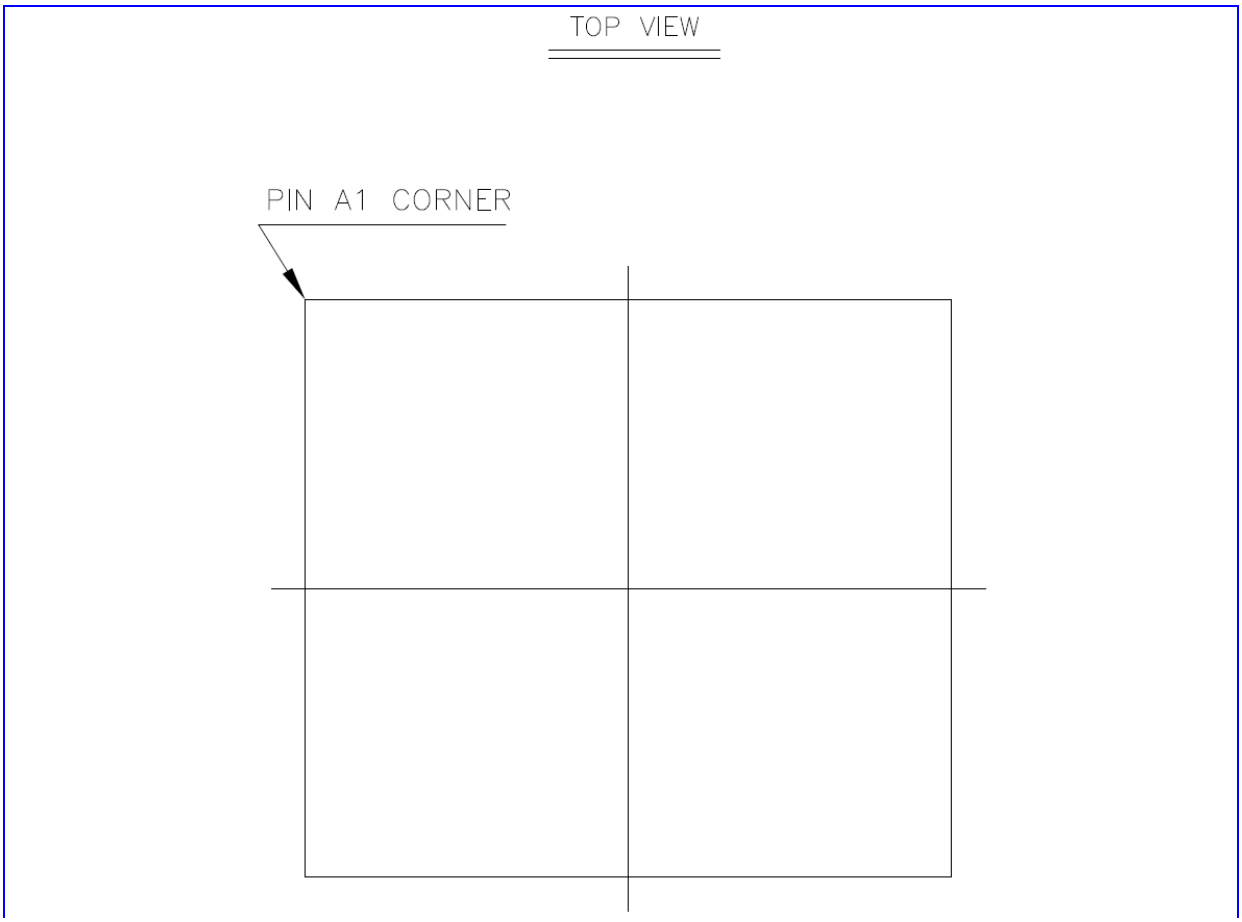
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	voltage for IO Type 5	DVDIO = 1.8V			0.27	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type 6	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA
DRPU6	Digital I/O pull-up	DVDIO = 2.8V	40	85	190	kΩ

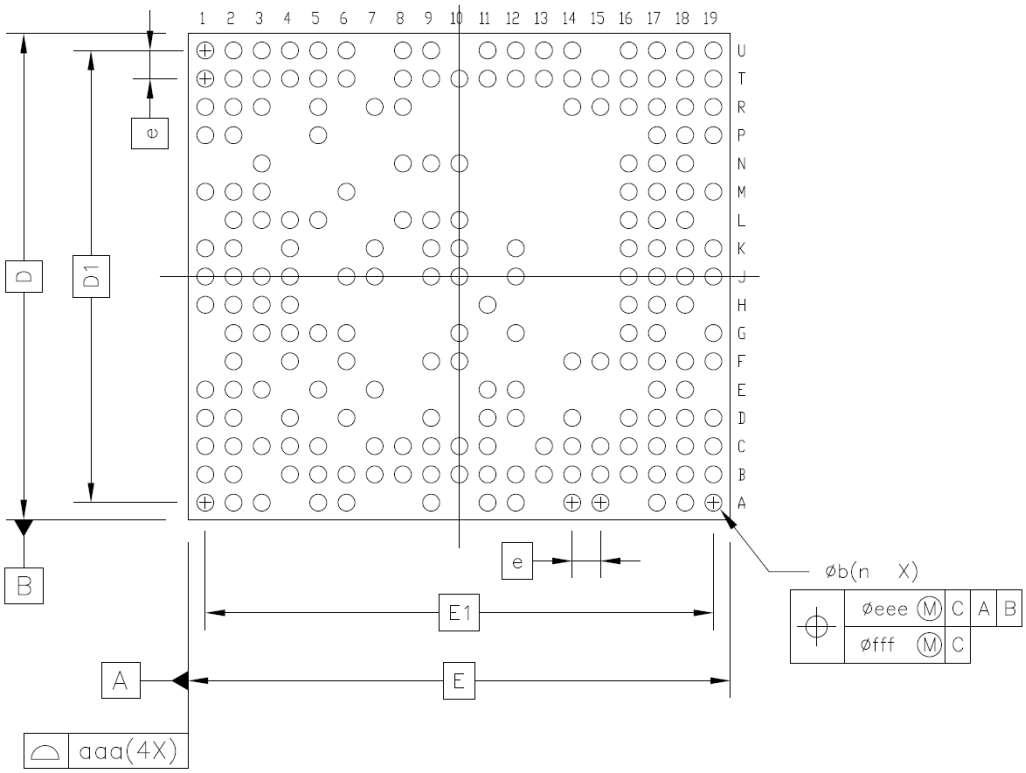
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	resistance for IO Type 6	DVDIO = 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH7	Digital high input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN7<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-0.8	-	35	
DIIL7	Digital low input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-9.3	-	11.4	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIOH7	Digital high output current for IO Type 7	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL7	Digital low output current for IO Type 7	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU7	Digital I/O pull-up resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD7	Digital I/O pull-down resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH7	Digital output high voltage for IO Type 7	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL7	Digital output low voltage for IO Type 7	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

2.3 Package Information

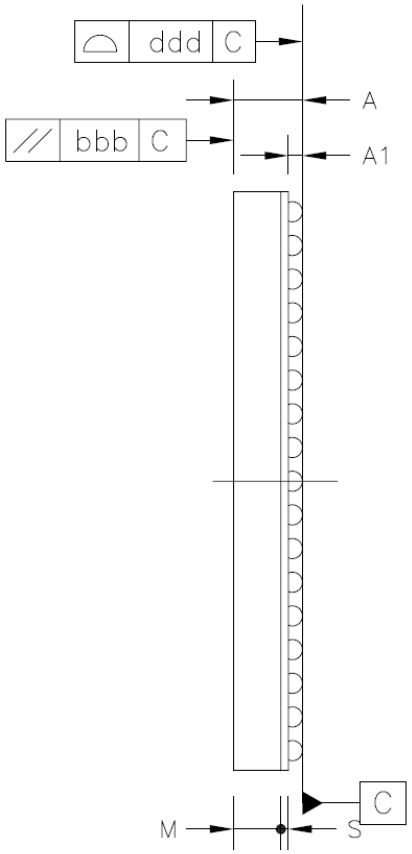
2.3.1 Package Outlines




1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
U T R P N M L K J H G F E D C B A
e
D
D1
B
e
E1
A
E
aaa(4X)
Øb(n X)
Øeee M C A B
Øfff M C

BOTTOM VIEW

SIDE VIEW



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			SBS TFBGA		
Body Size:	X	E	9.600		
	Y	D	8.600		
Ball Pitch :		e	0.500		
Total Thickness :		A	—	—	1.100
Mold Thickness :		M	0.700 Ref.		
Substrate Thickness :		S	0.110 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.160	—	0.260
Ball Width :		b	0.250	—	0.350
Package Edge Tolerance :		aaa	0.100		
Mold Flatness :		bbb	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	199		
Edge Ball Center to Center :	X	E1	9.000		
	Y	D1	8.000		

Figure 5. ***Outlines and dimension of TFBGA 9.6mm*8.6mm, 199-ball, 0.5 mm pitch package***

2.3.2 Thermal Operating Specifications

Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	48	C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	1.28	W	

2.3.3 Lead-free Packaging

MT6260 is provided in a lead-free package and meets RoHS requirements

2.4 Ordering Information

2.4.1 Top Marking Definition

Figure 6. ***Mass production top marking of MT6260***

Part number	Package	Description
MT6260A/BMB-PCU-H	TFBGA	8.6mm*9.6mm, 199-ball, 0.5 mm pitch package, non-security version