REGISTERED QUAD-RANK DDR SDRAM DIMM

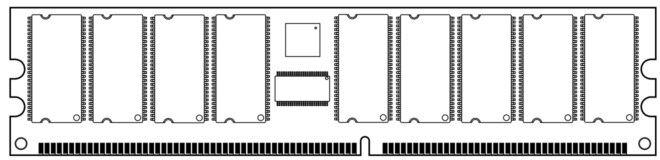
MT36VDDS12872D – 1GB (ADVANCE‡), MT36VDDT12872D – 1GB, MT36VDDS25672D – 2GB (ADVANCE‡), MT36VDDT25672D – 2GB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- 184-pin, dual in-line memory modules (DIMM), organized as four module ranks
- Fast data transfer rates: PC1600 and PC2100
- Utilizes 200 MT/s and 266 MT/s TwinDie™ DDR or Stacked TSOP DDR SDRAM components
- ECC, 1-bit error detection and correction
- Low-Profile PCB design
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to minimize loading
- 1GB (128 Meg x 72) and 2GB (256 Meg x 72)
- 2.5V I/O (SSTL_2 compatible)
- V_{DD}= $V_{DD}Q$= +2.5V
- V_{DDSPD} = +2.3V to +3.6V
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Selectable READ CAS latency
- Gold edge connectors

Figure 1: 184-Pin Low Profile DIMM (MO-206)



OPTIONS	MARKING
• Package	
184-Pin DIMM (Standard)	G
184-Pin DIMM (Lead-free)	Y
• Memory Clock/Data Frequency, CAS Latency[1]	
7.5ns (133 MHz)/266 MT/s, CL = 2	-262[2]
7.5ns (133 MHz)/266 MT/s, CL = 2	-26A[2]
7.5ns (133 MHz)/266 MT/s, CL = 2.5	-265
8ns (100 MHz)/200 MT/s, CL = 2	-202[2]

NOTE: 1. CL = Device CAS (READ) Latency; registered mode adds one clock cycle to CL due to the input register.
2. Contact factory for availability.

Table 1: Address Table

	MT36VDDS12872D	MT36VDDT12872D	MT36VDDS25672D	MT36VDDT25672D
Refresh Count	8K	8K	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Base Device Configuration	32 Meg x 8	32 Meg x 8	64 Meg x 8	64 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)	2K (A0–A9, A11)	2K (A0–A9, A11)
Module Rank Addressing	4 (S0#-S3#)	4 (S0#-S3#)	4 (S0#-S3#)	4 (S0#-S3#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORYCLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT36VDDS12872DG-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDS12872DY-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDS12872DG-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDS12872DY-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDS12872DG-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDS12872DY-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDS12872DG-202__	1GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDS12872DY-202__	1GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDT12872DG-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT12872DY-26A__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT12872DG-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT12872DY-262__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT12872DG-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT12872DY-265__	1GB	128 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT12872DG-202__	1GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDT12872DY-202__	1GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDS25672DG-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDS25672DY-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDS25672DG-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDS25672DY-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDS25672DG-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDS25672DY-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDS25672DG-202__	2GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDS25672DY-202__	2GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDT25672DG-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT25672DY-26A__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT36VDDT25672DG-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT25672DY-262__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT36VDDT25672DG-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT25672DG-265__	2GB	256 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT36VDDT25672DG-202__	2GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2
MT36VDDT25672DY-202__	2GB	128 Meg x 72	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT36VDDT12872DY-265A1.

Table 3: Pin Assignment (184-Pin DIMM Front)

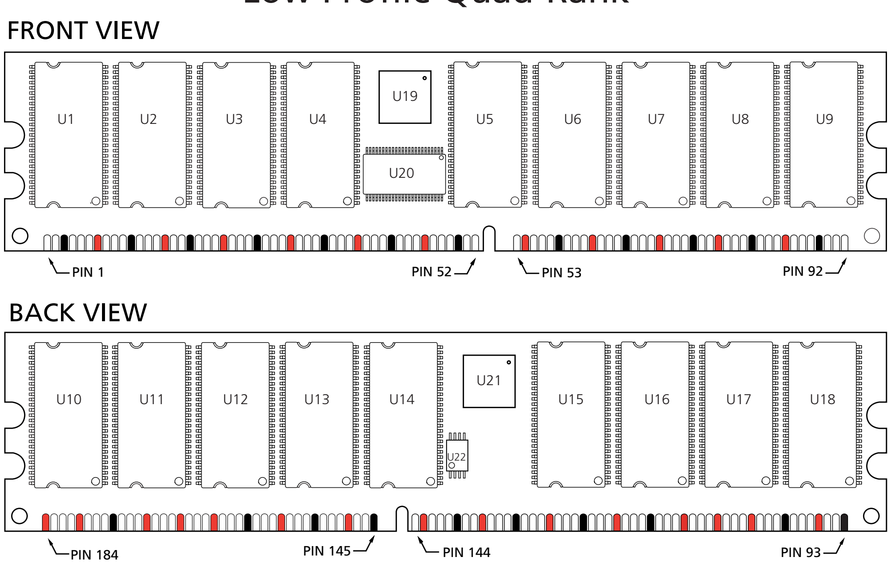
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DQS8	70	VDD
2	DQ0	25	DQS2	48	A0	71	S2#
3	VSS	26	VSS	49	CB2	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	CB3	74	VSS
6	DQ2	29	A7	52	BA1	75	DNU
7	VDD	30	VDD	53	DQ32	76	DNU
8	DQ3	31	DQ19	54	VDD	77	VDD
9	NC	32	A5	55	DQ33	78	DQS6
10	RESET#	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDD	38	VDD	61	DQ40	84	DQ57
16	DNU	39	DQ26	62	VDD	85	VDD
17	DNU	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	CB0	67	DQS5	90	NC
22	VDD	45	CB1	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Table 4: Pin Assignment (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DQS17/DM8	163	S3#
95	DQ5	118	A11	141	A10	164	VDD
96	VDD	119	DQS11/DM2	142	CB6	165	DQ52
97	DQS9/DM0	120	VDD	143	VDD	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	DNU
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15/DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13/DM4	172	VDD
104	VDD	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDD	151	DQ39	174	DQ60
106	DQ13	129	DQS12/DM3	152	VSS	175	DQ61
107	DQS10/DM1	130	A3	153	DQ44	176	VSS
108	VSS	131	DQ30	154	RAS#	177	DQS16/DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDD	179	DQ63
111	CKE1	134	CB4	157	S0#	180	VDD
112	VDD	135	CB5	158	S1#	181	SA0
113	NC	136	VDD	159	DQS14/DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	A12	138	CK0#	161	DQ46	184	VDDSPD

Figure 2: 184-Pin DIMM Pin Locations

Low Profile Quad-Rank



Indicates a VDD or VDDQ pin   Indicates a VSS pin

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment Tables on page 3 for more information

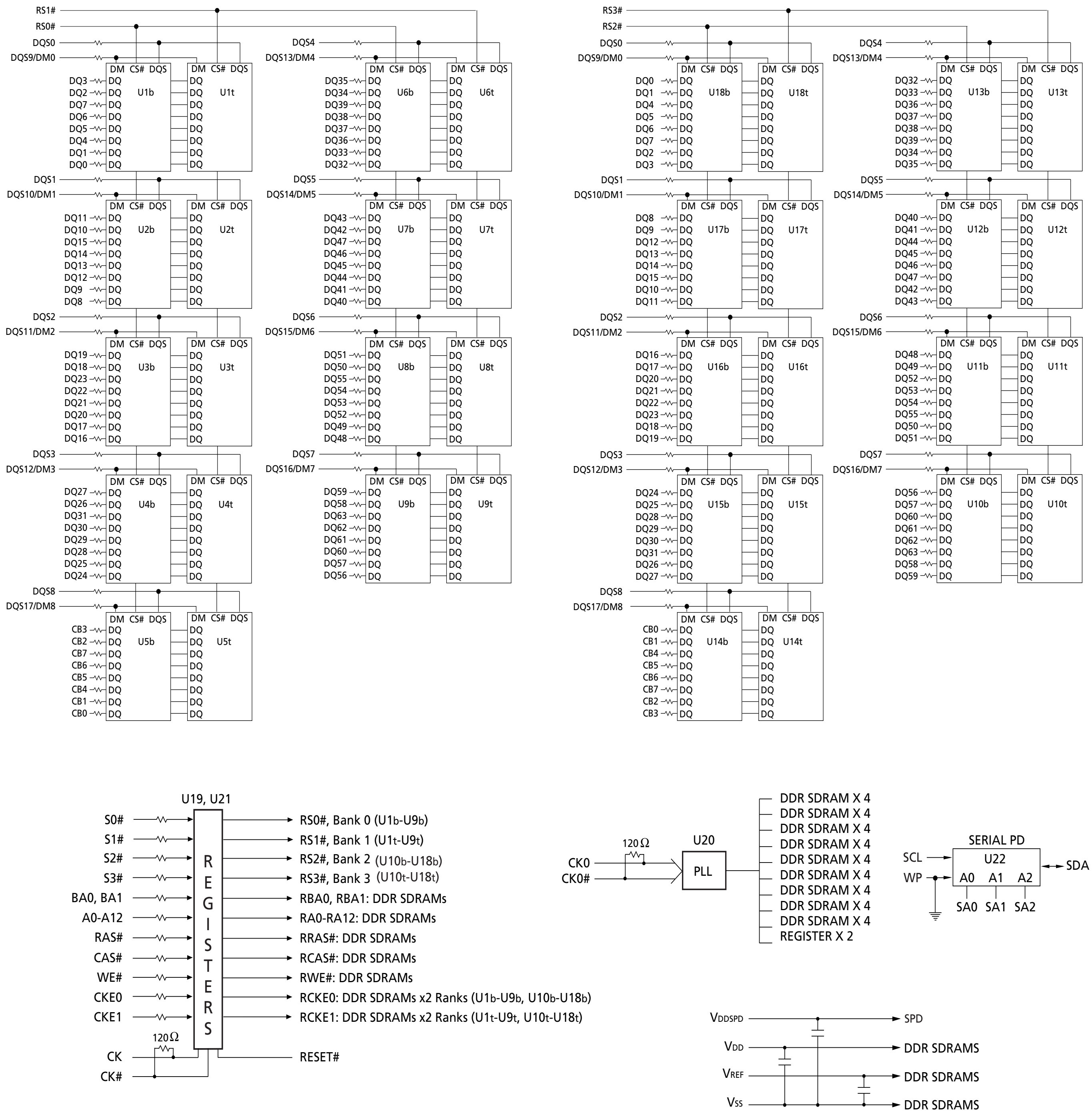
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	VREF	Input	SSTL_2 reference voltage.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
71, 157, 158, 163	CS0–CS4	Input	Chip Select.
137, 138	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21, 111	CKE0 - CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after VDD is applied.
52, 59	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115, 118, 122, 125, 130, 141	A0-A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
91	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
10	RESET#	Input	Asynchronously forces all register outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure CKE is LOW and SDRAM DQs are High-Z.
44, 45, 49, 51, 134, 135, 142, 144	CB0-CB7	Input/Output	Data I/Os: Check bits. ECC 1-bit error detection and correction.

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Pin Assignment Tables on page 3 for more information

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 14, 25, 36, 47, 56, 67, 78, 86, 97, 107, 119, 129, 140, 149, 159, 169, 177	DQS0-DQS17	Input/Output	Data Strobe: DQS0-DQS8, Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data. Data Mask: DQS9-DQS17 function as DM0-DM8 to mask WRITE data when when HIGH.
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
7, 15, 22, 30, 38, 46, 54, 62, 70, 77, 85, 96,104, 108, 112, 120, 128, 136, 143, 148, 156, 164, 168, 172, 180	VDD	Supply	Power Supply: +2.5V ±0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	VSS	Supply	Ground.
184	VDDSPD	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
9, 82, 90, 101, 102, 103, 113, 173	NC	—	No Connect: These pins should be left unconnected.
16, 17, 75, 76, 167	DNU	—	Do Not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.

Figure 3: Functional Block Diagram



NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron modules utilize various component speed grades, as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

MT46V32M8S2 DDR SDRAMs for MT36VDDS12872D
MT46V64M8S2 DDR SDRAMs for MT36VDDT12872D
MT46V32M8TG DDR SDRAMs for MT36VDDS25672D
MT46V64M8TG DDR SDRAMs for MT36VDDT25672D

General Description

The Micron MT36VDDS12872D, MT36VDDT12872D, MT36VDDS25672D, and MT36VDDT25672D are high-speed CMOS, dynamic random-access, 1GB and 2GB quad-rank registered memory modules, organized in a x72 (ECC) configuration using internally configured quad-bank DDR SDRAM devices.

These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR SDRAM modules operates from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0–A12 select device row). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 256Mb, 512Mb, DDR SDRAM and 512Mb and 1Gb TwinDie DDR SDRAM component data sheets.

PLL and Register Operation

These DDR SDRAM modules operate in registered mode, where the control/address input signals are latched in the register on one rising clock edge and sent to the DDR SDRAM devices on the following rising clock edge (data access is delayed by one clock). A phase-lock loop (PLL) on the module is used to redrive the differential clock signals CK and CK# to the DDR SDRAM devices to minimize system clock loading.

Serial Presence-Detect Operation

These DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 4, Mode Register Definition Diagram, on page 8. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A12 when the burst length is set to two, by A2–A12 when the burst length is set to four and by A3–A12 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 9.

Read Latency

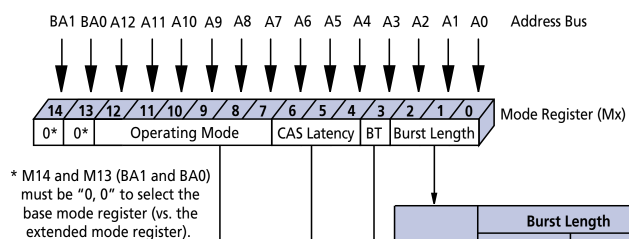
The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in Figure 5, CAS Latency Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table Table 7:, CAS Latency (CL) Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 4: Mode Register Definition Diagram

1GB and 2GB Modules



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	Reserved
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				SEQUENTIAL	INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

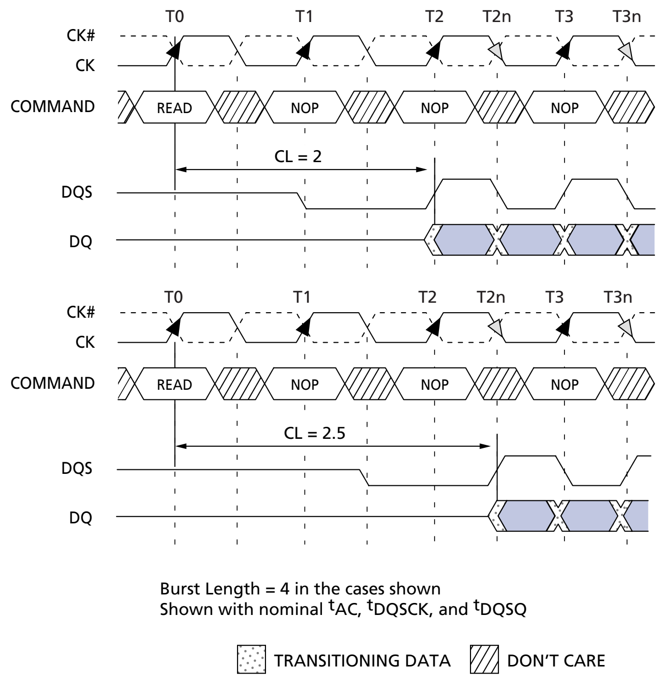
1. For a burst length of two, A1–A12 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A12 select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A12 select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Table 7: CAS Latency (CL) Table

Registered mode will add one clock cycle to each CL

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CL = 2	CL = 2.5
-262	$75 \leq f \leq 133$	$75 \leq f \leq 133$
-26A	$75 \leq f \leq 133$	$75 \leq f \leq 133$
-265	$75 \leq f \leq 100$	$75 \leq f \leq 133$
-202	$75 \leq f \leq 100$	$75 \leq f \leq 125$

Figure 5: CAS Latency Diagram



Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A12 each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A12 each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 6, Extended Mode Register Definition Digram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

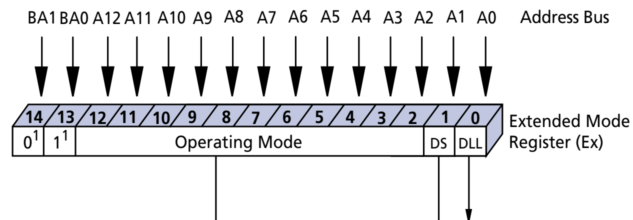
The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 6: Extended Mode Register Definition Digram

1GB and 2GB Modules



E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal

E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[2]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE:

1. E14 and E13 (BA1 and BA0) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Commands

Truth Table 1 provides a general reference of available commands. For a more detailed description of commands and operations, refer to the Micron 256Mb, 512Mb, 512Mb TwinDie, or 1Gb TwinDie DDR SDRAM component data sheets.

Table 8: Commands Truth Table

Note: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	2
ACTIVE (Select device bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select device bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	5
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	Code	6
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	7, 8
LOAD MODE REGISTER	L	L	L	L	Op-Code	9

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. DESELECT and NOP are functionally interchangeable.
3. BA0-BA1 provide device bank address and A0-A12 provide row address.
4. BA0-BA1 provide device bank address; A0-A9 (1GB), A0–A9, A11 (2GB) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
6. A10 LOW: BA0-BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
9. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A12 provide the op-code to be written to the selected mode register.

Table 9: DM Operation Truth Table

Used to mask write data; provided coincident with the corresponding data.

NAME (FUNCTION)	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply
Relative to VSS -1V to +3.6V
Voltage on VDDQ Supply
Relative to VSS -1V to +3.6V
Voltage on VREF and Inputs
Relative to VSS -1V to +3.6V
Voltage on I/O Pins
Relative to VSS -0.5V to VDDQ +0.5V

Operating Temperature
T_A (ambient)0°C to +55°C
Storage Temperature (plastic) . . . . . .-70°C to +150°C
Power Dissipation 36W
Short Circuit Output Current. 50mA

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDD	2.3	2.7	V	32, 36
I/O Supply Voltage		VDDQ	2.3	2.7	V	32, 36,39
I/O Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT (All Modules) Any input 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/Address, CAS#, RAS#, WE#, S#, CKE	II	-5	5	µA	48
	CK, CK#		-10	10		
	DQS, DQM		-8	8		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ	DQ	IOZ	-20	20	µA	48
OUTPUT LEVELS: High Current (VOUT = VDDQ-0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 34
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8			

Table 11: AC Input Operating Conditions

Notes: 1–5, 14; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	12, 25, 35
I/O Reference Voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

Table 12: IDD Specifications and Conditions (MT36VDDS12872D)

Notes: 1–5, 8, 10, 12; DDR SDRAM components; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD, VDDQ = +2.5V ±0.2V

		MAX				
PARAMETER/CONDITION	**SYM**	**-262**	**-26A/ -265**	**-202**	**UNITS**	**NOTES**
OPERATING CURRENT: One die in IDD0 condition, one die in IDD2P condition. (IDD0 Condition) one device bank; Active-Precharge; ^{t}RC=^{t}RC (MIN); ^{t}CK=^{t}CK (MIN); DQ, DM and DQS inputs changing once per clocke cycle; Address and control inputs changing once every two clock cycles.	IDD0[a]	TBD	1,341	TBD	mA	20, 42
OPERATING CURRENT: One die in IDD1 condition, one die in IDD2P condition. (IDD1 Condition) one device bank; Active-Precharge; Burst = 2; ^{t}RC=^{t}RC (MIN); ^{t}CK=^{t}CK (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle.	IDD1[a]	TBD	1,521	TBD	mA	20, 42
PRECHARGE POWER-DOWN STANDBY CURRENT: Both die in IDD2P condition . (IDD2P Condition) All device banks idle; Power-down mode; ^{t}CK=^{t}CK (MIN); CKE= LOW	IDD2P[b]	TBD	288	TBD	mA	21, 28, 44
IDLE STANDBY CURRENT: Both die in IDD2F condition. (IDD2F Condition) CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK (MIN); CK = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM	IDD2F[b]	TBD	2,880	TBD	mA	45
ACTIVE POWER-DOWN STANDBY CURRENT: Both die in IDD3P condition. (IDD3P Condition) One device bank active; Power-down mode; ^{t}CK = CK (MIN); CKE= LOW	IDD3P[b]	TBD	2,160	TBD	mA	21, 28, 44
ACTIVE STANDBY CURRENT: Both die in IDD3N condition. (IDD3N condition) CS# = HIGH; CKE= HIGH; One device bank active; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N[b]	TBD	3,240	TBD	mA	41
OPERATING CURRENT: One die in IDD4R condition, one die in IDD2P condition. (IDD4R condition) Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA	IDD4R[a]	TBD	1,836	TBD	mA	20, 42
OPERATING CURRENT: One die in IDD4W condition, one die in IDD2P condition. (IDD4W condition) Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W[a]	TBD	1,971	TBD	mA	20
AUTO REFRESH CURRENT: An AUTO REFRESH command is given to one die, and on the next clock cycle the second die receives an AUTO REFRESH command. ^{t}RC = ^{t}RC(MIN), CKE = HIGH	IDD5[b]	TBD	8,460	TBD	mA	20, 44
AUTO REFRESH DISTRIBUTED CURRENT: An AUTO REFRESH command given to one die and on the next clock cycle the second die recieves an AUTO REFRESH command. ^{t}RC = 7.8125µs, CKE = LOW for ^{t}RFC time.	IDD5A[b]	TBD	360	TBD	mA	24, 44
SELF REFRESH CURRENT: Both die are in IDD6 condition, CKE ≤ 0.2V	IDD6[b]	TBD	288	TBD	mA	9
OPERATING CURRENT: One die in IDD7 condition, one die in IDD3N condition. (IDD7 condition) Four device bank interleaving READs (BL = 4) with auto precharge, ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during active READ or WRITE commands.	IDD7[a]	TBD	3,906	TBD	mA	20, 43

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 13: IDD Specifications and Conditions (MT36VDDT12872D)

Notes: 1–5, 8, 10, 12; DDR SDRAM components; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD, VDDQ = +2.5V ±0.2V

PARAMETER/CONDITION		SYM	MAX -262	MAX -26A/ -265	MAX -202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles;		IDD0[a]	1,233	1,053	1,188	mA	20, 42
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1[a]	1,548	1,413	1,503	mA	20, 42
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = (LOW)		IDD2P[b]	144	144	144	mA	21, 28, 44
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ^{t}CK = ^{t}CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F[b]	1,620	1,620	1,620	mA	45
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ^{t}CK = ^{t}CK (MIN); CKE = LOW		IDD3P[b]	900	900	1,080	mA	21, 28, 44
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ^{t}RC = ^{t}RAS (MAX); ^{t}CK = ^{t}CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N[b]	1,800	1,800	1,800	mA	41
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); IOUT = 0mA		IDD4R[a]	1,458	1,458	1,683	mA	20, 42
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^{t}CK = ^{t}CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W[a]	1,323	1,323	1,818	mA	20
AUTO REFRESH CURRENT	^{t}RC = ^{t}RFC (MIN)	IDD5[b]	8,460	8,460	8,820	mA	20, 44
	^{t}RC = 7.81µs	IDD5A[b]	216	216	216	mA	24, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6[b]	144	144	144	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge with, ^{t}RC = minimum ^{t}RC allowed; ^{t}CK = ^{t}CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.		IDD7[a]	3,258	3,258	3,393	mA	20, 43

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 14: IDD Specifications and Conditions (MT36VDDS25672D)

Notes: 1–5, 8, 10, 12; DDR SDRAM components; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD, VDDQ = +2.5V ±0.2V

		MAX				
PARAMETER/CONDITION	SYM	-262	-26A/ -265	-202	UNITS	NOTES
OPERATING CURRENT: One die in IDD0 condition, one die in IDD2P condition. (IDD0 Condition) one device bank; Active-Precharge; ${}^tRC={}^tRC$ (MIN); ${}^tCK={}^tCK$ (MIN); DQ, DM and DQS inputs changing once per clocke cycle; Address and control inputs changing once every two clock cycles.	IDD0[a]	TBD	TBD	TBD	mA	20, 42
OPERATING CURRENT: One die in IDD1 condition, one die in IDD2P condition. (IDD1 Condition) one device bank; Active-Precharge; Burst = 2; ${}^tRC={}^tRC$ (MIN); ${}^tCK={}^tCK$ (MIN); Iout = 0mA; Address and control inputs changing once per clock cycle.	IDD1[a]	TBD	TBD	TBD	mA	20, 42
PRECHARGE POWER-DOWN STANDBY CURRENT: Both die in IDD2P condition . (IDD2P Condition) All device banks idle; Power-down mode; ${}^tCK={}^tCK$ (MIN); CKE= LOW	IDD2P[b]	TBD	TBD	TBD	mA	21, 28, 44
IDLE STANDBY CURRENT: Both die in IDD2F condition. (IDD2F Condition) CS# = HIGH; All device banks idle; ${}^tCK = {}^tCK$ (MIN); CK = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS and DM	IDD2F[b]	TBD	TBD	TBD	mA	45
ACTIVE POWER-DOWN STANDBY CURRENT: Both die in IDD3P condition. (IDD3P Condition) One device bank active; Power-down mode; ${}^tCK$ = CK (MIN); CKE= LOW	IDD3P[b]	TBD	TBD	TBD	mA	21, 28, 44
ACTIVE STANDBY CURRENT: Both die in IDD3N condition. (IDD3N condition) CS# = HIGH; CKE= HIGH; One device bank active; ${}^tRC = {}^tRAS$ (MAX); ${}^tCK = {}^tCK$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N[b]	TBD	TBD	TBD	mA	41
OPERATING CURRENT: One die in IDD4R condition, one die in IDD2P condition. (IDD4R condition) Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ${}^tCK = {}^tCK$ (MIN); IOUT = 0mA	IDD4R[a]	TBD	TBD	TBD	mA	20, 42
OPERATING CURRENT: One die in IDD4W condition, one die in IDD2P condition. (IDD4W condition) Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ${}^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W[a]	TBD	TBD	TBD	mA	20
AUTO REFRESH CURRENT: An AUTO REFRESH command is given to one die, and on the next clock cycle the second die receives an AUTO REFRESH command. ${}^tRC = {}^tRC$(MIN), CKE = HIGH	IDD5[b]	TBD	TBD	TBD	mA	20, 44
AUTO REFRESH DISTRIBUTED CURRENT: An AUTO REFRESH command given to one die and on the next clock cycle the second die recieves an AUTO REFRESH command. ${}^tRC$ = 7.8125µs, CKE = LOW for ${}^tRFC$ time.	IDD5A[b]	TBD	TBD	TBD	mA	24, 44
SELF REFRESH CURRENT: Both die are in IDD6 condition, CKE ≤ 0.2V	IDD6[b]	TBD	TBD	TBD	mA	9
OPERATING CURRENT: One die in IDD7 condition, one die in IDD3N condition. (IDD7 condition) Four device bank interleaving READs (BL = 4) with auto precharge, ${}^tRC = {}^tRC$ (MIN); ${}^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands.	IDD7[a]	TBD	TBD	TBD	mA	20, 43

NOTE:

a - Value calculated as one module bank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 15: I_{DD} Specifications and Conditions (MT36VDDT25672D)

Notes: 1–5, 8, 10, 12; DDR SDRAM components; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; V_{DD}, $V_{DD}Q$ = +2.5V ±0.2V

PARAMETER/CONDITION		SYM	MAX -262	MAX -26A/ -265	MAX -202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; ${}^tRC = {}^tRC$ (MIN); ${}^tCK = {}^tCK$ (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles;		I_{DD0}[a]	TBD	945	1,332	mA	20, 42
OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 2; ${}^tRC = {}^tRC$ (MIN); ${}^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}[a]	TBD	1,170	1,467	mA	20, 42
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; ${}^tCK = {}^tCK$ (MIN); CKE = (LOW)		I_{DD2P}[b]	TBD	180	216	mA	21, 28, 44
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; ${}^tCK = {}^tCK$ MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}[b]	TBD	1,440	1,260	mA	45
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; ${}^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD3P}[b]	TBD	648	900	mA	21, 28, 44
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; ${}^tRC = {}^tRAS$ (MAX); ${}^tCK = {}^tCK$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}[b]	TBD	1,440	1,260	mA	41
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ${}^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}[a]	TBD	1,665	1,647	mA	20, 42
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ${}^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}[a]	TBD	1,845	1,737	mA	20
AUTO REFRESH CURRENT	${}^tRC = {}^tRFC$ (MIN)	I_{DD5}[b]	TBD	1,845	2,997	mA	20, 44
	${}^tRC$ = 7.81µs	I_{DD5A}[b]	TBD	288	252	mA	24, 44
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD6}[b]	TBD	108	252	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge with, ${}^tRC$ = minimum ${}^tRC$ allowed; ${}^tCK = {}^tCK$ (MIN); Address and control inputs change only during Active READ, or WRITE commands.		I_{DD7}[a]	TBD	2,835	3,987	mA	20, 43

NOTE:

a - Value calculated as one module rank in this operating condition, and all other module ranks in I_{DD2P} (CKE LOW) mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 16: Capacitance (MT36VDDS12872D and MT36VDDT12872D)

Note: 11; notes appear on pages 19–22

PARAMETER	SYMBOL	MIN	MAX
Input/Output Capacitance: DQ, DQS/DM	C_{IO}	16.0	20.0
Input Capacitance: Command and Address	C_{I1}	2.5	3.5
Input Capacitance: S#	C_{I1}	2.5	3.5
Input Capacitance: CK, CK#	C_{I2}	–	4
Input Capacitance: CKE	C_{I3}	2.5	3.5

Table 17: Capacitance (MT36VDDS25672D and MT36VDDT25672D)

Note: 11; notes appear on pages 19–22

PARAMETER	SYMBOL	MIN	MAX
Input/Output Capacitance: DQ, DQS/DM	C_{IO}	TBD	TBD
Input Capacitance: Command and Address	C_{I1}	TBD	TBD
Input Capacitance: S#	C_{I1}	TBD	TBD
Input Capacitance: CK, CK#	C_{I2}	TBD	TBD
Input Capacitance: CKE	C_{I3}	TBD	TBD

Table 18: DDR SDRAM Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 12–15, 29; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

ACCHARACTERISTICS			-262		-26A/-265		-202		UNITS	NOTES
PARAMETER		SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of DQs from CK/CK#		^tAC	-0.70	+0.70	-0.75	+0.75	-0.8	+0.75	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	26
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	7.5	13	8	13	ns	40, 46
	CL = 2	^tCK (2)	7.5	13	7.5	13	10	13	ns	40, 46
DQ and DM input hold time relative to DQS		^tDH	0.45		0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS		^tDS	0.45		0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		2		ns	27
Access window of DQS from CK/CK#		^tDQSCK	-0.65	+0.6	-0.75	+0.75	-0.8	+0.75	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.45		0.5		0.5	ns	22, 23
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		0.2		^tCK	
Half clock period		^tHP	^tCH,^tCL		^tCH,^tCL		^tCH,^tCL		ns	30
Data-out high-impedance window from CK/CK#		^tHZ		+0.7		+0.75		+0.75	ns	16, 37

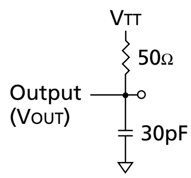
Table 18: DDR SDRAM Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–5, 12–15, 29; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

ACCHARACTERISTICS		-262		-26A/-265		-202			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Data-out low-impedance window from CK/CK#	^tLZ	-0.7		-0.75		-0.8		ns	16,38
Address and control input hold time (fast slew rate)	^tIH_F	0.75		0.90		1.1		ns	12
Address and control input setup time (fast slew rate)	^tIS_F	0.75		0.90		1.1		ns	12
Address and control input hold time (slow slew rate)	^tIH_S	0.8		1		1.1		ns	12
Address and control input setup time (slow slew rate)	^tIS_S	0.8		1		1.1		ns	12
Address and control input pulse width (for each input)	^tIPW	2.2		2.2		2.5		ns	12
LOAD MODE REGISTER command cycle time	^tMRD	15		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^tQH	^tHP-^tQHS		^tHP-^tQHS		^tHP -^tQHS		ns	22, 23
Data Hold Skew Factor	^tQHS		0.75		0.75		0.75	ns	
ACTIVE to PRECHARGE command	^tRAS	40	120,000	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto Precharge command	^tRAP	15		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	^tRC	60		65		70		ns	
AUTO REFRESH command period	^tRFC	75		75		80		ns	44
ACTIVE to READ or WRITE delay	^tRCD	15		20		20		ns	
PRECHARGE command period	^tRP	15		20		20		ns	
DQS read preamble	^tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	ns	37
DQS read postamble	^tRPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank *a* to ACTIVEbank *b* command	^tRRD	15		15		15		^tCK	
DQS write preamble	^tWPRE	0.25		0.25		0.25		ns	
DQS write preamble setup time	^tWPRES	0		0		0		^tCK	18, 19
DQS write postamble	^tWPST	0.4	0.6	0.4	0.6	0.4	0.6	ns	17
Write recovery time	^tWR	15		15		15		^tCK	
Internal WRITE to READ command delay	^tWTR	1		1		1		ns	
Data valid output window (DVW)	na	^tQH -^tDQSQ		^tQH -^tDQSQ		^tQH - ^tDQSQ		^tCK	22
REFRESH to REFRESH command interval	^tREFC		70.3		70.3		70.3	ns	21
Average periodic refresh interval	^tREFI		7.8		7.8		7.8	µs	21
Terminating voltage delay to VDD	^tVTD	0		0		0		µs	
Exit SELF REFRESH to non-READ command	^tXSNR	75		75		80		ns	
Exit SELF REFRESH to READ command	^tXSRD	200		200		200		ns	

Notes

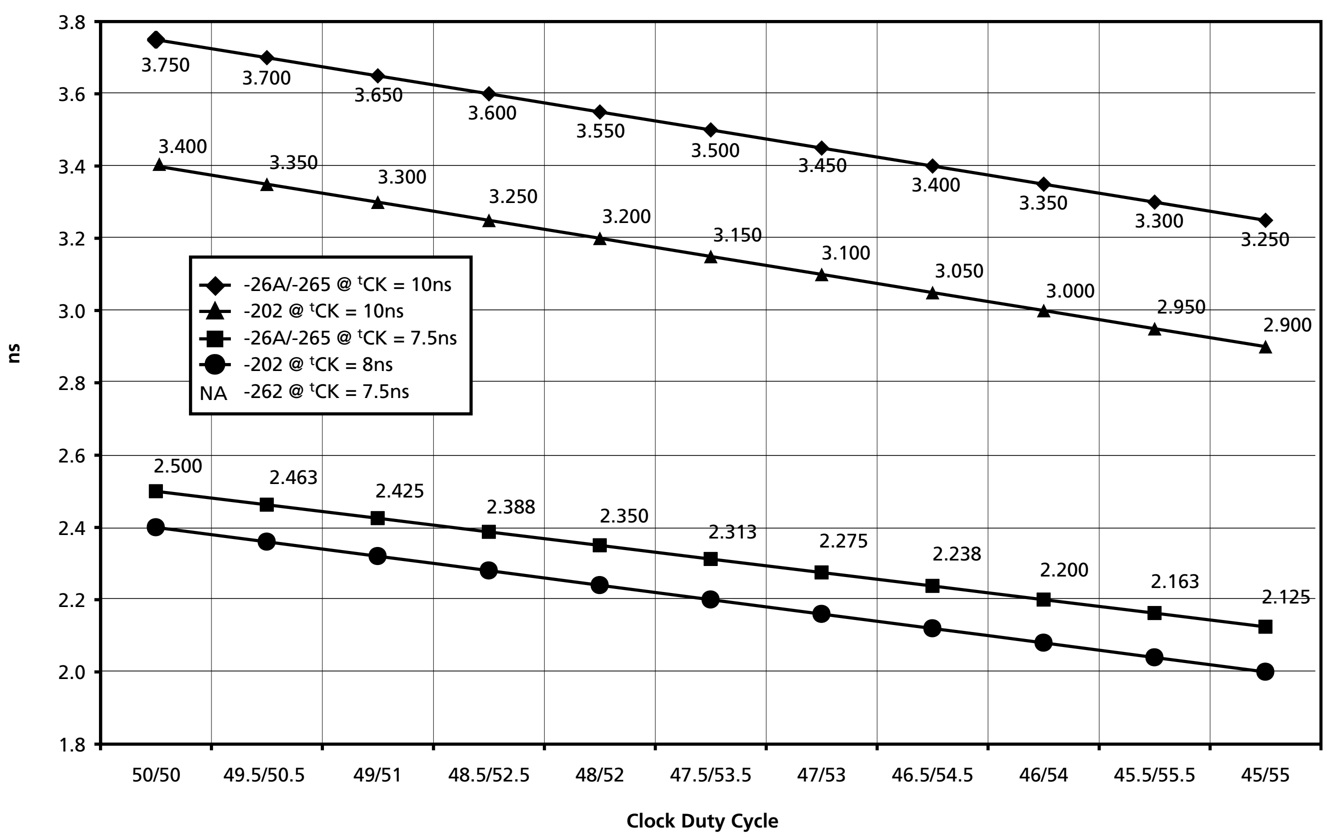
1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±2 percent of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF by-pass capacitor.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
8. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -262 and -26A; CL = 2.5 for -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V, VREF = VSS, f = 100 MHz, T_A = 25°C, VOUT(DC) = VDDQ/2, VOUT (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -262, -26A, and -265 with slew rates 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns, while ^{t}IH remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is VREF.
14. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.3 x VDDQ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is VTT.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for IDD measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

21. The refresh period 64ms. This equates to an average refresh rate of 7.821µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. Figure 7, Derating Data Valid Window (^{t}QH - ^{t}DQSQ), shows the derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.

Figure 7: Derating Data Valid Window (^{t}QH - ^{t}DQSQ)



30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS(MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch must be less than 1/3 of the clock and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, whichever is more positive.
33. Normal Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9, Pull-Up Characteristics.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9, Pull-Up Characteristics.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: VIH (MAX) = VDDQ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIl undershoot: VIL (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. VDD and VDDQ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^{t}HZ(MAX) and the last DVW. ^{t}HZ(MAX) will prevail over ^{t}DQSCK(MAX) + ^{t}RPST(MAX) condition. ^{t}LZ(MIN) will prevail over ^{t}DQSCK(MIN) + ^{t}RPRE(MAX) condition.
38. or slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.

Figure 8: Pull-Down Characteristics

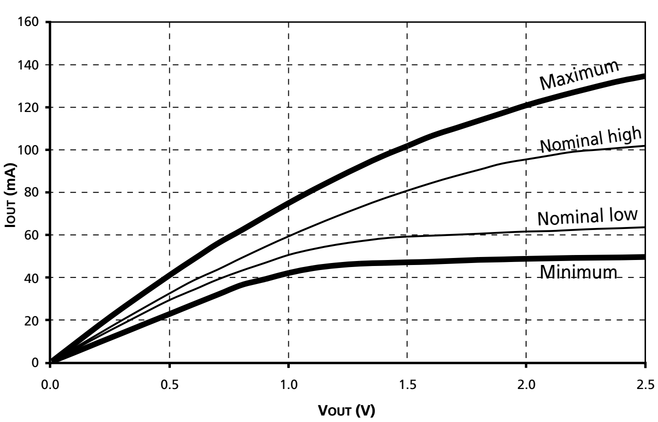
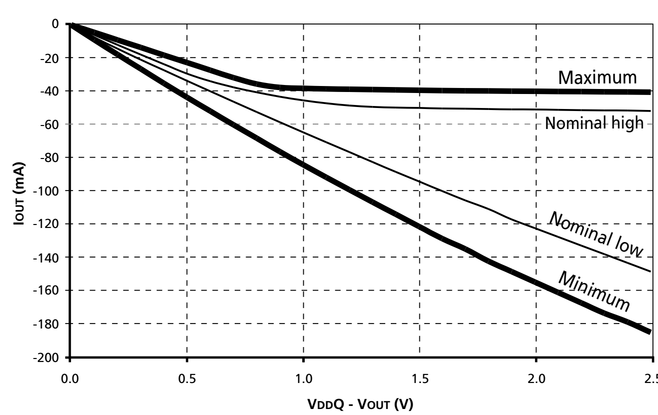


Figure 9: Pull-Up Characteristics



40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. For the -262, -26A, and -265 modules, IDD3N is specified to be 35mA at 100 MHz.
42. Random addressing changing and 50 percent of data changing at every transfer.
43. Random addressing changing and 100 percent of data changing at every transfer.
44. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
45. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."
46. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
47. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.

Table 19: Register Timing Requirements and Switching Characteristics

Notes: 2–6

REGISTER	PARAMETER	SYMBOL	CONDITIONS	$0°C \le T_A \le +70°C$ VDD = 2.5V ± 0.2V MIN	MAX	UNITS	NOTES
1:1 13-26 bit SSTL	Clock Frequency	^tclock			200	MHz	
	Pulse duration, CK, CK# HIGH or LOW	^tW		2.5			
	Differential inputs, active time (see Note 1)	^tact			22	ns	1
	Differential inputs, inactive time (see Note 2)	^tinact			22	ns	1
	Setup time, fast slew rate (See Notes 3 and 5)	^tsu	Data before CK↑/ CK↓	0.75		ns	
	Setup time, slow slew rate (See Notes 4 and 5)			0.9		ns	
	Hold time, fast slew rate (See Notes 3 and 5)	th	Data after CK↑/ CK↓	0.75			
	Hold time, slow slew rate (See Notes 4 and 5)			0.9		ns	

NOTE:

1. This parameter is not necessarily production tested.
2. Data inputs must be low a minimum time of tact MAX, after RESET is taken HIGH.
3. Data and clock inputs must be held at valid levels (not floating) a minimum time of ^{t}inact MAX, after RESET# is taken LOW.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CK, CK# signals input slew rates are ≥ 1 V/ns.

Table 20: PLL Clock Driver Timing Requirements and Switching Characteristics

Note: 1

PARAMETER	SYMBOL	TEST CONDITIONS	T_A = 0–70°C VDD = 2.5V ± 0.2V			UNITS	NOTES
			MIN	NOM	MAX		
Clock frequency	^{f}C		66		167	MHz	2, 3
Input clock duty cycle			40%		60%		
Stabilization time[1]					0.1	ms	4
Low-to high level propagation delay time	^{t}PLH	CK mode/CK to any output	1.5	3.5	6	ns	
High-to low level propagation delay time	^{t}PHL	CK mode/CK to any output	1.5	3.5	6	ns	5
Output enable time	^{t}en	CK mode/G to any Y output		3		ns	
Output disable time	^{t}dis	CK mode/G to any Y output		3		ns	6
Jitter (peak-to-peak)	$^{t}(jitter)$	66 MHz			120	ps	6
		100/125/133/167 MHz			75		
Jitter (cycle-to-cycle)	$^{t}(jitter)$	66 MHz			110	ps	7
		100/125/133/167 MHz			65		2, 3
Phase error	$^{t}(phase error)$	Terminated with 120Ω/16pF	-150		150	ns	
							4
Output skew	$^{t}skew(o)$	Terminated with 120Ω/16pF			100	ns	
Pulse skew	^{t}dis	Terminated with 120Ω/16pF			100	ns	5
Duty cycle		66 MHz to 100 MHz	49.5%		50.5%		
		101 MHz to 167 MHz	49%		51%		6
Output rise and fall times (20% - 80%)	^{t}r, ^{t}f	Load = 120Ω/16pF	650	800	950	ps	6

NOTE:

1. The timing and switching specifications for the PLL listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. The PLL must be able to handle spread spectrum induced skew.
3. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low-speed system debug.)
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
5. Static Phase Offset does not include Jitter.
6. Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
7. The output slew rate is determined from the IBIS model:

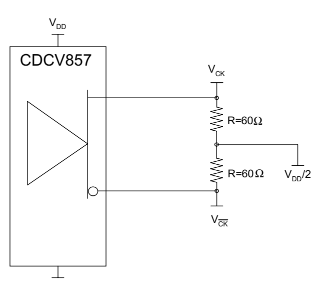
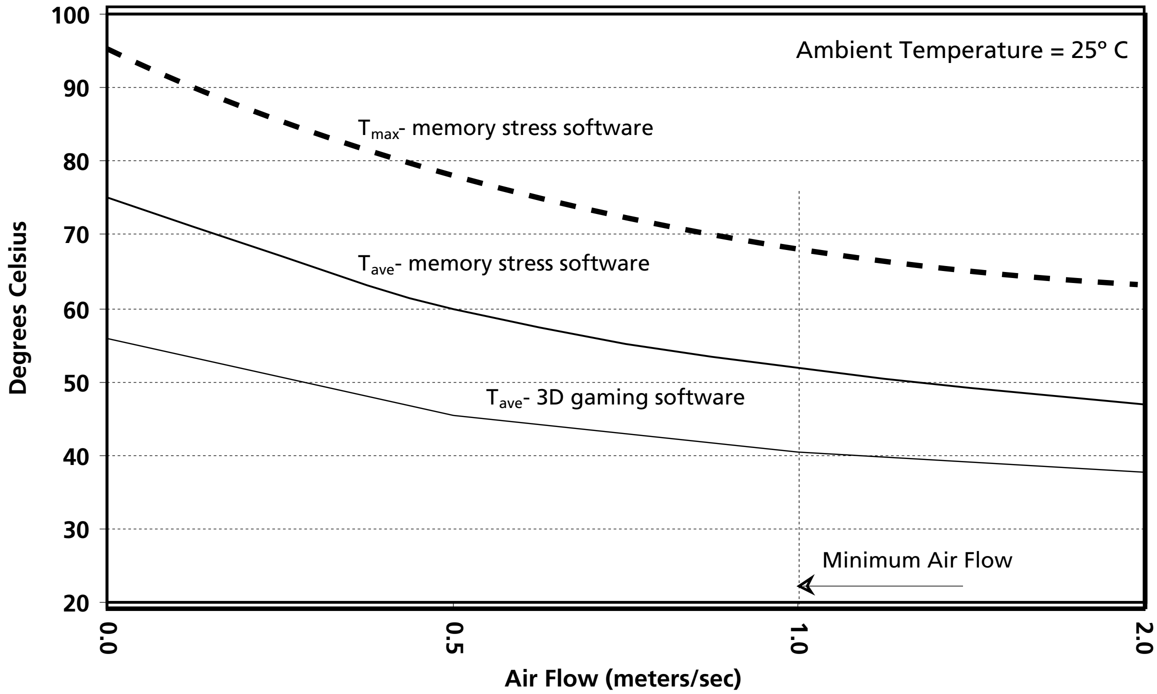


Figure 10: Component Case Temperature Vs. Air Flow



NOTE:

1. Micron Technology, Inc. recommends a minimum air flow of 1 meter/second (~197 LFM) across MT36VDDS12872D, MT36VDDT12872D, MT36VDDS25672D, and MT36VDDT25672D modules when installed in a system.
2. The component case temperature measurements shown above were obtained experimentally. The typical system to be used for experimental purposes is a dual-processor 600 MHz work station, fully loaded, with four comparable registered memory modules. Case temperatures charted represent worst-case component locations on modules installed in the internal slots of the system.
3. Temperature versus air speed data is obtained by performing experiments with the system motherboard removed from its case and mounted in a Eiffel-type low air speed wind tunnel. Peripheral devices installed on the system motherboard for testing are the processor(s) and video card, all other peripheral devices are mounted outside of the wind tunnel test chamber.
4. The memory diagnostic software used for determining worst-case component temperatures is a memory diagnostic software application developed for internal use by Micron Technology, Inc.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 11, Data Validity, and Figure 12, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 13, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 11: Data Validity

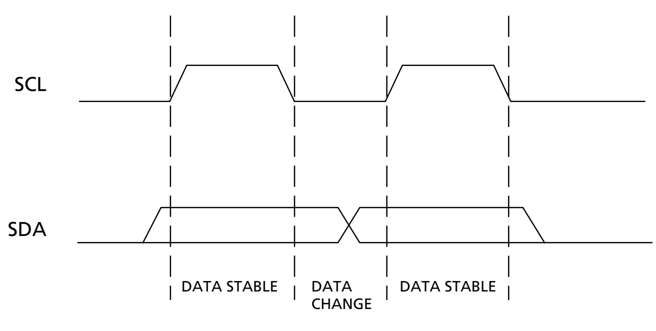


Figure 12: Definition of Start and Stop

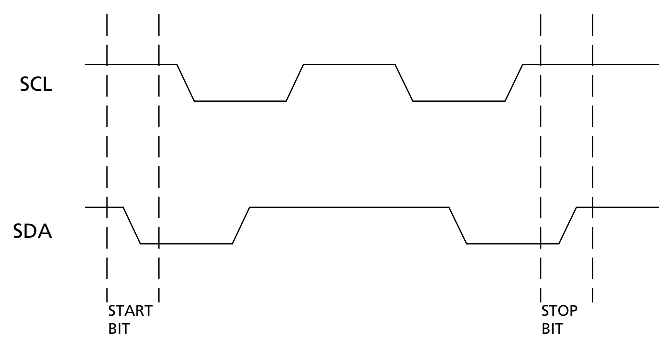


Figure 13: Acknowledge Response from Receiver

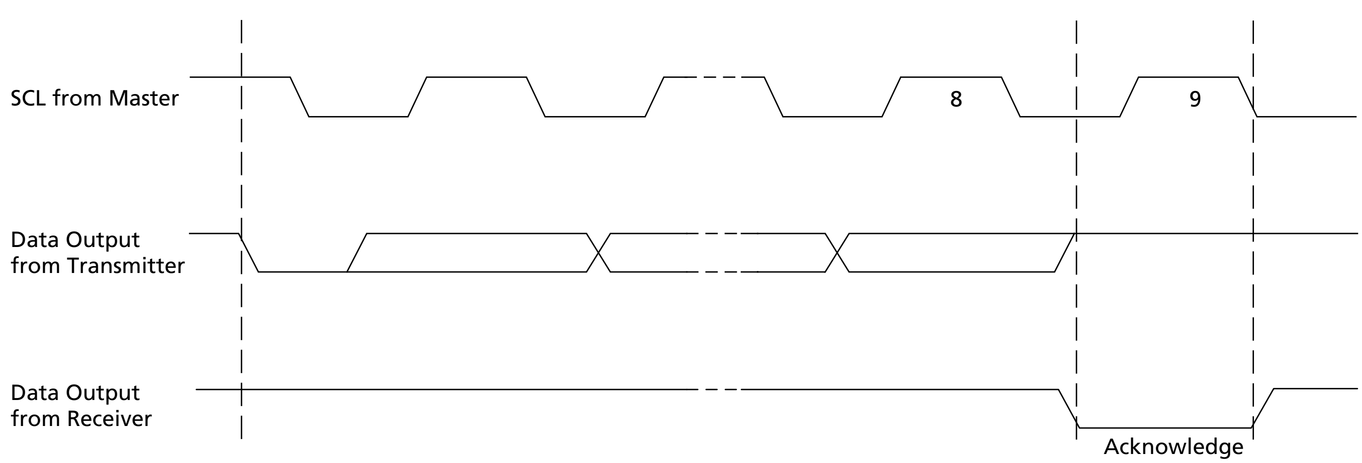


Table 21: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	R$\overline{W}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	R$\overline{W}$

Table 22: EEPROM Operating Modes

MODE	R$\overline{W}$ BIT	$\overline{WC}$	BYTES	INITIAL SEQUENCE
Current Address Read	1	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘1’
Random Address Read	0	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘0’, Address
	1	V_{IH} or V_{IL}	1	reSTART, Device Select, R$\overline{W}$ = ‘1’
Sequential Read	1	V_{IH} or V_{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{W}$ = ‘0’
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = ‘0’

Table 23: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DDSPD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

Figure 14: SPD EEPROM Timing Diagram

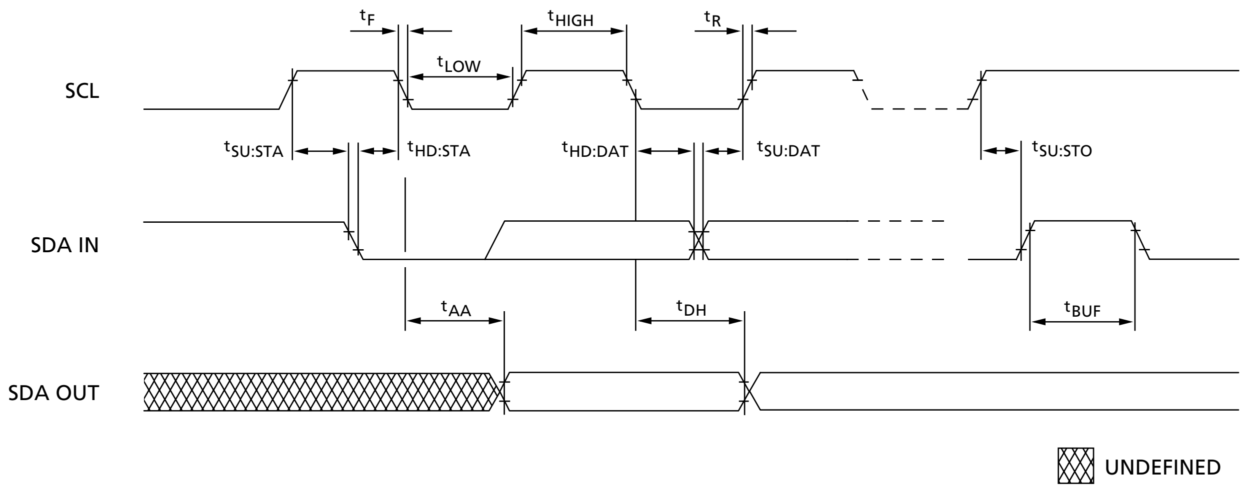


Table 24: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
ClockHIGHperiod	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	1

NOTE:

1. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 25: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes at end of SPD Matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT36VDDS12872D/ MT36VDDT12872D	MT36VDDS25672D/ MT36VDDT25672D
0	Number of Bytes Used by Micron	128	80	80
1	Total Number of SPD Memory Bytes	256	08	08
2	Memory Type	DDR SDRAM	07	07
3	Number of Row Addresses	13	0D	0D
4	Number of Column Addresses	10 or 11	0A	0B
5	Number of Module Ranks	4	04	04
6	Module Data Width	72	48	48
7	Module Data Width (continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, ^{t}CK, CAS Latency = 2.5, (See note 1)	7ns(-262/-26A) 7.5ns (-265) 8ns (-202)	70 75 80	70 75 80
10	SDRAM Access From Clock, ^{t}AC, CAS Latency = 2.5	0.75ns (-262/-26A/-265) 0.8ns (-202)	75 80	75 80
11	Module Configuration Type	ECC	02	02
12	Refresh Rate/ Type	7.81µs/SELF	82	82
13	SDRAM Width (Primary SDRAM)	8	08	08
14	Error-checking SDRAM Data Width	8	08	08
15	Minimum Clock Delay, Back-to-Back Random Column Access	1	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Registered, PLL	26	26
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0	C0
23	SDRAM Cycle Time, ^{t}CK,CAS Latency = 2	7.5ns (-262/-26A) 10ns (-265/-202)	75 A0	75 A0
24	SDRAM Cycle Time, ^{t}CK, CAS Latency = 2	7.5ns	75	75
25	SDRAM Cycle Time, ^{t}CK, CAS Latency = 1	–	00	00
26	SDRAM Access From CK, ^{t}AC, CAS Latency = 1	–	00	00
27	Minimum Row Precharge Time, ^{t}RP	15ns (-262) 20ns (-26A/-265/-202)	3C 50	3C 50
28	Minimum Row Active to Row Active, ^{t}RRD	15ns	3C	3C
29	Minimum RAS# to CAS# Delay, ^{t}RCD	15ns (-262) 20ns (-26A/-265/-202)	3C 50	3C 50
30	Minimum RAS# Pulse Width, ^{t}RAS (See note 2)	45ns (-262/-26A/-265) 40ns (-202)	2D 28	2D 28
31	Module Rank Density	256MB or 512MB	40	80
32	Address and Command Setup Time, ^{t}IS, (See note 3)	1.0ns (-262/-26A/-265) 1.1ns (-202)	A0 B0	A0 B0
33	Address and Command Hold Time, ^{t}IH (See note 3)	1.0ns (-262/-26A/-265) 1.1ns (-202)	A0 B0	A0 B0

Table 25: Serial Presence-Detect Matrix

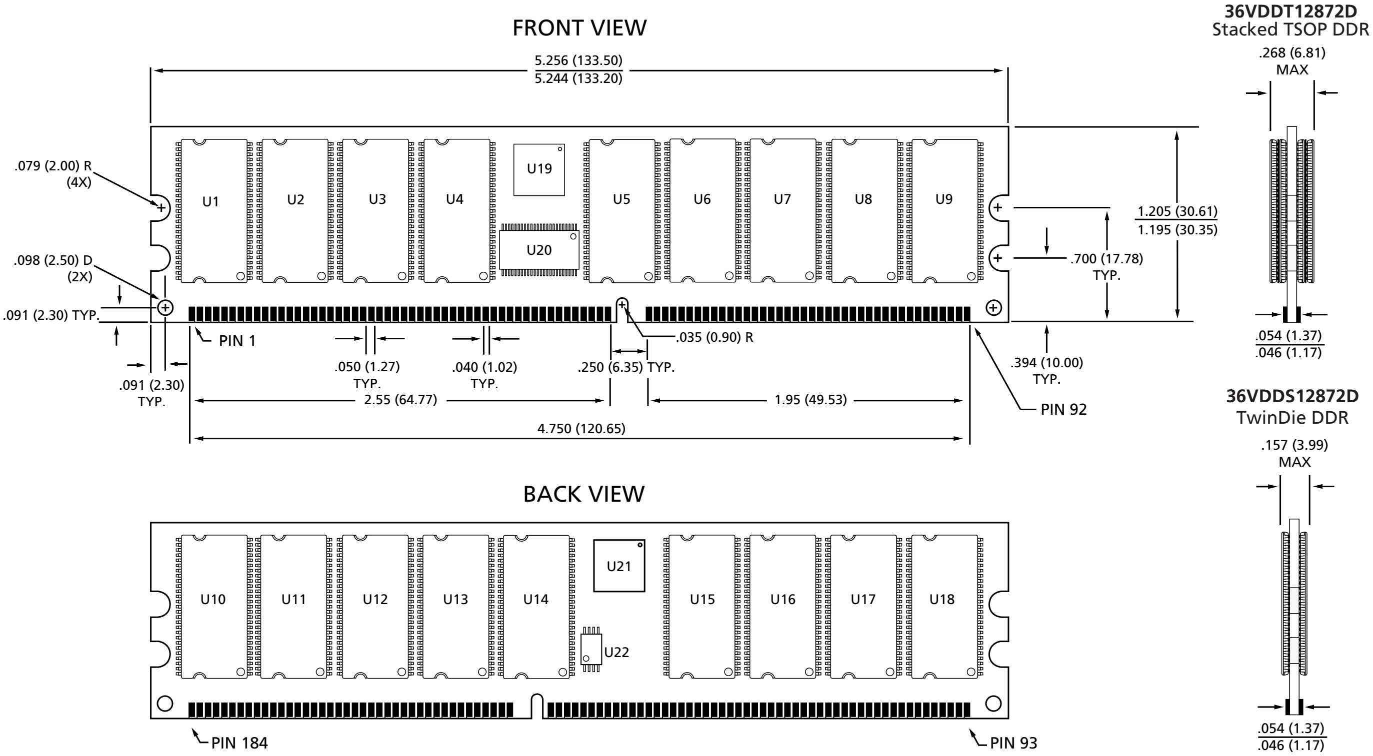
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes at end of SPD Matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT36VDDS12872D/ MT36VDDT12872D	MT36VDDS25672D/ MT36VDDT25672D
34	Data/Data Mask Input Setup Time, ^{t}DS	0.5ns (-262/-26A/-265) 0.6ns (-202)	50 60	50 60
35	Data/Data Mask Input Hold Time, ^{t}DH	0.5ns (-262/-26A/-265) 0.6ns (-202)	50 60	50 60
36-40	Reserved		00	00
41	Minimum Active/auto Refresh Time, ^{t}RC	60ns (-262) 65ns (-26A/-265) 70ns (-202)	3C 41 46	3C 41 46
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, ^{t}RFC	75ns (-262/-26A/-265) 80ns (-202)	4B 50	4B 50
43	Maximum Cycle Time, ^{t}CK(MAX)	13ns	34	34
44	Maximum DQS-DQ SKEW TIME, ^{t}DQSQ	0.5ns (-262/-26A/-265) 0.6ns (-202)	32 3C	32 3C
45	Maximum Read Data Hold Skew Factor, ^{t}QHS	0.75ns (-262/-26A/-265) 1.0ns (-202)	75 A0	75 A0
46	Reserved		00	00
47	DIMM Height		01	01
48–61	Reserved		00	00
62	SPD Revision	Release 1.0	10	10
63	Checksum for Bytes 0-62	-262 -26A -265 -202	D5 02 32 CD	16 43 73 0E
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code	(continued)	FF	FF
72	Manufacturing Location	1 - 12	01 - 0C	01 - 0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1 - 9	01-09	01-09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–

NOTE:

1. Value for -26A ^{t}CK set to 7ns (0x70) for optimum BIOS compatibility. Actual device spec. value is 7.5ns.
2. The value of ^{t}RAS for -262, -26A, and -265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec. value is 40ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

Figure 15: Low-Profile 184-Pin DIMM (Quad Rank)



NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Advance: This data sheet contains initial descriptions of products still under development.

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