5A, 26V, 380kHz, Synchronous Step-Down Converter

Features

- **Wide Input Voltage from 4.5V to 26V**
- **Output Current Up to 5A**
- **Adjustable Output Voltage from 0.8V to 90%V_{IN}**
  - **- 0.8V Reference Voltage**
  - **- ±2.5% System Accuracy**
- **Integrated 50mW P-Channel Power MOSFET and 20mW N-Channel Power MOSFET**
- **High Efficiency up to 95%**
- **Current-Mode Operation**
  - **- Stable with Ceramic Output Capacitors**
  - **- Fast Transient Response**
- **Power-On-Reset Monitoring**
- **Fixed 380kHz Switching Frequency in PWM Mode**
- **Automatic Pulse-Skipping Mode (PSM)/PWM Mode Operation**
- **Built-in Digital Soft-Start**
- **Output Current-Limit Protection with Frequency Foldback**
- **70% Under-Voltage Protection**
- **Over-Temperature Protection**
- **118% Over-Voltage Protection**
- **<5mA Quiescent Current During Shutdown**
- **Thermal-Enhanced TQFN5x6-28 Package**
- **Pb-Free Available as an Option**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD Monitor / TV**
- **SetTop Box**
- **Portable DVD**
- **Wireless LAN**
- **ADSL, Switch HUB**
- **Notebook Computer**
- **Step-Down Converters Requiring High Efficiency and 5A Output Current**

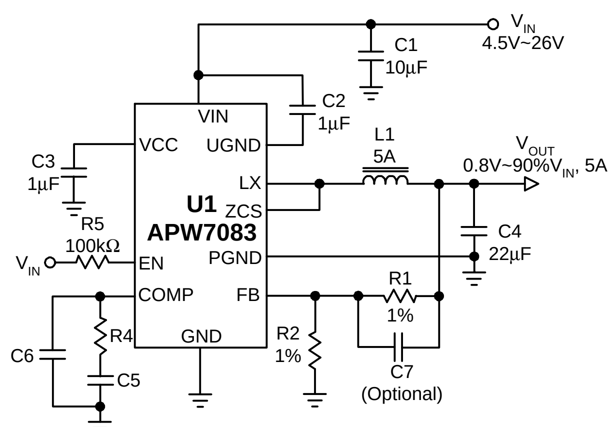
General Description

The APW7083 is a 5A, synchronous, step-down converter with integrated 50mΩ P-channel power MOSFET and 20mΩ N-channel power MOSFET. The device, with current-mode control scheme, can convert 4.5~26V input voltage to the output voltage adjustable from 0.8 to 90% V_{IN} to provide excellent output voltage regulation.

The APW7083 regulates the output voltage in an automatic PSM/PWM mode operation, depending on the output current, for high efficiency operation over light to full load current. The APW7083 is also equipped with power-on-reset, soft-start, and whole protections (including over-voltage, under-voltage, over-temperature, and current-limit) in a single package. In shutdown mode, the supply current drops below 5µA.

This device, available in 28-pin TQFN5x6 package, provides a very compact system solution with minimal external components and good thermal conductance.

Simplified Application Circuit



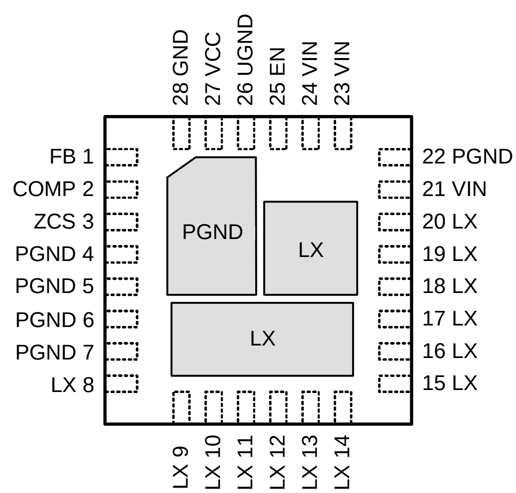
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7083 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN5x6-28 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7083 QB : APW7083 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN5x6-28
(Top View)

□ = Thermal Pad (connected to copper plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)		-0.3 ~ 30	V
V_{LX} V_{ZCS}	LX to GND Voltage ZCS to GND Voltage	> 100ns	-1 ~ V_{IN} +0.3	V
		< 100ns	-5 ~ V_{IN} +6	
V_{CC}	VCC Supply Voltage (VCC to GND)	V_{IN} > 6.2V	-0.3 ~ 6.5	V
		$V_{IN} \leq$ 6.2V	V_{IN}+0.3	
V_{UGND_GND}	UGND to GND Voltage		-0.3 ~ V_{IN}+0.3	V
V_{VIN_UGND}	VIN to UGND Voltage		-0.3 ~ 6.5V	V
	EN to GND Voltage		20	V
	FB, COMP to GND Voltage		-0.3 ~ V_{CC} +0.3	V
	Maximum Junction Temperature		150	^{o}C
T_{STG}	Storage Temperature		-65 ~ 150	^{o}C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	^{o}C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TQFN5x6-28	75	^{o}C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 26	V
	VCC Supply Voltage	4.0 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.8 ~ 90% V_{IN}	V
I_{OUT}	Converter Output Current	0 ~ 5	A
	VCC Input Capacitor	0.22 ~ 2.2	µF
	VIN-to-UGND Input Capacitor	0.22 ~ 2.2	µF
T_A	Ambient Temperature	-40 ~ 85	^{o}C
T_J	Junction Temperature	-40 ~ 125	^{o}C

Note 3: Refer to the typical application circuits.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A=-40~85°C, unless otherwise specified. V_{CC} is regulated by an internal regulator. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7083			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB} = 0.85V, V_{EN} = 3V, LX = Open	-	1.0	2.0	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN} = 0V, V_{IN} = 26V	-	-	5	μA
I_{VCC}	VCC Supply Current	V_{EN} = 3V, V_{CC} = 5.0V	-	0.7	-	mA
I_{VCC_SD}	VCC Shutdown Supply Current	V_{EN} = 0V, V_{CC} = 5.0V	-	-	1	μA
VCC 4.2V LINEAR REGULATOR						
	Output Voltage	V_{IN} = 5.2 ~ 26V, I_O = 0 ~ 8mA	4.0	4.2	4.5	V
	Load Regulation	I_O = 0 ~ 8mA	-60	-40	0	mV
	Current-Limit	V_{CC} > POR Threshold	8	-	30	mA
VIN-TO-UGND 5.5V LINEAR REGULATOR						
	Output Voltage ($V_{VIN-UGND}$)	V_{IN} = 6.2 ~ 26V, I_O = 0 ~ 10mA	5.3	5.5	5.7	V
	Load Regulation	I_O = 0 ~ 10mA	-80	-60	0	mV
	Current-Limit	V_{IN} = 6.2 ~ 26V	10	-	30	mA
POWER-ON-RESET (POR) AND LOCKOUT VOLTAGE THRESHOLDS						
	VCC POR Voltage Threshold	V_{CC} rising	3.7	3.9	4.1	V
	VCC POR Hysteresis		-	0.15	-	V
	EN Lockout Voltage Threshold	V_{EN} rising	2.4	2.5	2.6	V
	EN Lockout Hysteresis		-	0.2	-	V
	VIN-to-UGND Lockout Voltage Threshold	$V_{VIN-UGND}$ rising	-	3.5	-	V
	VIN-to-UGND Lockout Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.8	-	V
	Output Voltage Accuracy	T_J = 25°C, I_{OUT} = 0A, V_{IN} = 12V	-1	-	+1	%
		T_J = -40 ~ 125°C, I_{OUT} = 0 ~ 3A, V_{IN} = 4.5 ~ 26V	-2.5	-	+2.5	
	Line Regulation	V_{IN} = 4.5V to 26V, I_{OUT} = 0A	-	0.1	-	%
	Load Regulation	I_{OUT} < 1A	-	-0.3	-	%/A
		I_{OUT} = 1 ~ 5A	-	-0.53	-	
OSCILLATOR AND DUTY						
F_{OSC}	Oscillator Running Frequency	V_{IN} = 4.5 ~ 26V	340	380	420	kHz
	Foldback Frequency	V_{FB} = 0V	-	80	-	kHz
	Maximum Converter's Duty Cycle		-	93	-	%
	Minimum Pulse Width of LX	V_{IN} = 4.5 ~ 26V	-	200	-	ns
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	400	-	μA/V
	Error Amplifier DC Gain	COMP = Open	60	80	-	dB

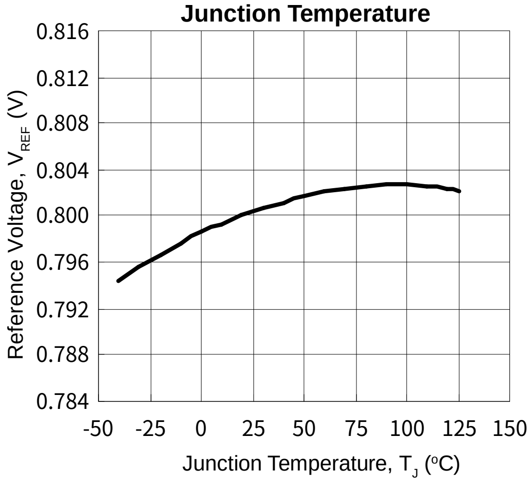
Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A=-40~85°C, unless otherwise specified. V_{CC} is regulated by an internal regulator. Typical values are at T_A=25°C.

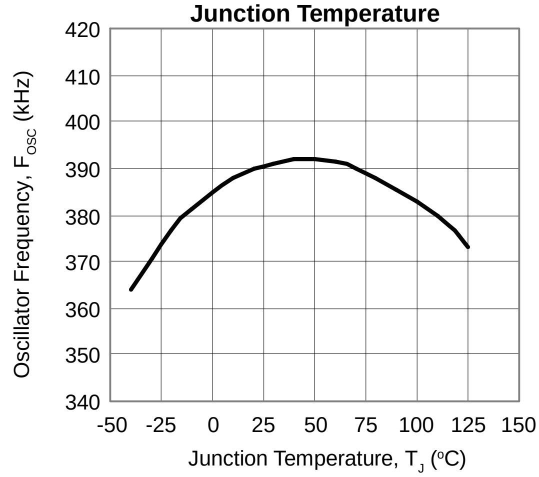
Symbol	Parameter	Test Conditions	APW7083			Unit
			Min.	Typ.	Max.	
CURRENT-MODE PWM CONVERTER (CONT.)						
	Current-Sense Resistance		-	0.12	-	Ω
	High-side Switch Resistance	Between VIN and Exposed Pad, T_J = 25°C	-	50	80	mΩ
	Low-side Switch Resistance	Between GND and Exposed Pad, T_J = 25°C	-	20	30	mΩ
PROTECTIONS						
I_{LIM}	P-Channel Power MOSFET Current-Limit	Peak Current	6	8	10	A
V_{UV}	FB Under-Voltage Threshold	V_{FB} falling	66	70	74	%
	FB Under-Voltage Hysteresis		-	40	-	mV
	FB Under-Voltage Debounce		-	2	-	μs
V_{OV}	FB Over-Voltage Threshold	V_{FB} Rising	114	118	122	%
	FB Over-Voltage Hysteresis		-	40	-	mV
T_{OTP}	Over-Temperature Trip Point		-	150	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
T_D	Dead-Time	V_{LX} = -0.7V, V_{IN} = 4.5 ~ 26V	-	30	-	ns
SOFT-START, ENABLE, AND INPUT CURRENTS						
t_{SS}	Soft-Start Interval		-	8	-	ms
	Preceding Delay before Soft-Start		-	11	-	ms
	EN Logic Low Voltage	V_{EN} falling, V_{IN} = 4.5 ~ 26V	-	-	0.5	V
	EN Logic High Voltage	V_{EN} rising, V_{IN} = 4.5 ~ 26V	2.1	-	-	V
	EN Pin Clamped Voltage	I_{EN} = 10mA	12	-	17	V
	P-Channel Power MOSFET Leakage Current	V_{EN} = 0V, V_{LX} = 0V, V_{IN} = 26V	-	-	4	μA
I_{FB}	FB Pin Input Current	V_{FB} = 0.8V	-100	-	+100	μA
I_{EN}	EN Pin Input Current	V_{EN} < 3V	-500	-	+500	μA

Typical Operating Characteristics

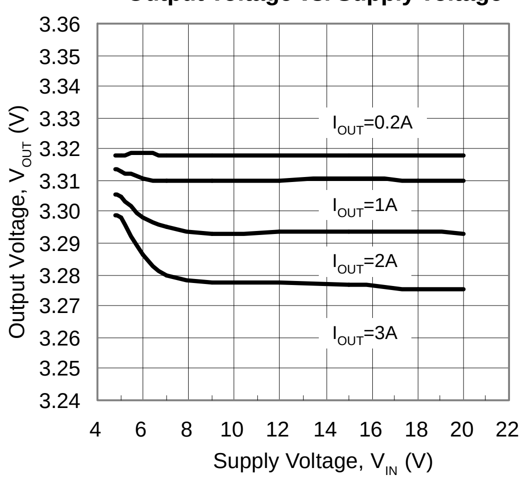
Reference Voltage vs. Junction Temperature



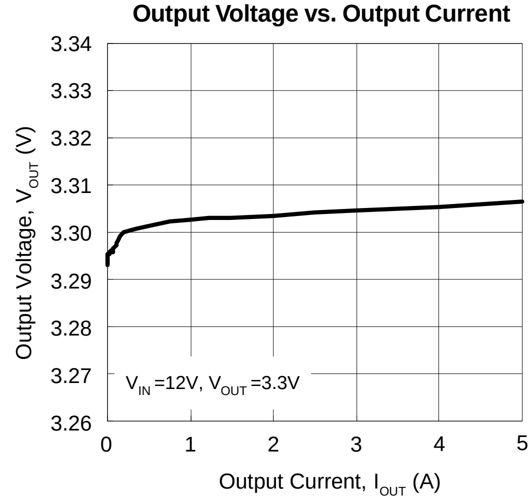
Oscillator Frequency vs. Junction Temperature



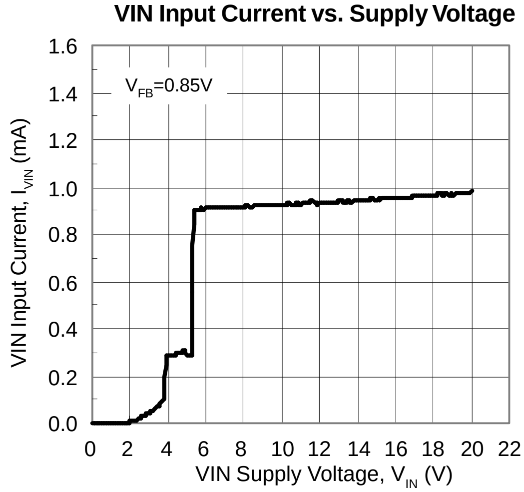
Output Voltage vs. Supply Voltage



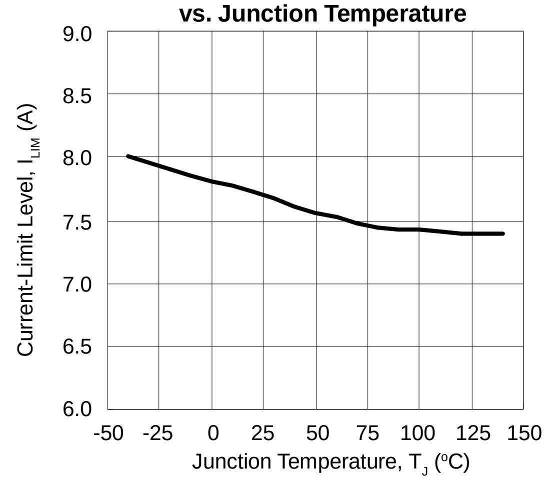
Output Voltage vs. Output Current



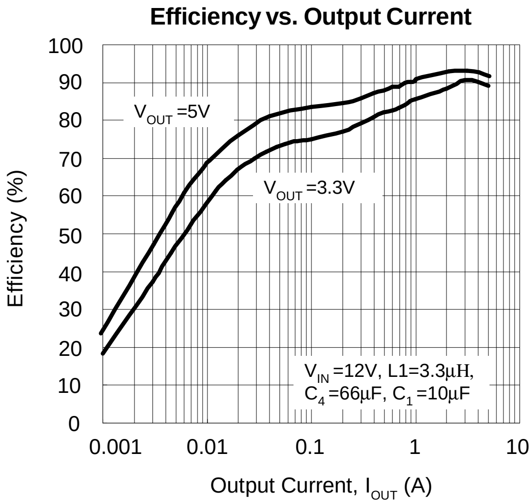
VIN Input Current vs. Supply Voltage

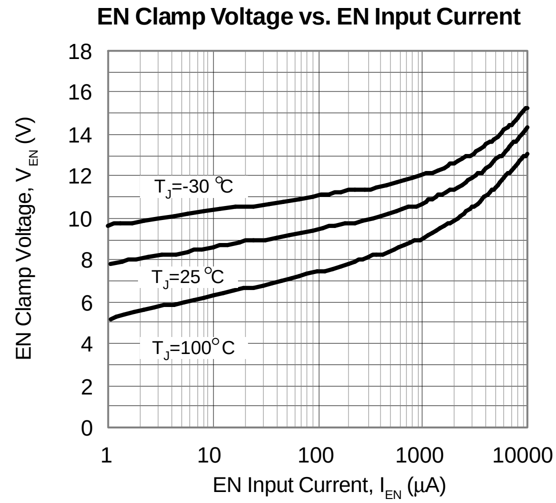


Current-Limit Level (Peak Current) vs. Junction Temperature



Typical Operating Characteristics (Cont.)

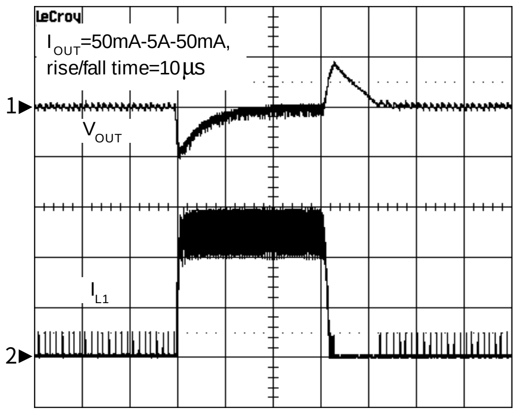




Operating Waveforms

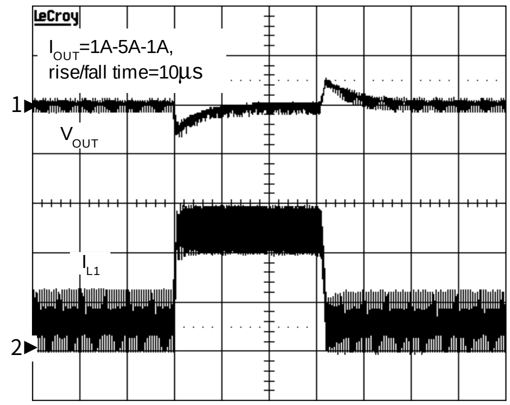
Refer to the “Typical Application Circuit”. The test conditions are V_{IN}=12V, V_{OUT}=3.3V, L1=3.3μH, C4=66μF, T_A= 25°C unless otherwise specified.

Load Transient Response



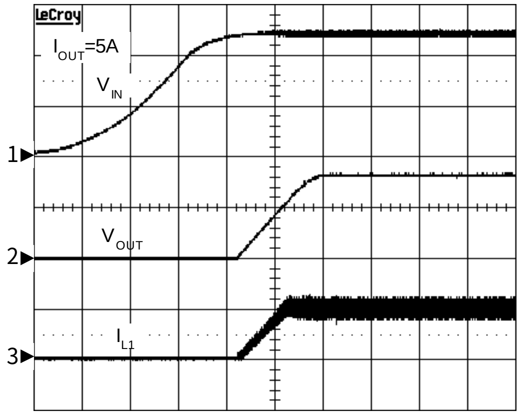
CH1: V_{OUT}, 200mV/Div, offset=3.3V
CH2: I_{L1}, 2A/Div, DC
TIME: 100μs/Div

Load Transient Response



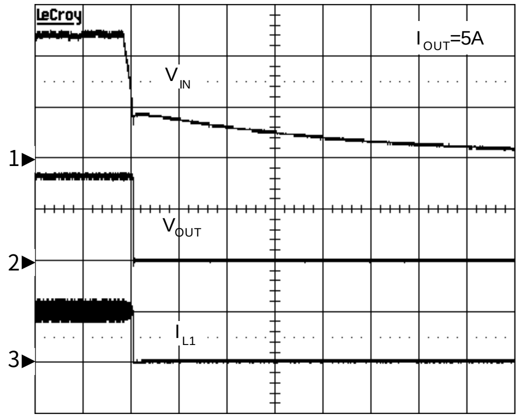
CH1: V_{OUT}, 200mV/Div, offset=3.3V
CH2: I_{L1}, 2A/Div, DC
TIME: 100μs/Div

Power On



CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{L1}, 5A/Div, DC
TIME: 5ms/Div

Power Off

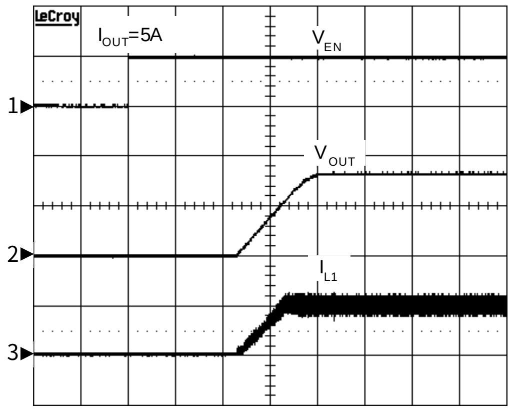


CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{L1}, 5A/Div, DC
TIME: 5ms/Div

Operating Waveforms (Cont.)

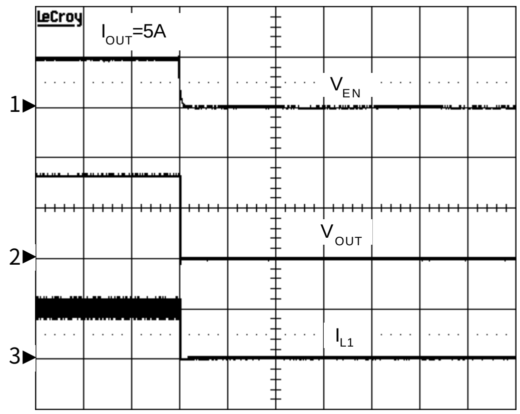
Refer to the "Typical Application Circuit". The test conditions are V_{IN}=12V, V_{OUT}=3.3V, L1=3.3µH, C4=66µF, T_A= 25°C unless otherwise specified.

Enable Through EN Pin



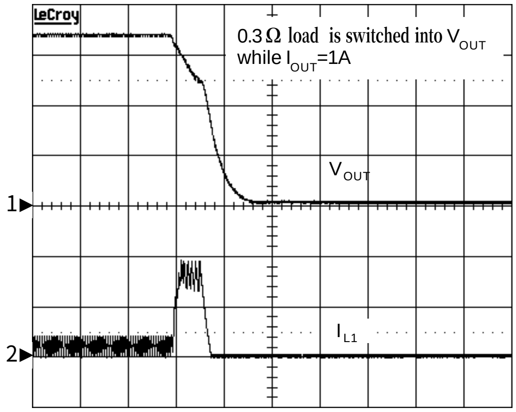
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{L1}, 5A/Div, DC
TIME: 5ms/Div

Shutdown Through EN Pin



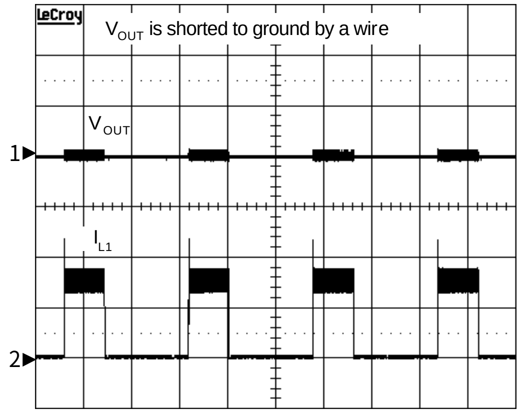
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{L1}, 5A/Div, DC
TIME: 5ms/Div

Over Current



CH1: V_{OUT}, 1V/Div, DC
CH2: I_{L1}, 5A/Div, DC
TIME: 50µs/Div

Short Circuit

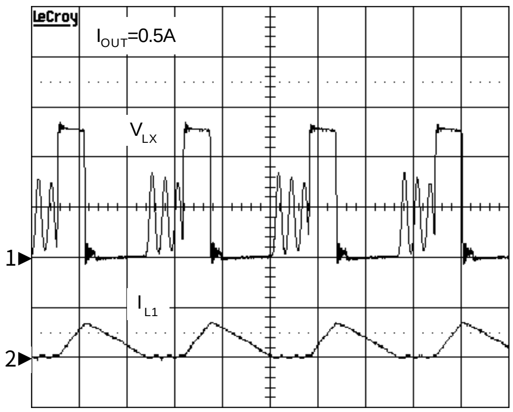


CH1: V_{OUT}, 1V/Div, DC
CH2: I_{L1}, 5A/Div, DC
TIME: 50ms/Div

Operating Waveforms (Cont.)

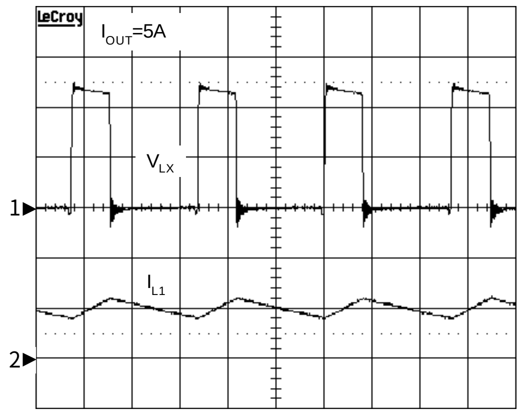
Refer to the "Typical Application Circuit". The test conditions are V_{IN}=12V, V_{OUT}=3.3V, L1=3.3μH, C4=66μF, T_A= 25°C unless otherwise specified.

Switching Waveform



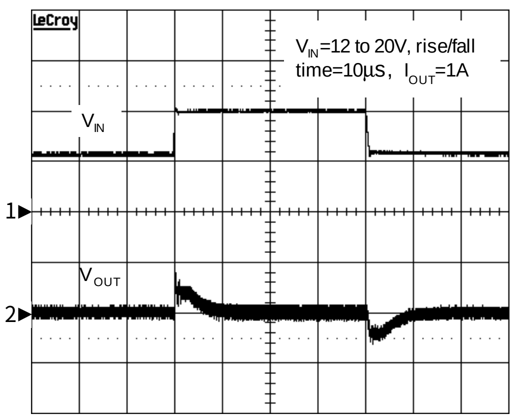
CH1: V_{LX}, 5V/Div, DC
CH2: I_{L1}, 2A/Div, DC
TIME: 1μs/Div

Switching Waveform



CH1: V_{LX}, 5V/Div, DC
CH2: I_{L1}, 2A/Div, DC
TIME: 1μs/Div

Line Transient Response

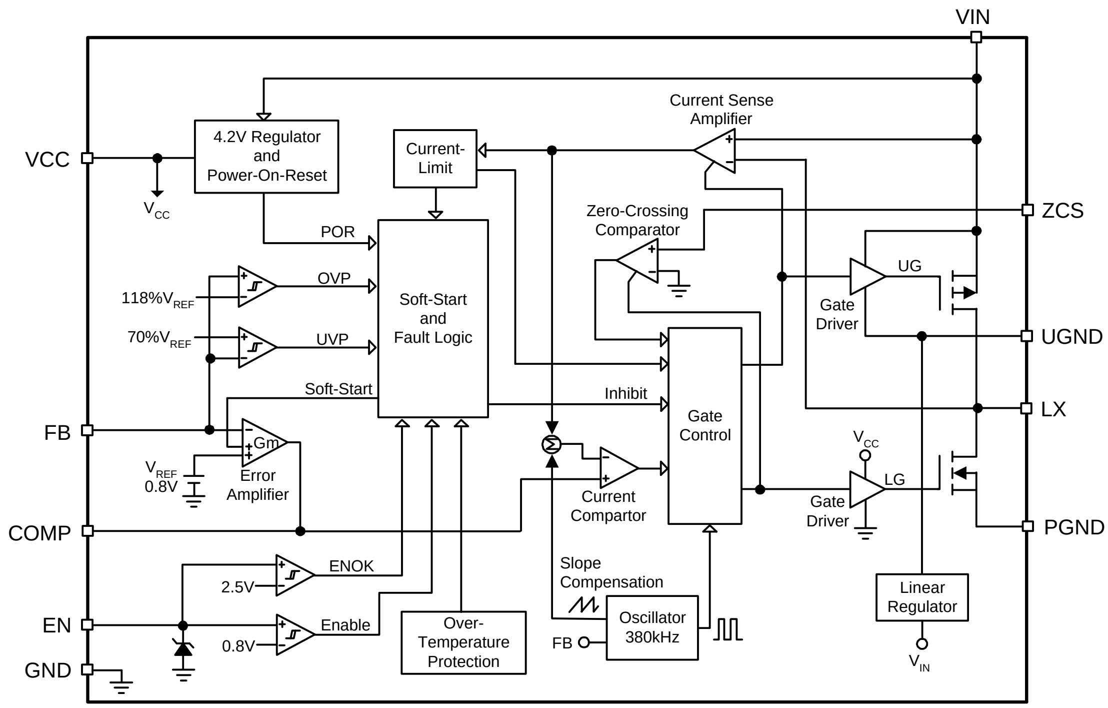


CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 100mV/Div, offset=3.3V
TIME: 100μs/Div

Pin Description

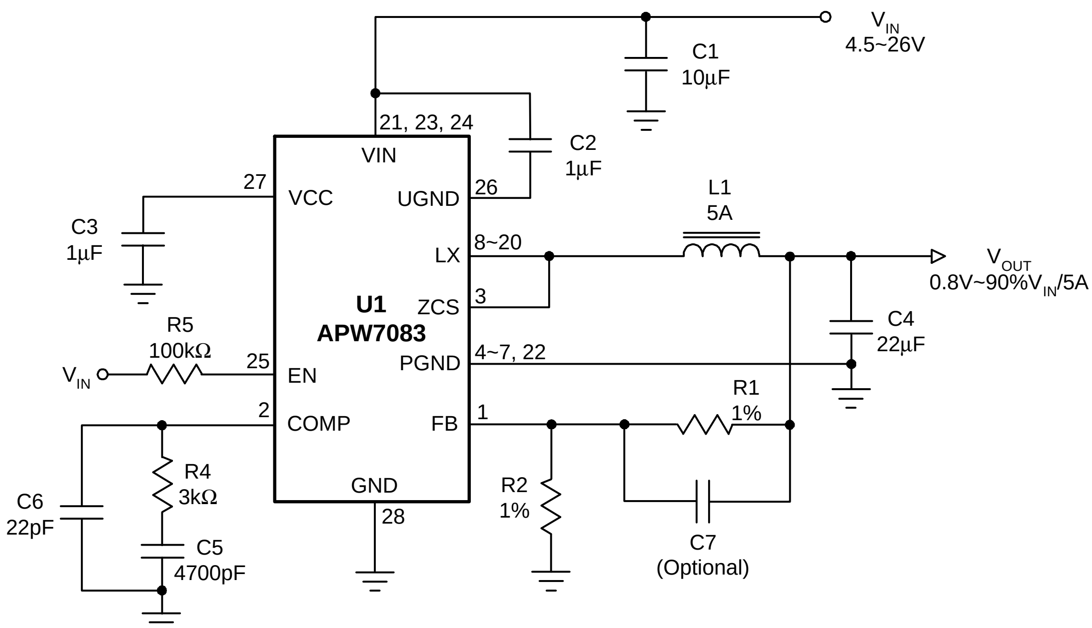
PIN		FUNCTION
NO.	NAME	
1	FB	Feedback Input. The IC senses feedback voltage via FB and regulate the voltage at 0.8V. Connecting FB with a resistor-divider from the output set the output voltage in the range from 0.8V to 90% V_{IN}.
2	COMP	Output of error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required for noise decoupling.
3	ZCS	Zero-Crossing Sense pin. Please externally connect this pin with LX.
4~7, 22	PGND	POWER Ground pins. All these pins must be connected externally to the power ground plane.
8~20	LX	Power Switching Output. Connect this pin to the underside Exposed Pad.
21, 23, 24	VIN	Power Input. VIN supplies the power (4.5V to 26V) to the control circuitry, gate driver and step-down converter switch. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and GND eliminates switching noise and voltage ripple on the input to the IC.
25	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic start-up.
26	UGND	Gate driver power ground of the P-channel Power MOSFET. A linear regulator regulates a 5.5V voltage between VIN and UGND to supply power to P-channel MOSFET gate driver. Connect a ceramic capacitor (1µF typ.) between VIN and UGND for noise decoupling and stability of the linear regulator.
27	VCC	Bias input and 4.2V linear regulator's output. This pin supplies the bias to some control circuits. The 4.2V linear regulator converts the voltage on VIN to 4.2V to supply the bias when no external 5V power supply is connected with VCC. Connect a ceramic capacitor (1µF typ.) between VCC and GND for noise decoupling and stability of the linear regulator.
28	GND	Signal Ground.

Block Diagram



Typical Application Circuit

4.5~26V Single Power Input Step-down Converter (with Ceramic Input/Output Capacitors)



Recommended Feedback Compensation Network Components List:

V_{IN} (V)	V_{OUT} (V)	L1 (µH)	C4 (µF)	C4 ESR (mΩ)	R1 (kΩ)	R2 (kΩ)	C7 (pF)	R4 (kΩ)	C5 (pF)	C6 (pF)
12	5	3.3	66	3	63.4	12	68	24	1000	22
12	3.3	3.3	66	3	47	15	82	20	1500	22
12	1.2	3.3	66	3	7.5	15	270	12	2200	22

Function Description

Main Control Loop

The APW7083 is a constant frequency current mode switching regulator. During normal operation, the internal P-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and would be turned off when an internal current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier (EAMP). An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

VCC Power-On-Reset (POR) and EN Undervoltage Lockout

The APW7083 keeps monitoring the voltage on VCC pin to prevent wrong logic operations which may occur when VCC voltage is not high enough for the internal control circuitry to operate. The VCC POR has a rising threshold of 3.9V (typical) with 0.15V of hysteresis.

An external undervoltage lockout (UVLO) is sensed and programmed at the EN pin. The EN UVLO has a rising threshold of 2.5V with 0.2V of hysteresis. The EN UVLO should be programmed by connecting a resistive divider from VIN to EN to GND.

After the VCC, EN, and VIN-to-UGND voltages exceed their respective voltage thresholds, the IC starts a start-up process and then ramps up the output voltage to the setting of output voltage. Connecting a RC network from EN to GND is for setting a turn-on delay that can be used to sequence the output voltages of multiple devices.

VCC 4.2V Linear Regulator

VCC is the output terminal of the internal 4.2V linear regulator which is powered from VIN and provides power to the APW7083. The linear regulator designed to be stable with a low-ESR ceramic output capacitor powers the internal control circuitry, then bypasses VCC to GND with a ceramic capacitor of at least 0.22μF. In order to provide good noise decoupling, please place the capacitor physically close to the IC. The linear regulator is not intended for powering up any external loads. Do not connect any external load to VCC. The linear regulator is also equipped with current-limit protection to protect itself during overload or short-circuit conditions on VCC pin.

VIN-to-UGND 5.5V Linear Regulator

The built-in 5.5V linear regulator regulates a 5.5V voltage between VIN and UGND pins to supply bias and gate charge for the P-channel Power MOSFET gate driver. The linear regulator is designed to be stable with a low-ESR ceramic output capacitor of at least 0.22μF. It is also equipped with current-limit function to protect itself during over-load or short-circuit conditions between VIN and UGND.

The APW7083 shuts off the output of the converters when the output voltage of the linear regulator is below 3.5V (typical). The IC resumes working by initiating a new soft-start process when the linear regulator's output voltage is above the undervoltage lockout voltage threshold.

Digital Soft-Start

The APW7083 has a built-in digital soft-start to control the output voltage rise and limit the input current surge during start-up. During soft-start, an internal ramp, connected to the one of the positive inputs of the error amplifier, rises up from 0V to 1V to replace the reference voltage (0.8V) until the ramp voltage reaches the reference voltage.

The device is designed with a preceding delay about 10.8ms (typical) before soft-start process.

Enable/Shutdown

Driving EN to ground places the APW7083 in shutdown. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current of VIN reduces to <1μA (typical).

Output Under-Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the re-

Function Description (Cont.)

Output Under-Voltage Protection (Cont.)

quired regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output. The under-voltage threshold is 70% of the nominal output voltage. The under-voltage comparator has a built-in 2µs noise filter to prevent the chips from wrong UVP shutdown caused by noise. The under-voltage protection works in a hiccup mode without latched shutdown. The IC will initiate a new soft-start process at the end of the proceeding delay.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7083. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the power MOSFET, allowing the devices to cool. The thermal sensor allows the converter to start a start-up process and regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Over-Voltage Protection

The over-voltage function monitors the output voltage by FB pin. The FB voltage should increase over 118% of the reference voltage due to the high-side MOSFET failure, or for other reasons, the over-voltage protection comparator, will force the low-side MOSFET gate driver high. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chips will restore its normal operation. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver - a common problem for OVP schemes with a latch.

Current-Limit Protection

The APW7083 monitors the output current, flowing through the P-channel power MOSFET, and limits the current peak at current-limit level to prevent loads and the IC from damages during overload or short-circuit conditions.

Frequency Foldback

When the output is shortened to the ground, the frequency of the oscillator will be reduced to about 80kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage on FB approaches 0.8V again.

Application Information

Power Sequencing

The APW7083 can operate with single or dual power input (s). In dual-power application, the voltage (V_{CC}) applied at VCC pin must be lower than the voltage (V_{IN}) on VIN pin. The internal parasitic diode from VCC to VIN will conduct due to the forward-voltage between VCC and VIN. Therefore, V_{IN} must be provided before V_{CC}.

Setting Output Voltage

The regulated output voltage is determined by:

$$V_{OUT} = 0.8 \cdot (1 + \frac{R1}{R2}) \quad (V)$$

Suggested R2 is in the range from 1k to 20kΩ. For portable applications, a 10k resistor is suggested for R2. To prevent stray pickup, please locate resistors R1 and R2 close to APW7083.

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time the P-channel power MOSFET (Q1) turns on. Place the small ceramic capacitors physically close to the VIN and between the VIN and GND.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current (I_{RMS}) of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad (A)$$

where D is the duty cycle of the power MOSFET.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

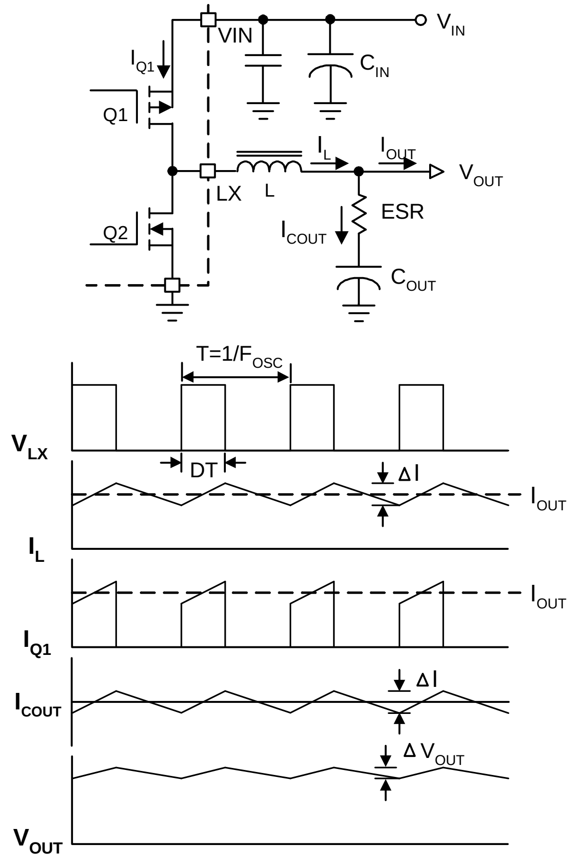


Figure 1. Converter Waveforms

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current (ΔI). The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calculated as the following equations:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{........... (1)}$$

$$\Delta I = \frac{V_{OUT} \cdot (1 - D)}{F_{OSC} \cdot L} \quad \text{........... (2)}$$

$$V_{ESR} = \Delta I \cdot ESR \quad \text{........... (3)}$$

The peak-to-peak voltage of the ideal output capacitor is calculated as the following equations:

Application Information (Cont.)

Output Capacitor Selection (Cont.)

$$\Delta V_{COUT} = \frac{\Delta I}{8 \cdot F_{OSC} \cdot C_{OUT}} \quad (V) \qquad \text{........... (4)}$$

For the applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is shown as below:

$$\Delta V_{OUT} = \Delta I \cdot ESR \quad (V) \qquad \text{........... (5)}$$

For the applications using ceramic capacitors, the V_{ESR} is much smaller than the ΔV_{COUT} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is close to ΔV_{COUT} .

The load transient requirement is a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses. The equation (2) shows that the inductance value has a direct effect on ripple current.

Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I \leq 0.4 \cdot I_{OUT(MAX)}$. Remember, the maximum ripple current occurs at the maximum input voltage. The minimum inductance of the inductor is calculated by using the following equation:

$$\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{380000 \cdot L \cdot V_{IN}} \leq 2$$

$$L \geq \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{760000 \cdot V_{IN}} \quad (H) \qquad \text{........... (6)}$$

where $V_{IN} = V_{IN(MAX)}$

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. Figure 2 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. The following is a checklist for your layout:

1. Firstly, to initial the layout by placing the power components. Orient the power circuitry to achieve a clean power flow path. If possible, make all the connections on one side of the PCB with wide, copper filled areas.
2. In Figure 2, the loops with the same color bold lines conduct high slew rate current. These interconnecting impedances should be minimized by using wide, short printed circuit traces.
3. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX or others) on the PCB. Therefore, place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.
4. The VCC decoupling capacitor should be right next to the VCC and GND pins. Capacitor C2 should be connected as close to the VIN and UGND pins as possible.
5. Place the decoupling ceramic capacitor C1 near the VIN as close as possible. The bulk capacitors C8 are also placed near VIN. Use a wide power ground plane to connect the C1, C8, and C4 to provide a low impedance

Application Information (Cont.)

Layout Consideration (Cont.)

path between the components for large and high slew rate current.

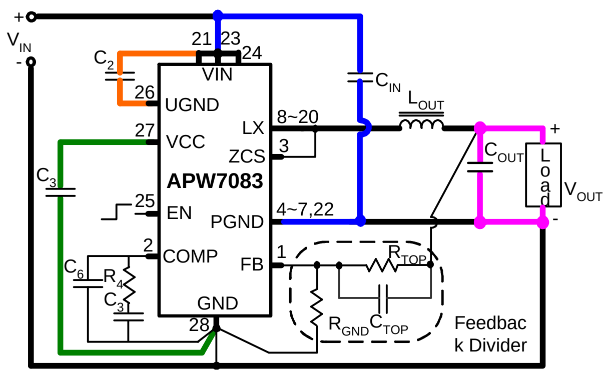


Figure 2. Current Path Diagram

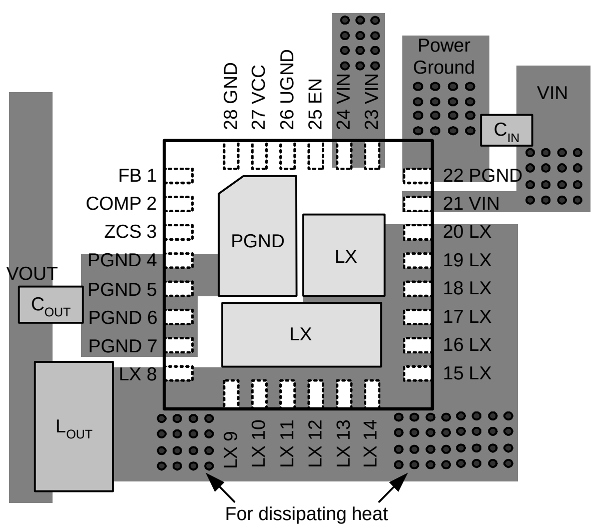


Figure 3. Recommended Layout Diagram

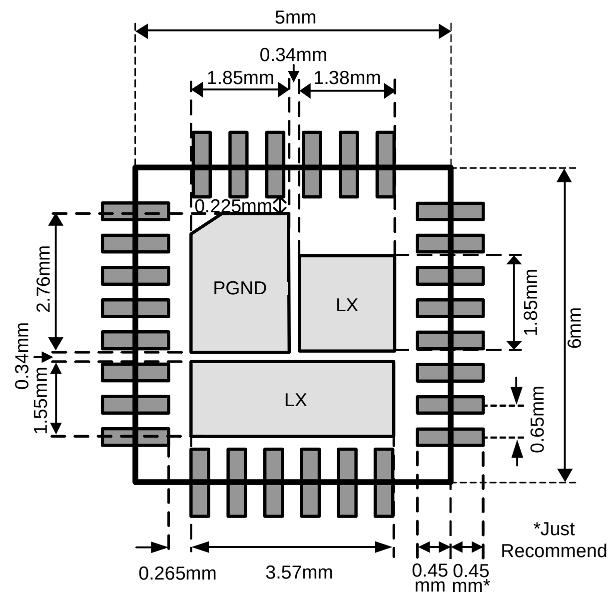
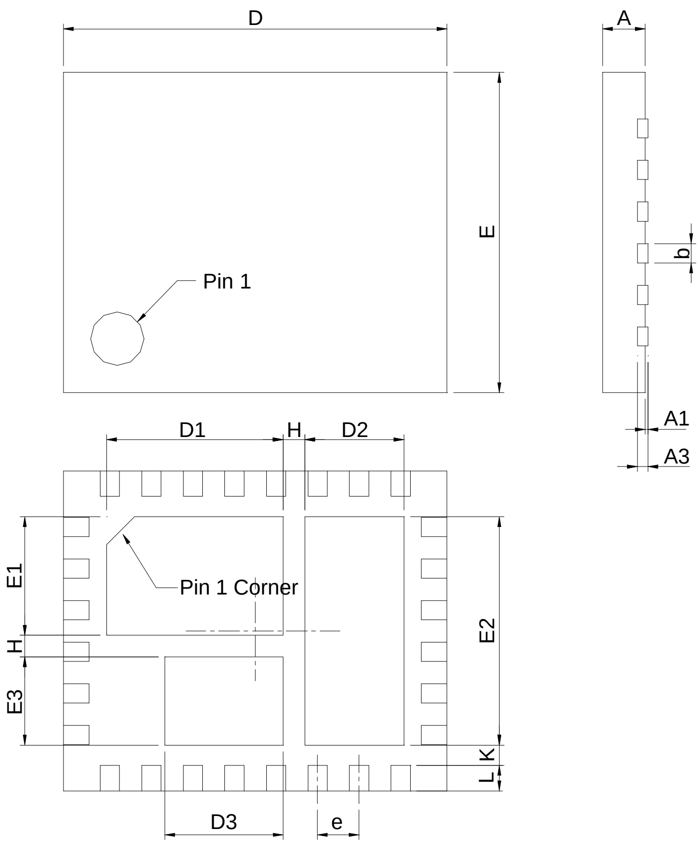


Figure 4. Recommended Minimum Footprint

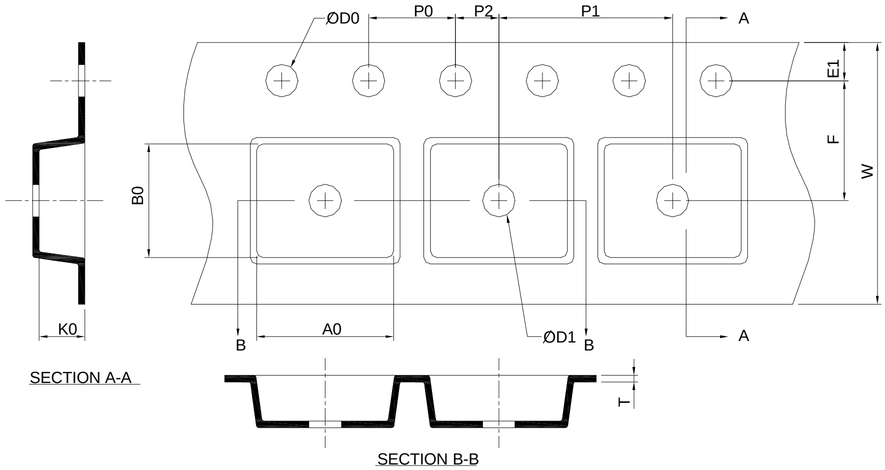
Package Information

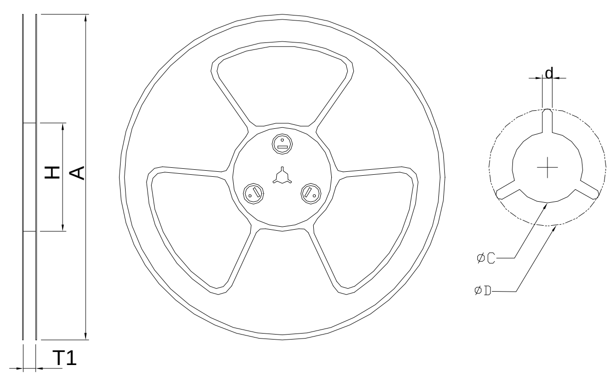
TQFN5x6-28



SYMBOL	TQFN5x6-28			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	5.90	6.10	0.232	0.240
D1	2.71	2.81	0.107	0.111
D2	1.50	1.60	0.059	0.063
D3	1.80	1.90	0.071	0.075
E	4.90	5.10	0.193	0.201
E1	1.80	1.90	0.071	0.075
E2	3.52	3.62	0.139	0.143
E3	1.33	1.43	0.052	0.056
e	0.65 BSC		0.026 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
H	0.34 REF		0.013 REF	

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TQFN5x6-28	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.3±0.05	6.5±0.10	5.3±0.10	1.4±0.10

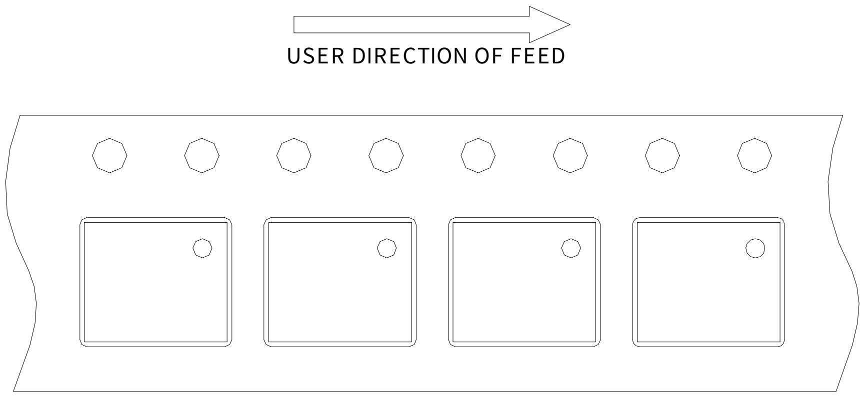
(mm)

Devices Per Unit

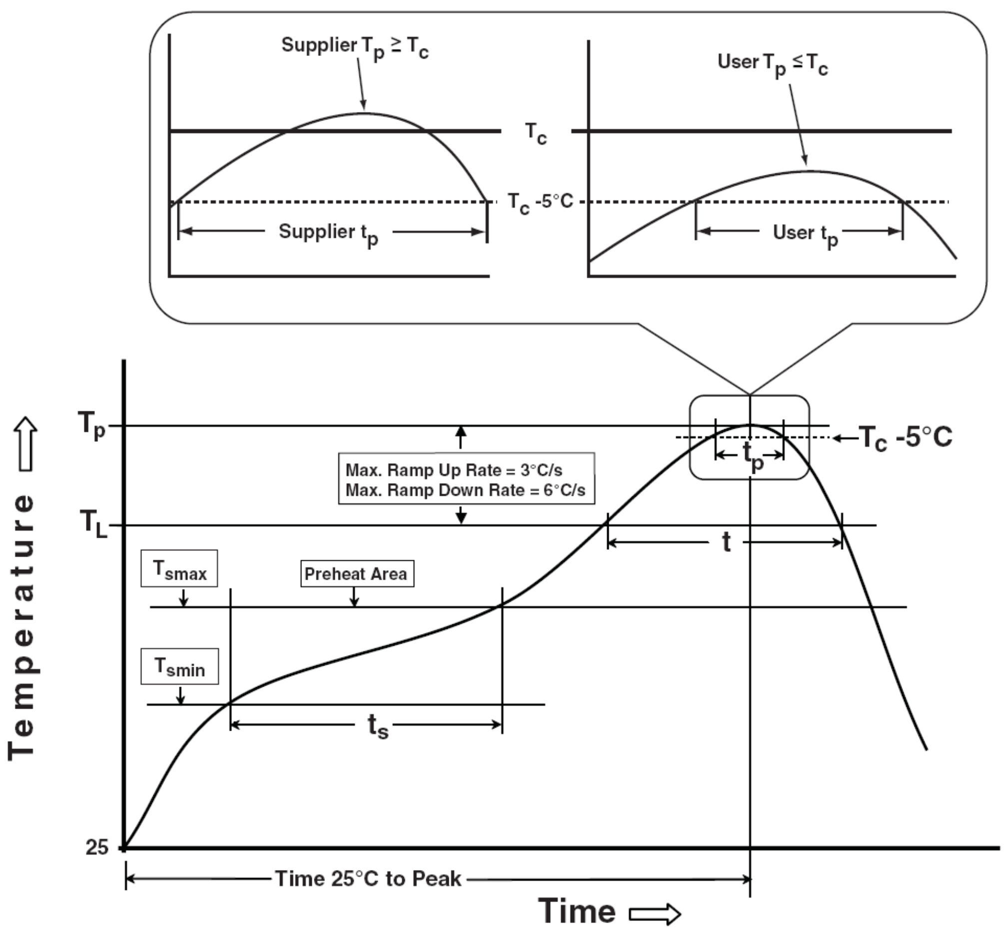
Package Type	Unit	Quantity
TQFN5x6-28	Tape & Reel	2500

Taping Direction Information

TQFN5x6-28



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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