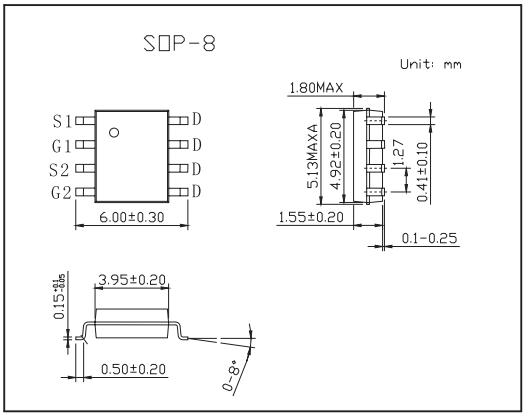
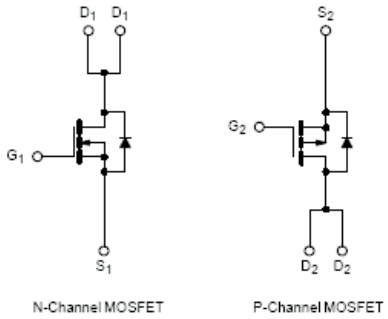
KI4562DY



■ PIN Configuration



N-Channel MOSFET P-Channel MOSFET

■ Absolute Maximum Ratings T_A = 25℃

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±12	±12	V
Continuous Drain Current (T_J = 150℃)* T_A = 25℃	I_D	±7.1	±6.2	A
T_A = 70℃		±5.7	±4.9	A
Pulsed Drain Current	I_{DM}	±40	±40	A
Continuous Source Current (Diode Conduction)*	I_S	1.7	-1.7	A
Maximum Power Dissipation* T_A = 25℃	P_D	2		W
T_A = 70℃		1.3		W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		℃
Maximum Junction-to-Ambient *	R_{thJA}	62.5		℃/W

*Surface Mounted on FR4 Board, t≤10 sec.

■ Electrical Characteristics T_J = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-Ch	0.6			V
		V_{DS} = V_{GS}, I_D = -250 μA	P-Ch	-0.6			
Gate Body Leakage	I_{GSS}	V_{DS} = 0 V V_{GS} = ±12 V	N-Ch			±100	nA
		V_{DS} = 0 V V_{GS} = ±12 V	P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0 V	N-Ch			1	
		V_{DS} = -20V, V_{GS} = 0 V	P-Ch			-1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55℃	N-Ch			5	μA
		V_{DS} = -20V, V_{GS} = 0 V, T_J = 55℃	P-Ch			-5	
On State Drain Currenta	$I_{D(on)}$	V_{DS} ≥5 V, V_{GS} = 4.5 V	N-Ch	20			A
		V_{DS} ≤-5 V, V_{GS} = -4.5 V	P-Ch	-20			
Drain Source On State Resistance*	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.1A	N-Ch		0.019	0.025	Ω
		V_{GS} = -4.5 V, I_D = -6.2A	P-Ch		0.027	0.033	
		V_{GS} = 2.5 V, I_D = 6.0A	N-Ch		0.025	0.035	
		V_{GS} = -2.5 V, I_D = -5.0A	P-Ch		0.040	0.050	
Forward Transconductance*	g_{fs}	V_{DS} = 10 V, I_D = 7.1A	N-Ch		27		S
		V_{DS} = -10 V, I_D = -6.2A	P-Ch		20		
Diode Forward Voltage*	V_{SD}	I_S = 1.7A, V_{GS} = 0 V	N-Ch			1.2	V
		I_S = -1.7A, V_{GS} = 0 V	P-Ch			-1.2	
Total Gate Charge	Q_g	N-Channel	N-Ch		25	50	nC
		V_{DS} = 10 V, V_{GS} = 4.5V, I_D = 7.1A	P-Ch		22	35	
Gate Source Charge	Q_{gs}		N-Ch		6.5		
		P-Channel	P-Ch		7		
Gate Drain Charge	Q_{gd}	V_{DS} = -10 V, V_{GS} = -4.52 V, I_D = -6.2A	N-Ch		4		
			P-Ch		3.5		
Turn On Time	$t_{d(on)}$	N Channel	N-Ch		40	60	ns
		V_{DD} = 10 V, R_L = 10Ω	P-Ch		27	50	
Rise Time	t_r	I_D= 1A, V_{GEN} = 4.5V, R_g = 6 Ω	N-Ch		40	60	
			P-Ch		32	50	
Turn Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		90	150	
		V_{DD} = -10 V, R_L = 10Ω	P-Ch		95	150	
Fall Time	t_f	I_D= -1 A, V_{GEN} = -4.5 V, R_g = 6 Ω	N-Ch		40	60	
			P-Ch		45	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/μs	N-Ch		40	80	
		I_F = -1.7 A, di/dt = 100 A/μs	P-Ch		40	80	

* Pulse test; pulse width ≤300μs, duty cycle≤2%.