Data Sheet | June 28, 2007 | FN6153.2

# 5MHz, Single and Dual Precision Rail-to-Rail Input-Output (RRIO) Op Amps

The ISL28136 and ISL28236 are low-power single and dual operational amplifiers optimized for single supply operation from 2.4V to 5.5V, allowing operation from one lithium cell or two Ni-Cd batteries. These devices feature a gain-bandwidth product of 5MHz and are unity-gain stable with a -3dB bandwidth of 13MHz.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The parts typically draw less than 1mA supply current per amplifier while meeting excellent DC accuracy, AC performance, noise and output drive specifications. Operation is guaranteed over -40°C to +125°C temperature range.

## Ordering Information

| PART NUMBER (Note) | PART MARKING | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|
| ISL28136FHZ-T7* | GABP | 6 Ld SOT-23 Tape and Reel | MDP0038 |
| ISL28136FHZ-T7A* | GABP | 6 Ld SOT-23 Tape and Reel | MDP0038 |
| ISL28136FBZ | 28136FBZ | 8 Ld SOIC | MDP0027 |
| ISL28136FBZ-T7* | 28136FBZ | 8 Ld SOIC Tape and Reel | MDP0027 |
| *Coming Soon* ISL28236FBZ-T7* | | 8 Ld SOIC Tape and Reel | MDP0027 |
| *Coming Soon* ISL28236FAZ-T7A* | | 8 Ld MSOP Tape and Reel | MDP0043 |

* “-T7” and “-T7A” suffix is for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

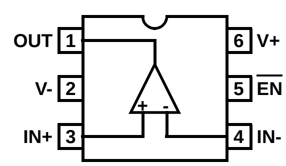
- 5MHz Gain bandwidth product @ $A_V = 100$
- 13MHz -3db unity gain bandwidth
- 900µA typical supply current (per amplifier)
- 150µV maximum offset voltage (8 Ld SO)
- 16nA typical input bias current
- Down to 2.4V single supply voltage range
- Rail-to-rail input and output
- Enable pin (ISL28136 only)
- -40°C to +125°C operation
- Pb-free plus anneal available (RoHS compliant)

## Applications

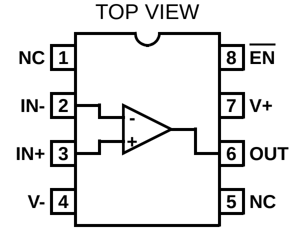
- Low-end audio
- 4mA to 20mA current loops
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

## Pinouts

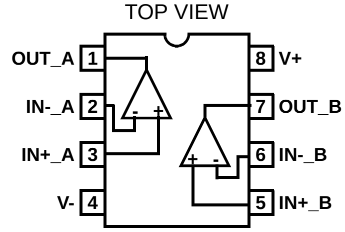
**ISL28136**
**(6 LD SOT-23)**
TOP VIEW



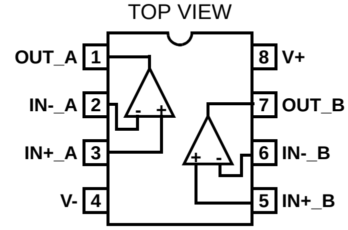

**ISL28136**
**(8 LD SOIC)**
TOP VIEW




**ISL28236**
**(8 LD SOIC)**
TOP VIEW




**ISL28236**
**(8 LD MSOP)**
TOP VIEW



## Absolute Maximum Ratings ($T_A$ = +25°C)

Supply Voltage . . . . . . . . . . 5.75V
Supply Turn On Voltage Slew Rate . . . . . . . . . . 1V/µs
Differential Input Current . . . . . . . . . . 5mA
Differential Input Voltage . . . . . . . . . . 0.5V
Input Voltage . . . . . . . . . . V- - 0.5V to V+ + 0.5V
ESD Rating
Human Body Model . . . . . . . . . . 3kV
Machine Model . . . . . . . . . . 300V

## Thermal Information

Thermal Resistance — $\theta_{JA}$ (°C/W)
6 Ld SOT-23 Package . . . . . . . . . . 230
8 Ld SO Package . . . . . . . . . . 110
8 Ld MSOP Package . . . . . . . . . . 115
Ambient Operating Temperature Range . . . . . . . . . -40°C to +125°C
Storage Temperature Range . . . . . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . . . . . +125°C
Pb-free reflow profile . . . . . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

$V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 1) | TYP | MAX (Note 1) | UNIT |
|---|---|---|---|---|---|---|
| **DC SPECIFICATIONS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | 8 Ld SO | -150<br>**-270** | ±10 | 150<br>**270** | µV |
| | | 6 Ld SOT-23 | -400<br>**-450** | ±10 | 400<br>**450** | µV |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Input Offset Voltage vs Temperature | | | 0.4 | | µV/°C |
| $I_{OS}$ | Input Offset Current | <br>$T_A$ = -40°C to +85°C | -10<br>-15 | 0 | 10<br>15 | nA |
| $I_B$ | Input Bias Current | <br>$T_A$ = -40°C to +85°C | -10<br>-15 | 16 | 35<br>40 | nA |
| $V_{CM}$ | Common-Mode Voltage Range | Guaranteed by CMRR | 0 | | 5 | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 5V | 90<br>**85** | 114 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_+$ = 2.4V to 5.5V | 90<br>**85** | 99 | | dB |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O$ = 0.5V to 4V, $R_L$ = 100kΩ to $V_{CM}$ | 600<br>**500** | 1770 | | V/mV |
| | | $V_O$ = 0.5V to 4V, $R_L$ = 1kΩ to $V_{CM}$ | | 140 | | V/mV |
| $V_{OUT}$ | Maximum Output Voltage Swing | Output low, $R_L$ = 100kΩ to $V_{CM}$ | | 3 | 6<br>**10** | mV |
| | | Output low, $R_L$ = 1kΩ to $V_{CM}$ | | 70 | 90<br>**110** | mV |
| | | Output high, $R_L$ = 100kΩ to $V_{CM}$ | 4.99<br>**4.98** | 4.994 | | V |
| | | Output high, $R_L$ = 1kΩ to $V_{CM}$ | 4.92<br>**4.89** | 4.94 | | V |
| $I_{S,ON}$ | Supply Current, Enabled | Per Amp | 0.8 | 0.9 | 1.1<br>**1.4** | mA |
| $I_{S,OFF}$ | Supply Current, Disabled (ISL28136) | | | 10 | 14<br>**16** | µA |
| $I_O+$ | Short-Circuit Output Source Current | $R_L$ = 10Ω to $V_{CM}$ | 48<br>**45** | 56 | | mA |

## Electrical Specifications

$V_+$ = 5V, $V_-$ = 0V, $V_{CM}$ = 2.5V, $R_L$ = Open, $T_A$ = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 1) | TYP | MAX (Note 1) | UNIT |
|---|---|---|---|---|---|---|
| $I_{O}$- | Short-Circuit Output Sink Current | $R_L$ = 10Ω to $V_{CM}$ | 50<br>**45** | 55 | | mA |
| $V_{SUPPLY}$ | Supply Operating Range | V+ to V- | 2.4 | | 5.5 | V |
| $V_{\overline{EN}H}$ | $\overline{EN}$ Pin High Level (ISL28136) | | **2** | | | V |
| $V_{\overline{EN}L}$ | $\overline{EN}$ Pin Low Level (ISL28136) | | | | **0.8** | V |
| $I_{\overline{EN}H}$ | $\overline{EN}$ Pin Input High Current (ISL28136) | $V_{\overline{EN}}$ = V+ | | 1 | 1.5<br>**1.6** | µA |
| $I_{\overline{EN}L}$ | $\overline{EN}$ Pin Input Low Current (ISL28136) | $V_{\overline{EN}}$ = V- | | 16 | 25<br>**30** | nA |
| **AC SPECIFICATIONS** | | | | | | |
| GBW | Gain Bandwidth Product | $A_V$ = 100, $R_F$ = 100kΩ, $R_G$ = 1kΩ to $V_{CM}$ | | 5 | | MHz |
| Unity Gain Bandwidth | -3dB Bandwidth | $A_V$ = 1, $R_F$ = 0Ω, $R_L$ = 10kΩ to $V_{CM}$, $V_{OUT}$ = 10m$V_{P-P}$ | | 13 | | MHz |
| $e_N$ | Input Noise Voltage Peak-to-Peak | f = 0.1Hz to 10Hz, $R_L$ = 10kΩ to $V_{CM}$ | | 0.4 | | µ$V_{P-P}$ |
| | Input Noise Voltage Density | $f_O$ = 1kHz, $R_L$ = 10kΩ to $V_{CM}$ | | 15 | | nV/√Hz |
| $i_N$ | Input Noise Current Density | $f_O$ = 10kHz, $R_L$ = 10kΩ to $V_{CM}$ | | 0.35 | | pA/√Hz |
| CMRR | Input Common Mode Rejection Ratio | $f_O$ = to 120Hz; $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 1kΩ to $V_{CM}$ | | -90 | | dB |
| PSRR+ to 120Hz | Power Supply Rejection Ratio ($V_+$) | $V_+$, $V_-$ = ±1.2V and ±2.5V, $V_{SOURCE}$ = 1$V_{P-P}$, $R_L$ = 1kΩ to $V_{CM}$ | | -88 | | dB |
| PSRR- to 120Hz | Power Supply Rejection Ratio ($V_-$) | $V_+$, $V_-$ = ±1.2V and ±2.5V $V_{SOURCE}$ = 1$V_{P-P}$, $R_L$ = 1kΩ to $V_{CM}$ | | -105 | | dB |
| **TRANSIENT RESPONSE** | | | | | | |
| SR | Slew Rate | $V_{OUT}$ = ±1.5V; $R_f$ = 50kΩ, $R_G$ = 50kΩ to $V_{CM}$ | | ±1.9 | | V/µs |
| $t_r$, $t_f$, Large Signal | Rise Time, 10% to 90%, $V_{OUT}$ | $A_V$ = +2, $V_{OUT}$ = 2$V_{P-P}$, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 0.6 | | µs |
| | Fall Time, 90% to 10%, $V_{OUT}$ | $A_V$ = +2, $V_{OUT}$ = 2$V_{P-P}$, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 0.5 | | µs |
| $t_r$, $t_f$, Small Signal | Rise Time, 10% to 90%, $V_{OUT}$ | $A_V$ = +2, $V_{OUT}$ = 10m$V_{P-P}$, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 65 | | ns |
| | Fall Time, 90% to 10%, $V_{OUT}$ | $A_V$ = +2, $V_{OUT}$ = 10m$V_{P-P}$, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 62 | | ns |
| $t_{\overline{EN}}$ | Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% $V_{OUT}$ (ISL28136) | $V_{\overline{EN}}$ = 5V to 0V, $A_V$ = +2, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 5 | | µs |
| | Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% $V_{OUT}$ (ISL28136) | $V_{\overline{EN}}$ = 0V to 5V, $A_V$ = +2, $R_g$ = $R_f$ = $R_L$ = 1kΩ to $V_{CM}$ | | 0.3 | | µs |

NOTE:

1. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open

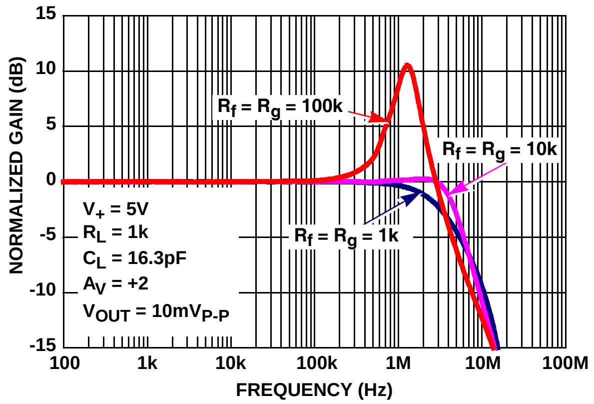



FIGURE 1. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES $R_f/R_g$

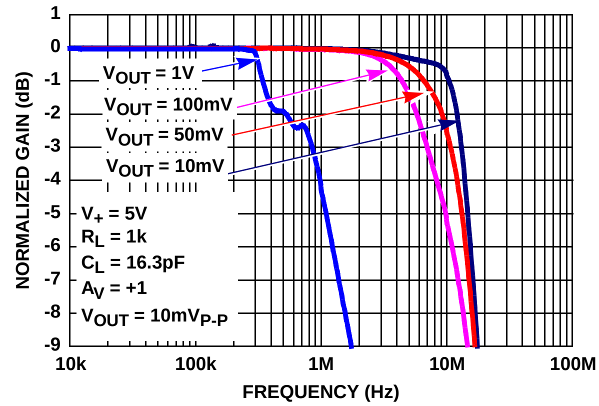



FIGURE 2. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 1k

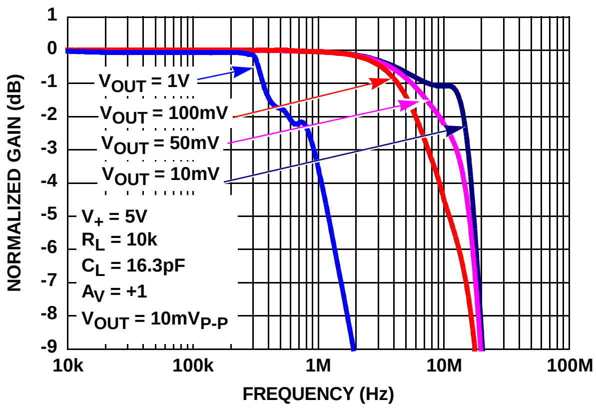



FIGURE 3. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 10k

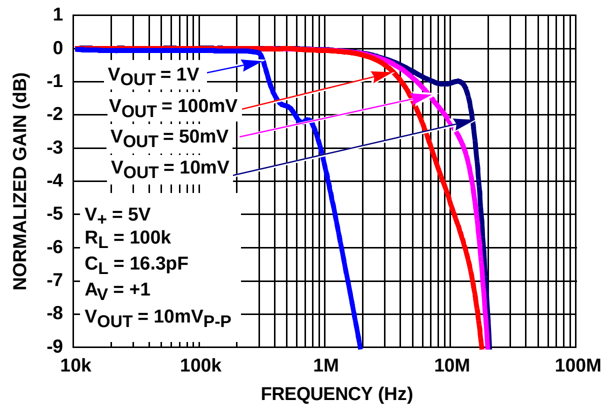



FIGURE 4. GAIN vs FREQUENCY vs $V_{OUT}$, $R_L$ = 100k

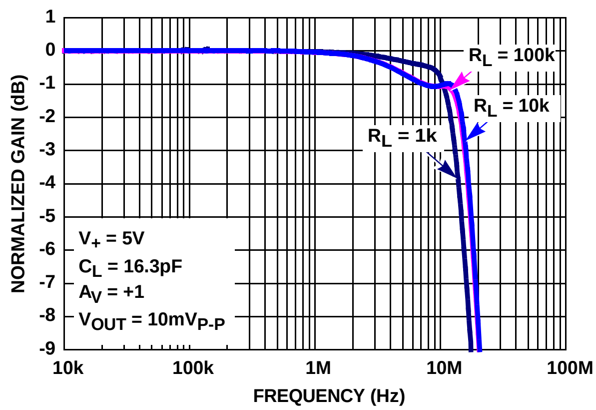



FIGURE 5. GAIN vs FREQUENCY vs $R_L$

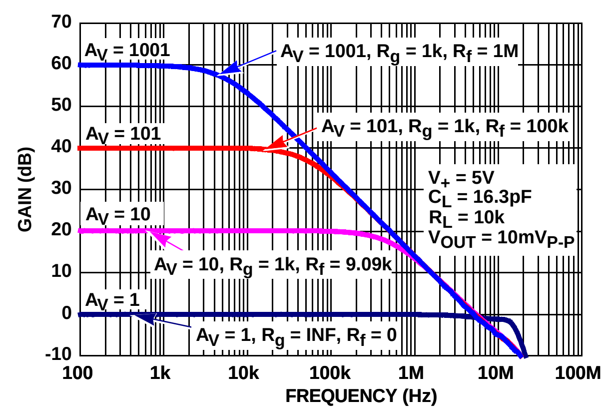



FIGURE 6. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open **(Continued)**

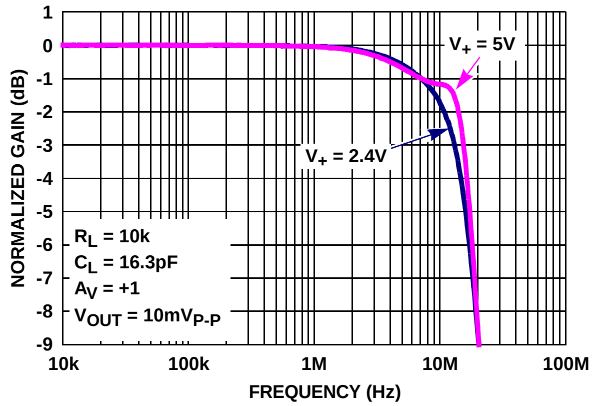



**FIGURE 7. GAIN vs FREQUENCY vs SUPPLY VOLTAGE**

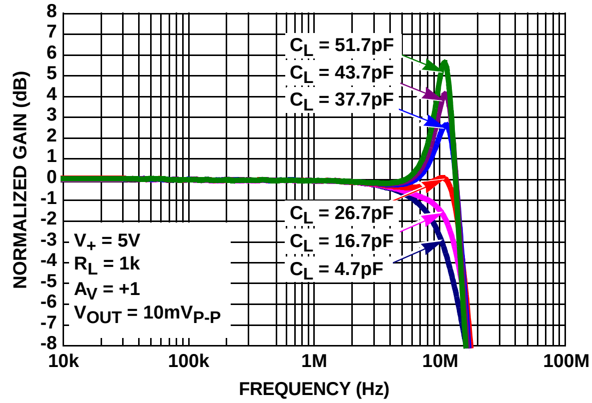



**FIGURE 8. GAIN vs FREQUENCY vs $C_L$**

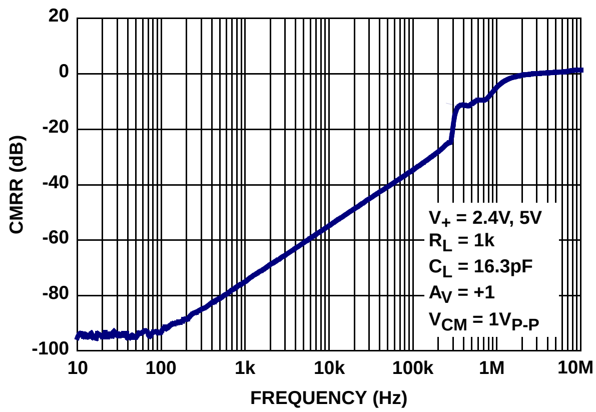



**FIGURE 9. CMRR vs FREQUENCY; $V_+ = 2.4V$ AND 5V**

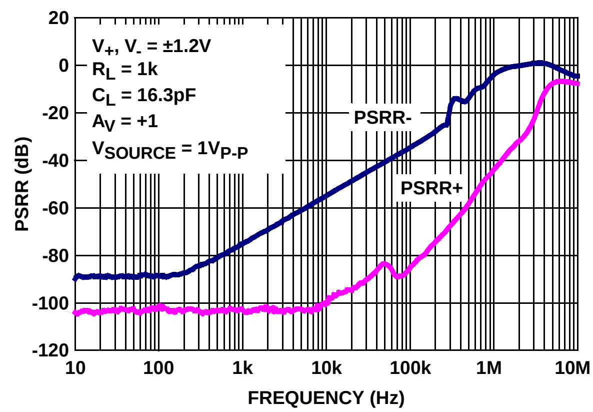



**FIGURE 10. PSRR vs FREQUENCY, $V_+$, $V_- = \pm1.2V$**

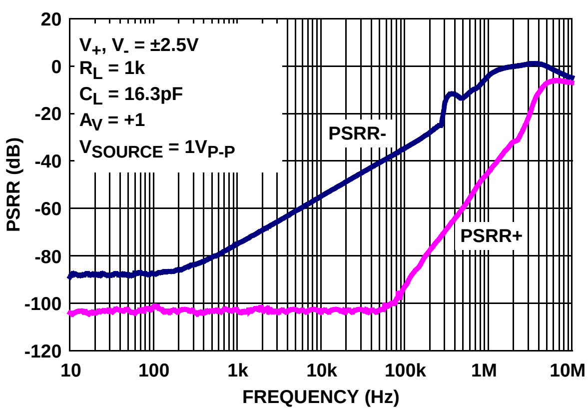



**FIGURE 11. PSRR vs FREQUENCY, $V_+$, $V_- = \pm2.5V$**

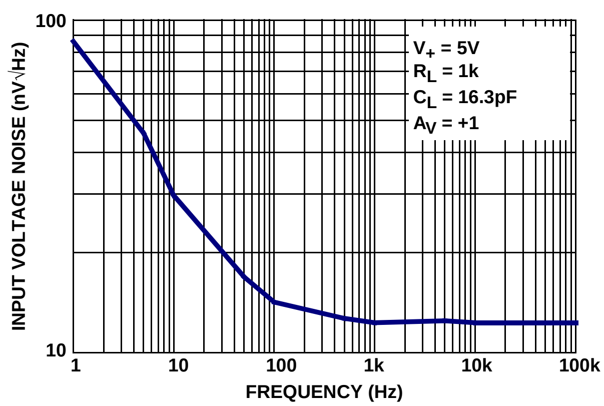



**FIGURE 12. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY**

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open **(Continued)**

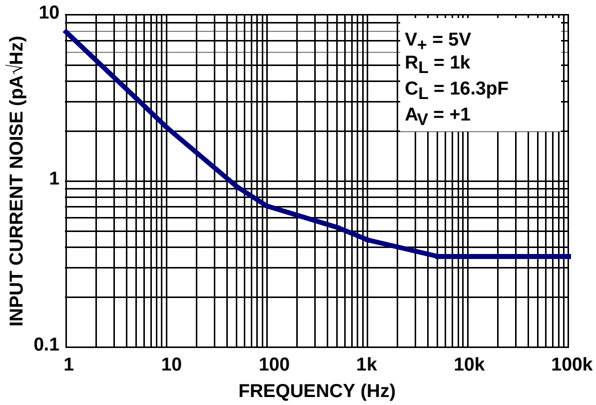



**FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY**

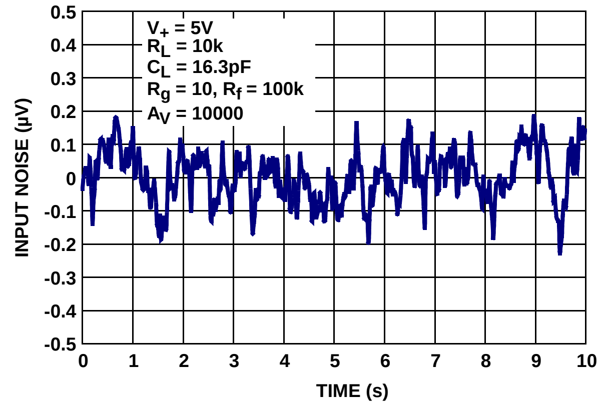



**FIGURE 14. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz**

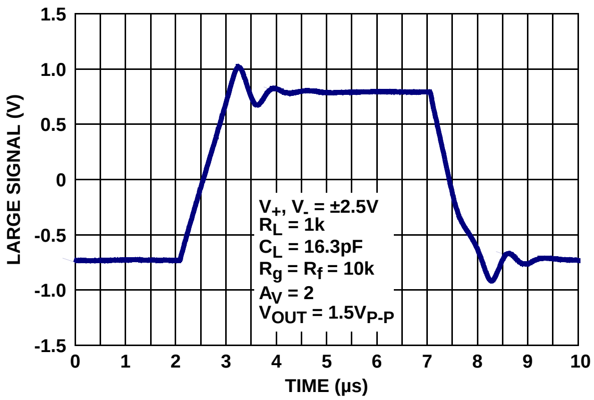



**FIGURE 15. LARGE SIGNAL STEP RESPONSE**

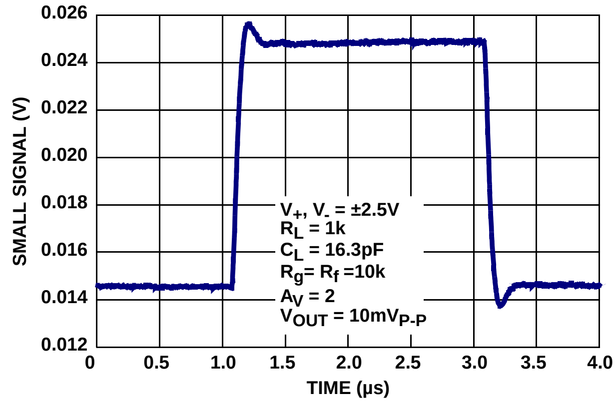



**FIGURE 16. SMALL SIGNAL STEP RESPONSE**

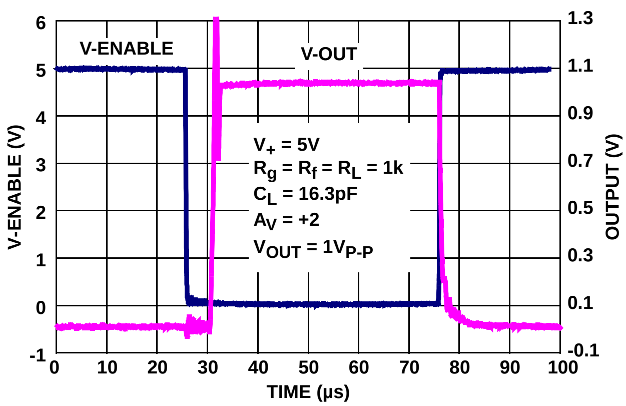



**FIGURE 17. ENABLE TO OUTPUT RESPONSE**

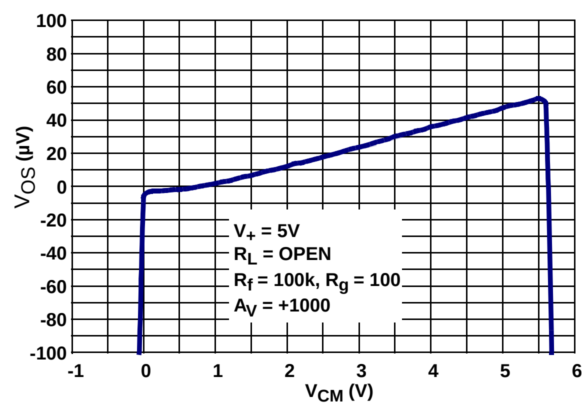



**FIGURE 18. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open **(Continued)**

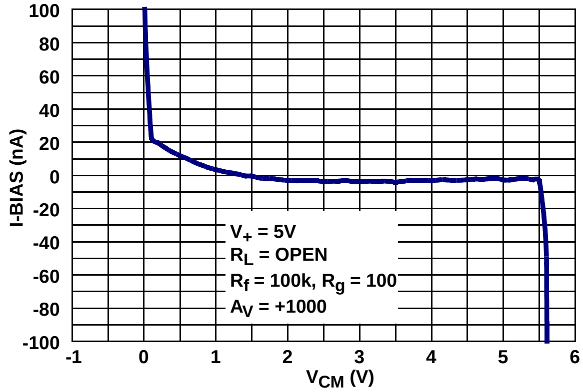



**FIGURE 19. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE**

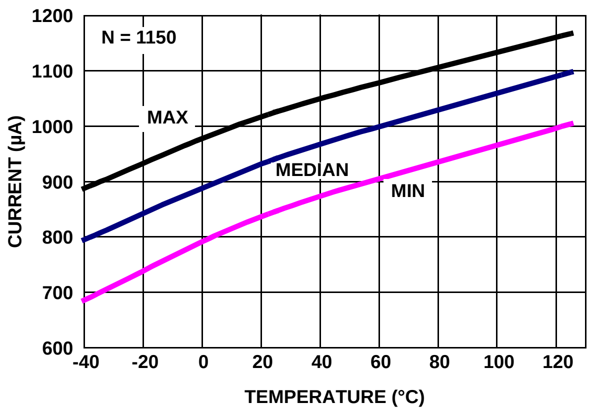



**FIGURE 20. SUPPLY CURRENT ENABLED vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V**

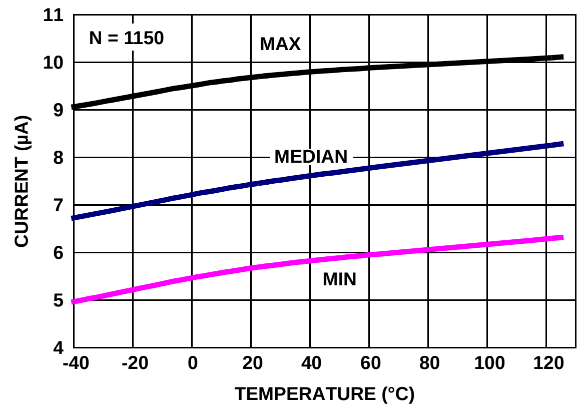



**FIGURE 21. SUPPLY CURRENT DISABLED vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V**

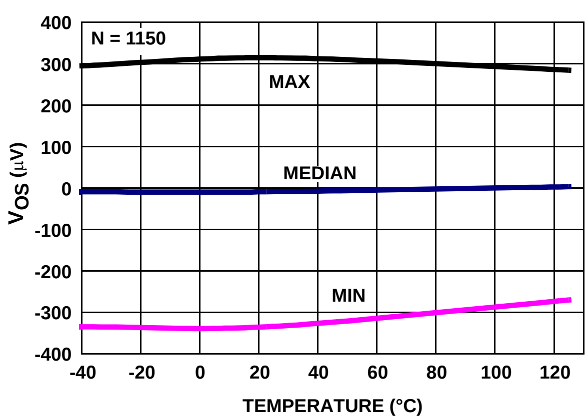



**FIGURE 22. $V_{OS}$ vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, SOT PACKAGE**

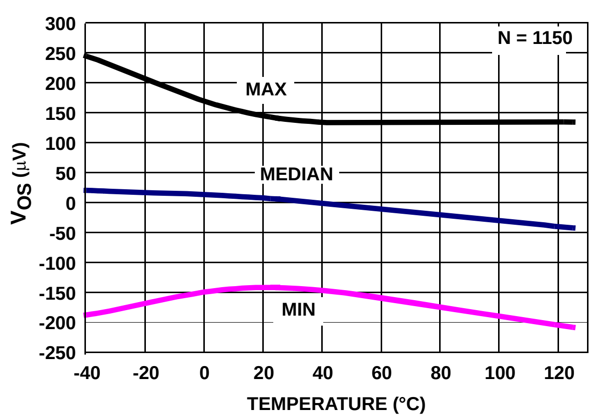



**FIGURE 23. $V_{OS}$ vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V, SOIC PACKAGE**

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open **(Continued)**

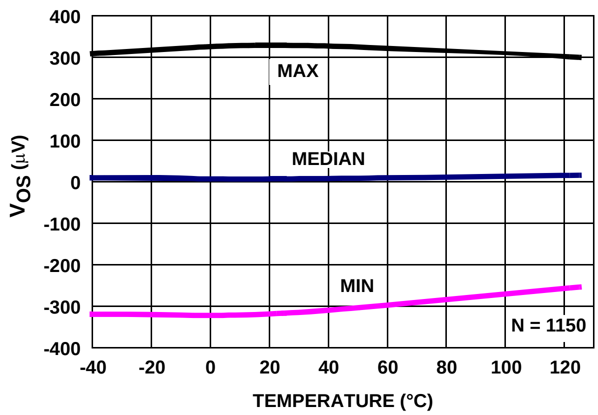



**FIGURE 24. $V_{OS}$ vs TEMPERATURE, $V_+$, $V_-$ = ±1.2V, SOT PACKAGE**

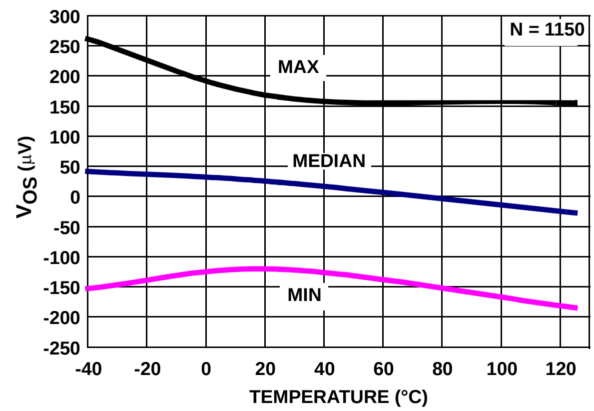



**FIGURE 25. $V_{OS}$ vs TEMPERATURE, $V_+$, $V_-$ = ±1.2V, SOIC PACKAGE**

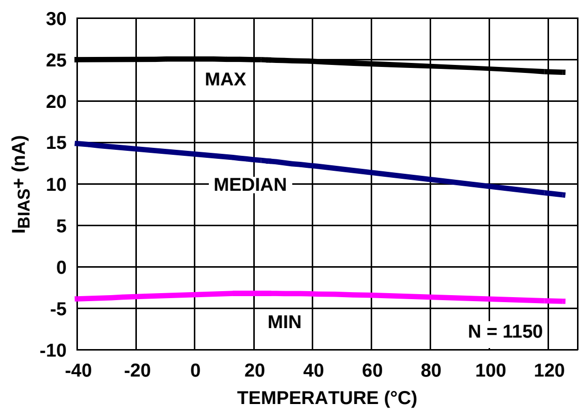



**FIGURE 26. $I_{BIAS}$+ vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V**

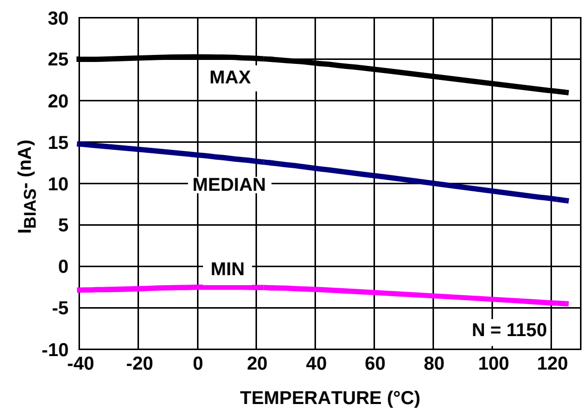



**FIGURE 27. $I_{BIAS}$- vs TEMPERATURE, $V_+$, $V_-$ = ±2.5V**

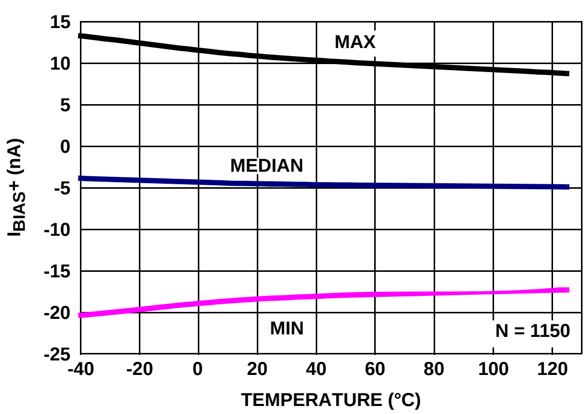



**FIGURE 28. $I_{BIAS}$+ vs TEMPERATURE, $V_+$, $V_-$ = ±1.2V**

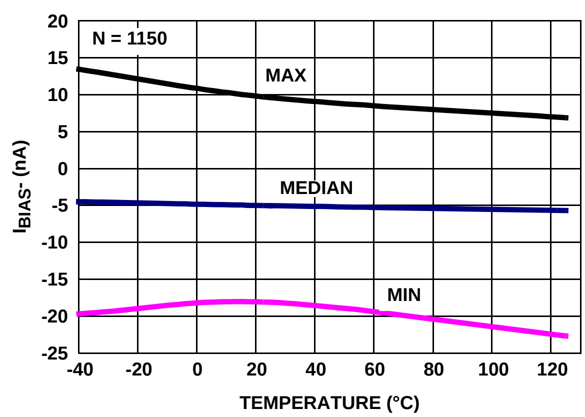



**FIGURE 29. $I_{BIAS}$- vs TEMPERATURE, $V_+$, $V_-$ = ±1.2V**

## *Typical Performance Curves* $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $R_L$ = Open **(Continued)**

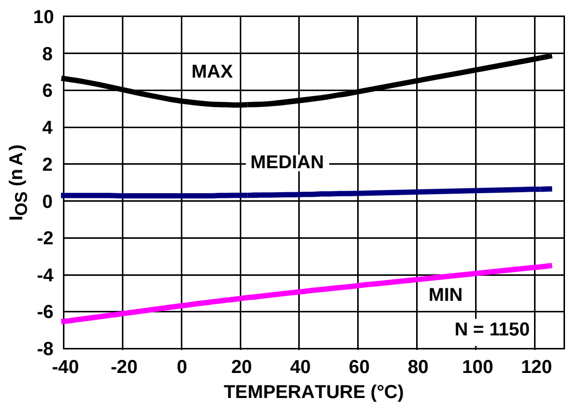



**FIGURE 30. $I_{OS}$ vs TEMPERATURE, $V_{+,}$ $V_-$ = ±2.5V**

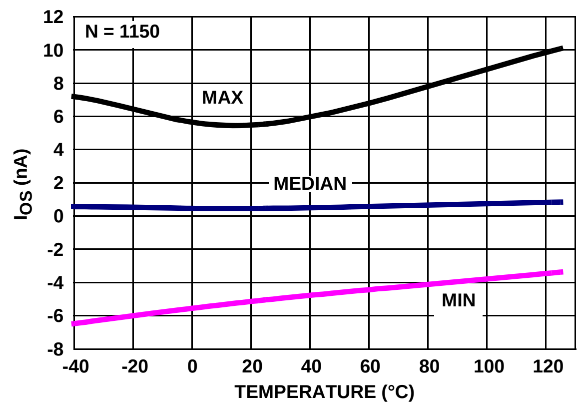



**FIGURE 31. $I_{OS}$ vs TEMPERATURE, $V_{+,}$ $V_-$ = ±1.2V**

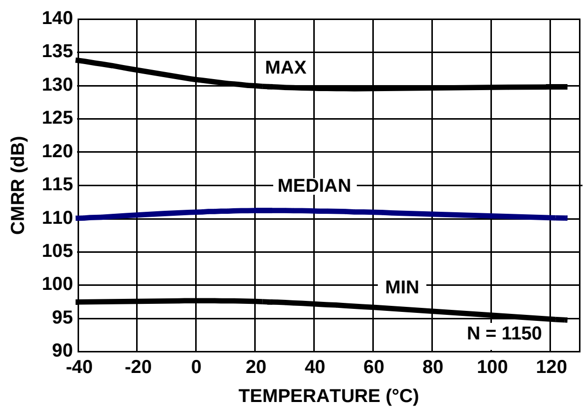



**FIGURE 32. CMRR vs TEMPERATURE, $V_{CM}$ = -2.5V TO +2.5V, $V_{+,}$ $V_-$ = ±2.5V**

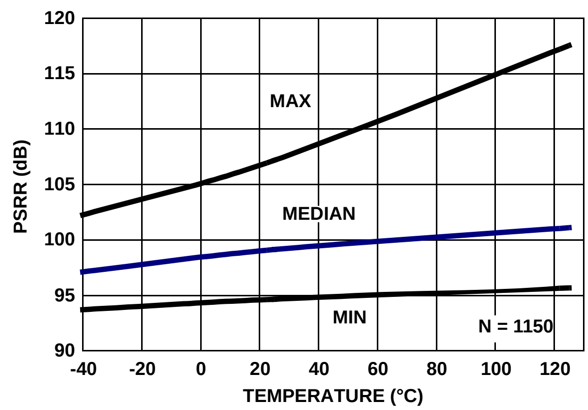



**FIGURE 33. PSRR vs TEMPERATURE, $V_{+,}$ $V_-$ = ±1.2V TO ±2.75V**

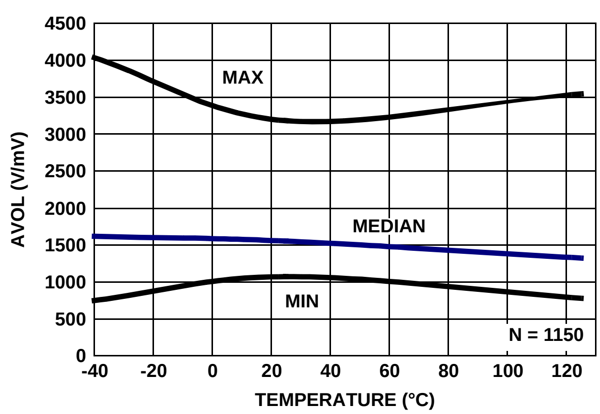



**FIGURE 34. AVOL vs TEMPERATURE, $V_{+,}$ $V_-$ = ±2.5V, $V_O$ = -2V TO +2V, $R_L$ = 100k**

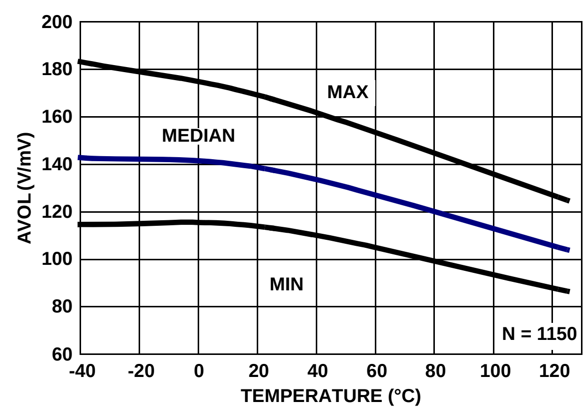



**FIGURE 35. AVOL vs TEMPERATURE, $V_{+,}$ $V_-$ = ±2.5V, $V_O$ = -2V TO +2V, $R_L$ = 1k**

## Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$ (Continued)

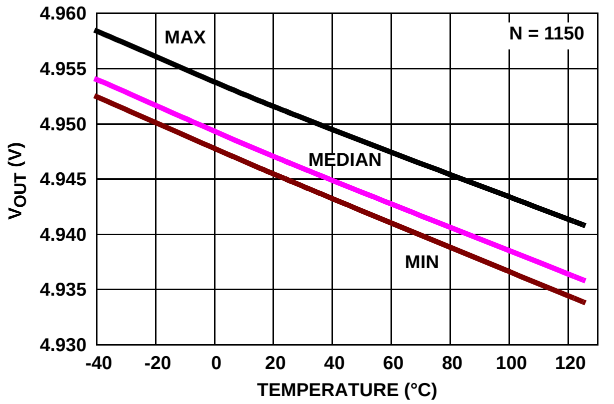



FIGURE 36. $V_{OUT}$ HIGH vs TEMPERATURE, $V_+, V_- = \pm2.5V$, $R_L = 1k$

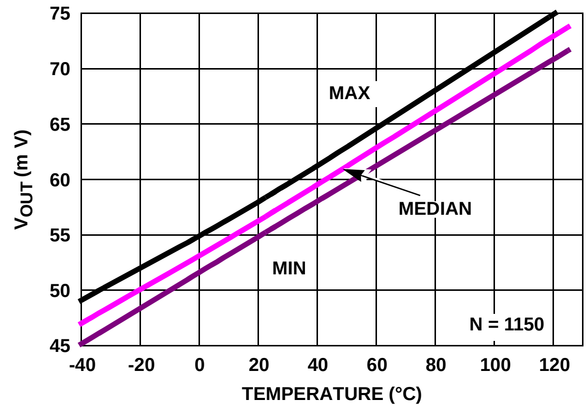
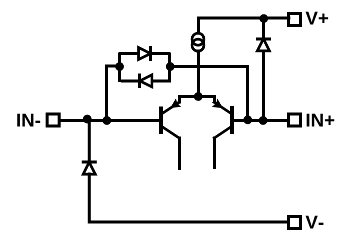
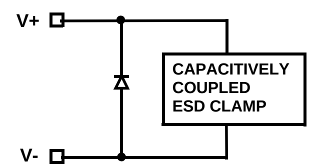
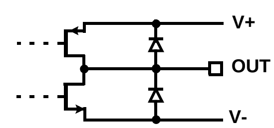
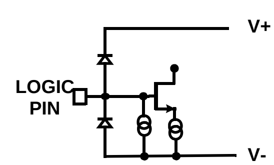



FIGURE 37. $V_{OUT}$ LOW vs TEMPERATURE, $V_+, V_- = \pm2.5V$, $R_L = 1k$

## Pin Descriptions

| ISL28136 (6 Ld SOT-23) | ISL28136 (8 Ld SOIC) | ISL28236 (8 Ld SOIC) (8 Ld MSOP) | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
|---|---|---|---|---|---|
| | 1, 5 | | NC | Not connected | |
| 4 | 2 | 2 (A)<br>6 (B) | IN-<br>IN-_A<br>IN-_B | inverting input | <br>Circuit 1 |
| 3 | 3 | 3 (A)<br>5 (B) | IN+<br>IN+_A<br>IN+_B | Non-inverting input | See Circuit 1 |
| 2 | 4 | 4 | V- | Negative supply | <br>Circuit 2 |
| 1 | 6 | 1 (A)<br>7 (B) | OUT<br>OUT_A<br>OUT_B | Output | <br>Circuit 3 |
| 6 | 7 | 8 | V+ | Positive supply | See Circuit 2 |
| 5 | 8 | | $\overline{EN}$ | Chip enable | <br>Circuit 3 |

## Applications Information

### Introduction

The ISL28136 and ISL28236 are single and dual channel Bi-CMOS rail-to-rail input, output (RRIO) micropower precision operational amplifiers. The parts are designed to operate from single supply (2.4V to 5.5V) or dual supply (±1.2V to ±2.75V). The parts have an input common mode range that extends 0.25V above the positive rail and down to the negative supply rail. The output operation can swing within about 3mV of the supply rails with a 100kΩ load.

### Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28136 and ISL28236 achieve input rail-to-rail operation without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives an undistorted behavior from typically down to the negative rail to 0.25V higher than the positive rail.

### Rail-to-Rail Output

A pair of complementary Bi-polar devices are used to achieve the rail-to-rail output swing. The PNP sinks current to swing the output in the negative direction. The NPN sources current to swing the output in the positive direction. The ISL28136 and ISL28236 with a 100kΩ load will swing to within 3mV of the positive supply rail and within 3mV of the negative supply rail.

### Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in two ways. 1) The input voltage times the gain of the amplifier exceeds the supply voltage by a large value or, 2) The output current required is higher than the output stage can deliver. These conditions can result in a shift in the Input Offset Voltage ($V_{OS}$) as much as 1µV/hr. of exposure under these conditions.

### IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals ("Pin Descriptions" on page 10 - Circuit 1). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (Figure 38).

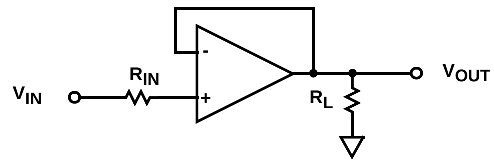



FIGURE 38. INPUT CURRENT LIMITING

### Enable/Disable Feature

The ISL28136 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA at room temperature. The $\overline{EN}$ pin has an internal pull down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default. The $\overline{EN}$ pin should never be left floating. When not used, the $\overline{EN}$ pin should either be left floating or connected to the V- pin.

By disabling the part, multiple ISL28136 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel $V_{OUT}$ = 1V, while disabled channel $V_{IN}$ = GND), so the mux implementation is best suited for small signal applications. If large signals are required, use series IN+ resistors, or a large value $R_F$, to keep the feed through current low enough to minimize the impact on the active channel. See the "Limitations of the Differential Input Protection" section for more details.

### Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non-inverting unity gain applications, the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback ($R_F$) and gain setting ($R_G$) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1) During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don't track, so differentials arise.

2) When the amplifier is disabled but an input signal is still present. An $R_L$ or $R_G$ to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel $V_{OUT}$ determines the voltage on the IN- terminal.

3) When the slew rate of the input pulse is considerably faster than the op amp's slew rate. If the $V_{OUT}$ can't keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 1.9V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled $I_{CC}$.

### Using Only One Channel

The ISL28236 is a dual op amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 39).

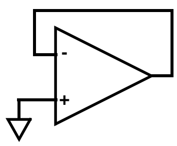



**FIGURE 39. PREVENTING OSCILLATIONS IN UNUSED CHANNELS**

### Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

### Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

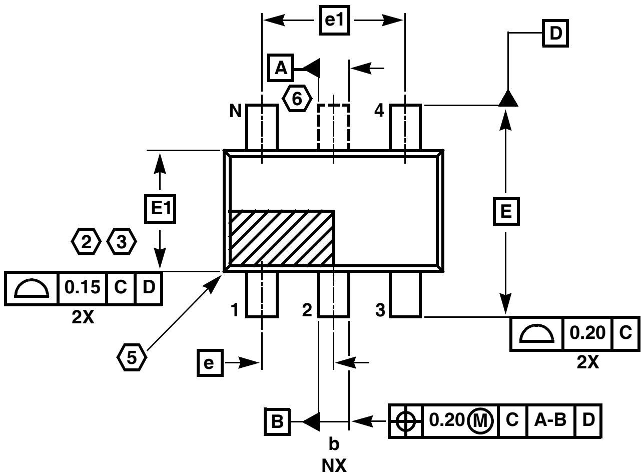
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)
- $PD_{MAX}$ for each amplifier can be calculated as follows:

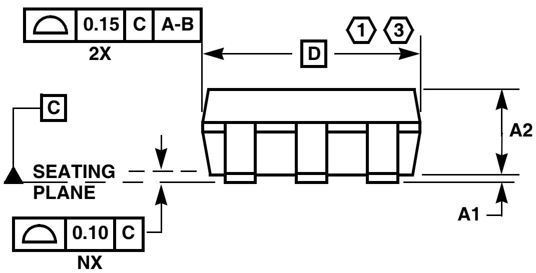
$$PD_{MAX} = 2{*}V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

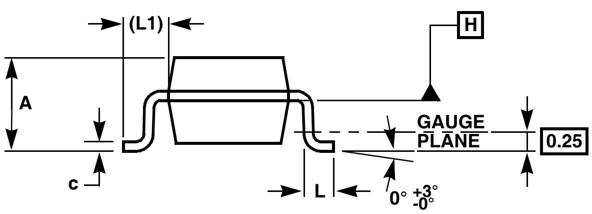
where:

- $T_{MAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier
- $V_S$ = Supply voltage (Magnitude of $V_+$ and $V_-$)
- $I_{MAX}$ = Maximum supply current of 1 amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application
- $R_L$ = Load resistance

## SOT-23 Package Family




### MDP0038

**SOT-23 PACKAGE FAMILY**

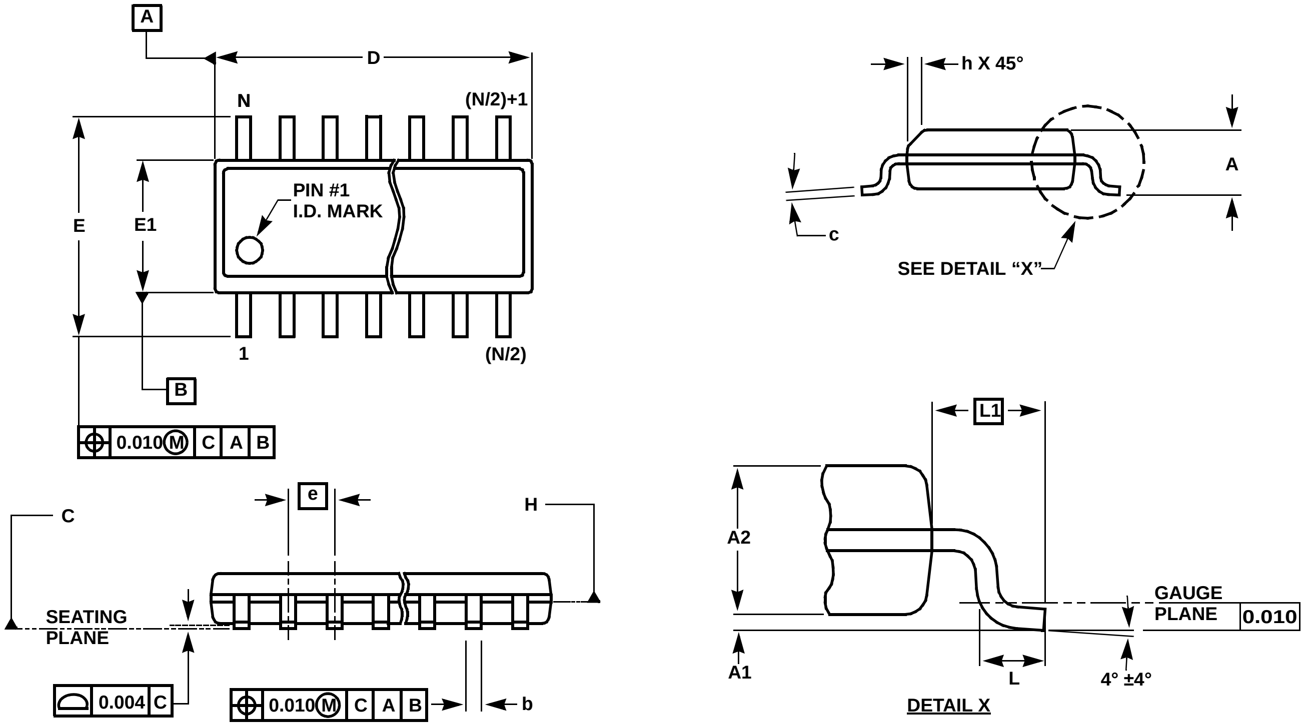
| SYMBOL | MILLIMETERS | | TOLERANCE |
|---|---|---|---|
| | SOT23-5 | SOT23-6 | |
| A | 1.45 | 1.45 | MAX |
| A1 | 0.10 | 0.10 | ±0.05 |
| A2 | 1.14 | 1.14 | ±0.15 |
| b | 0.40 | 0.40 | ±0.05 |
| c | 0.14 | 0.14 | ±0.06 |
| D | 2.90 | 2.90 | Basic |
| E | 2.80 | 2.80 | Basic |
| E1 | 1.60 | 1.60 | Basic |
| e | 0.95 | 0.95 | Basic |
| e1 | 1.90 | 1.90 | Basic |
| L | 0.45 | 0.45 | ±0.10 |
| L1 | 0.60 | 0.60 | Reference |
| N | 5 | 6 | Reference |

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

## *Small Outline Package Family (SO)*




## MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

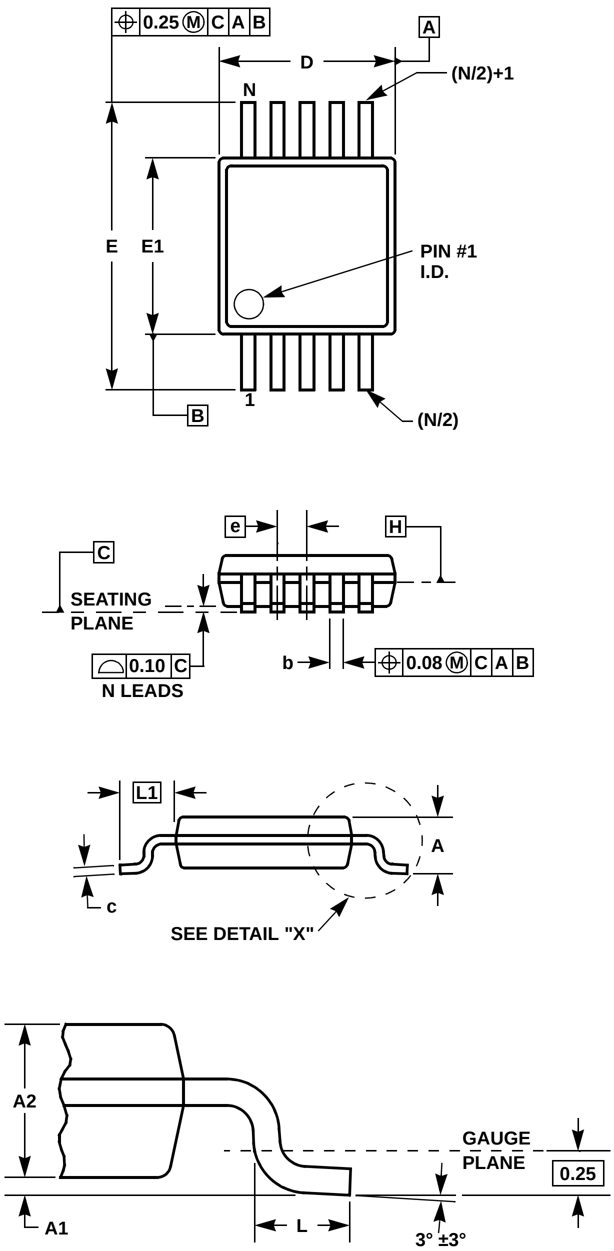
| SYMBOL | INCHES | | | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | | |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## *Mini SO Package Family (MSOP)*




## MDP0043

**MINI SO PACKAGE FAMILY**

| SYMBOL | MILLIMETERS | | TOLERANCE | NOTES |
|---|---|---|---|---|
| | MSOP8 | MSOP10 | | |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | ±0.05 | - |
| A2 | 0.86 | 0.86 | ±0.09 | - |
| b | 0.33 | 0.23 | +0.07/-0.08 | - |
| c | 0.18 | 0.18 | ±0.05 | - |
| D | 3.00 | 3.00 | ±0.10 | 1, 3 |
| E | 4.90 | 4.90 | ±0.15 | - |
| E1 | 3.00 | 3.00 | ±0.10 | 2, 3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | ±0.15 | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.