HD66702 (LCD-II/E20)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD66702 LCD-II/E20 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single LCD-II/E20 can display up to two 20-character lines. However, with the addition of HD44100 drivers, a maximum of up to two 40-character lines can be displayed.

The low 3-V power supply of the LCD-II/E20 under development is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 7 and 5 × 10 dot matrix possible
- 80 × 8-bit display RAM (80 characters max.)
- 7,200-bit character generator ROM
  - 160 character fonts (5 × 7 dot)
  - 32 character fonts (5 × 10 dot)
- 64 × 8-bit character generator RAM
  - 8 character fonts (5 × 7 dot)
  - 4 character fonts (5 × 10 dot)
- 16-common × 100-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 × 7 dots with cursor
  - 1/11 for one line of 5 × 10 dots with cursor
  - 1/16 for two lines of 5 × 7 dots with cursor
- Maximum display characters
  - One line

    1/8 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100R), 80-char. × 1-line (max. extension with eight HD44100s). 1/11 duty cycle, 20-char. × 1-line (no extension), 28-char. × 1-line (extended with one HD44100R), 80-char. × 1-line (max. extension with eight HD44100Rs)
  - Two lines

    1/16 duty cycle, 20-char. × 2-line (no extension), 28-char. × 2-line (extended with one HD44100R), 40-char. × 2-line (max. extension with eight HD44100Rs)
- Wide range of instruction functions
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Choice of power supply (V_{CC}): 4.5 to 5.5 V (standard), 2.7 to 5.5 V (low voltage)
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)
- Independent LCD drive voltage driven off of the logic power supply (V_{CC}): 3.0 to 8.3 V

Hitachi semiconductor

Ordering Information

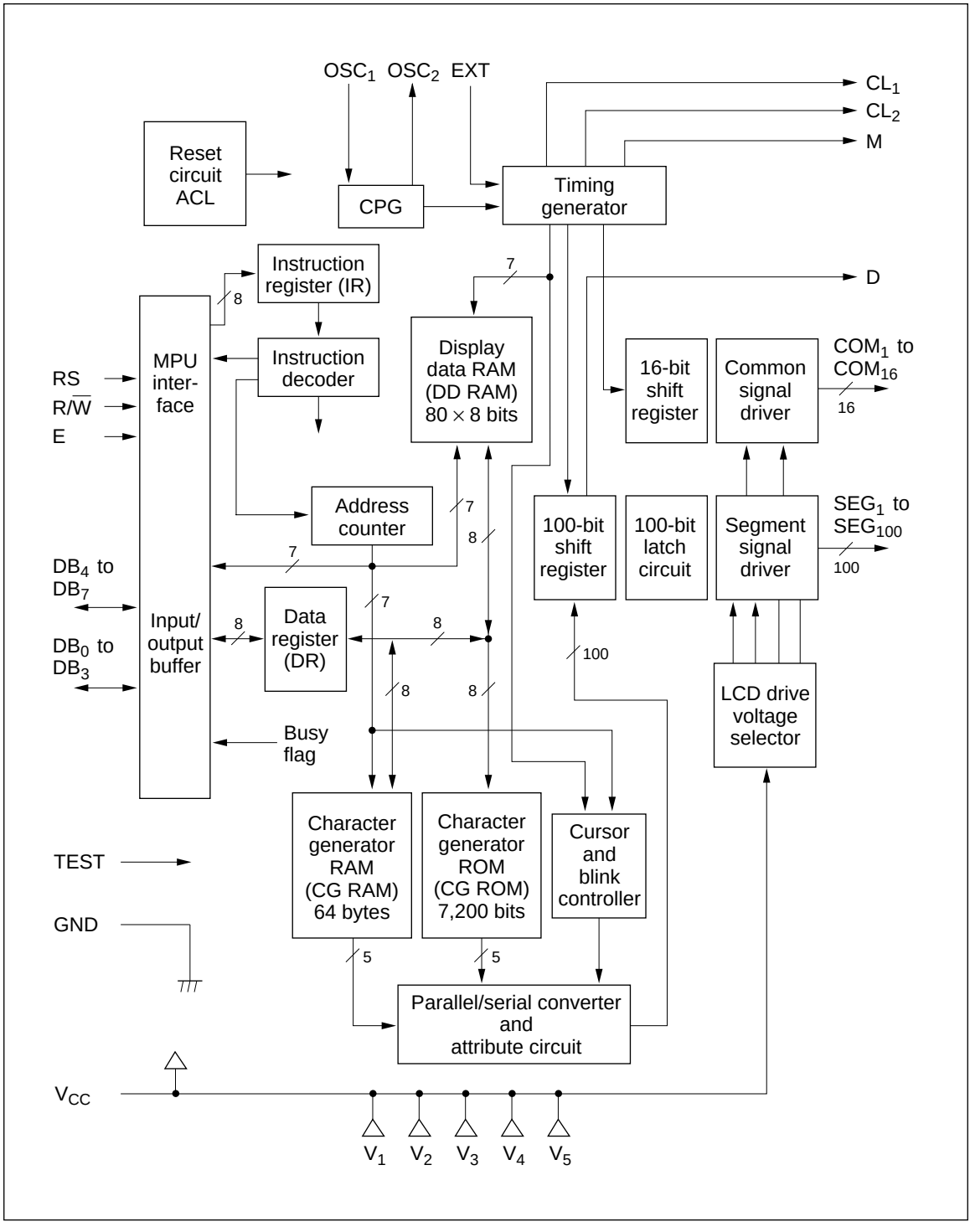
Type No.	Package	Operating Voltage	ROM Font
HCD66702RA00L	Chip	2.7 to 5.5 V	Standard Japanese font
HD66702RA00F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RA00FL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	
HD66702RA01F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	Japanese font for comunication system
HD66702RA02F	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	European font
HCD66702RBxxL	Chip	2.7 to 5.5 V	Custom font
HD66702RBxxF	144-pin plastic QFP (FP-144A)	4.5 to 5.5 V	
HD66702RBxxFL	144-pin plastic QFP (FP-144A)	2.7 to 5.5 V	

Note: xx: ROM code No.

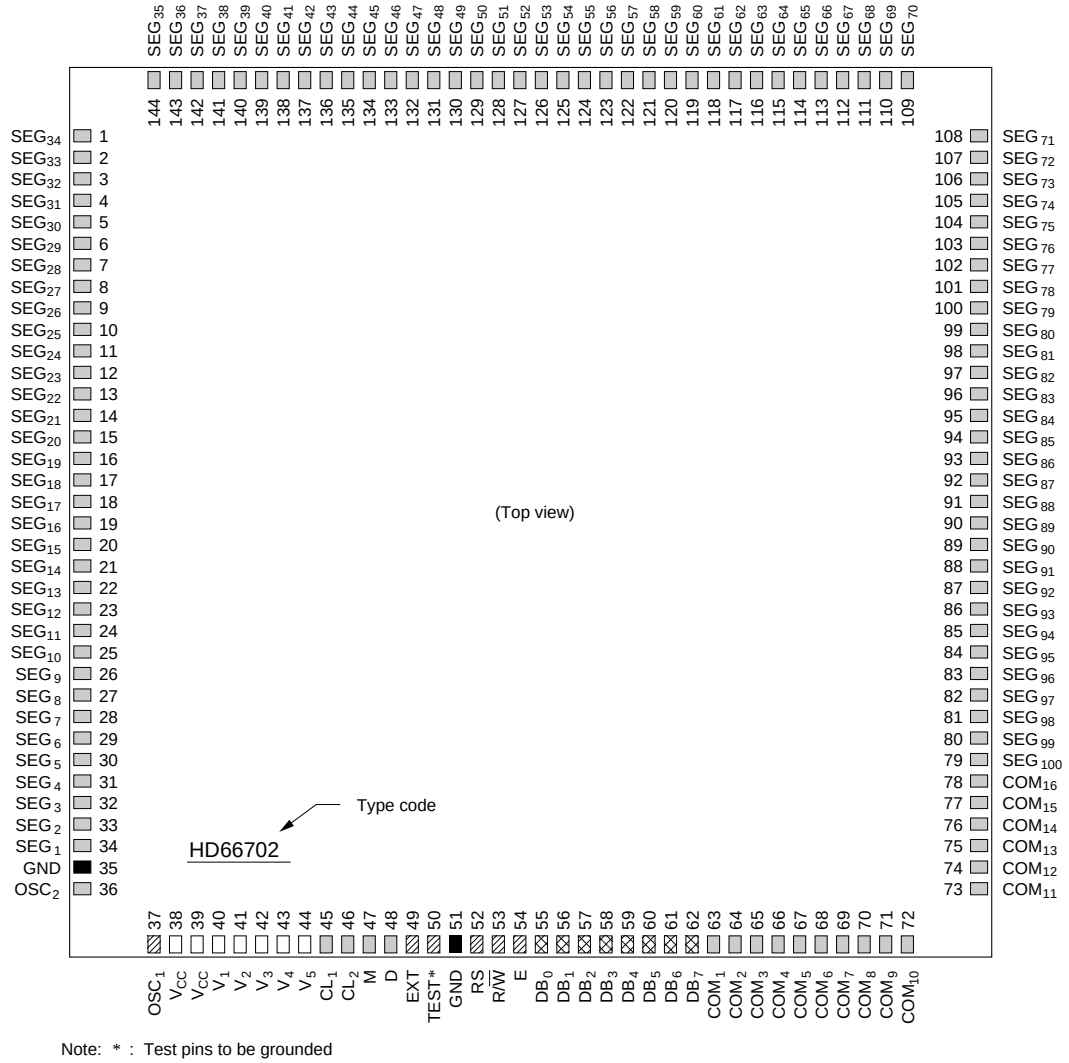
LCD-II Family Comparison

Item		LCD-II (HD44780U)	LCD-II/E20 (HD66702)
Power supply voltage		2.7 to 5.5 V	5 V ±10% (standard) 2.7 to 5.5 V (low voltage)
Liquid crystal drive voltage V_{LCD}	1/4 bias	3.0 to 11 V	3.0 to 8.3 V
	1/5 bias	3.0 to 11 V	3.0 to 8.3 V
Maximum display digits per chip		16 digits (8 digits × 2 lines)	40 digits (20 digits × 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		9,600 bits (208 character fonts for 5 × 8 dot and 32 character fonts for 5 × 10 dot)	7,200 bits (160 character fonts for 5 × 7 dot and 32 character fonts for 5 × 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	100
Common signals		16	16
Liquid crystal drive waveform		A	B
Ladder resistor for LCD power supply		External	External
Clock source		External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)		270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (69 to 128 Hz for 1/8 and 1/16 duty cycles; 50 to 93 Hz for 1/11 duty cycle)
R_f resistance		91 kΩ ±2% (5 V) 75 kΩ ±2% (3 V)	68 kΩ ±2% (5 V) 56 kΩ ±2% (3 V)
Instructions		Fully compatible within the LCD-II family	
CPU bus timing		1 MHz	1 MHz
Package		FP-80B, TFP-80, and 80-pin bare chip (no package)	144-pin bare chip (no package) and FP-144A

LCD-II/E20 Block Diagram



LCD-II/E20 Pad Arrangement



Note: * : Test pins to be grounded
□ : Power supply pins
■ : Power supply pins (ground)
▨ : Input pins
▯ : Output pins
⊠ : Input/Output pins

Minimum pad pitch = 130 µm

HCD66702 Pad Location Coordinates

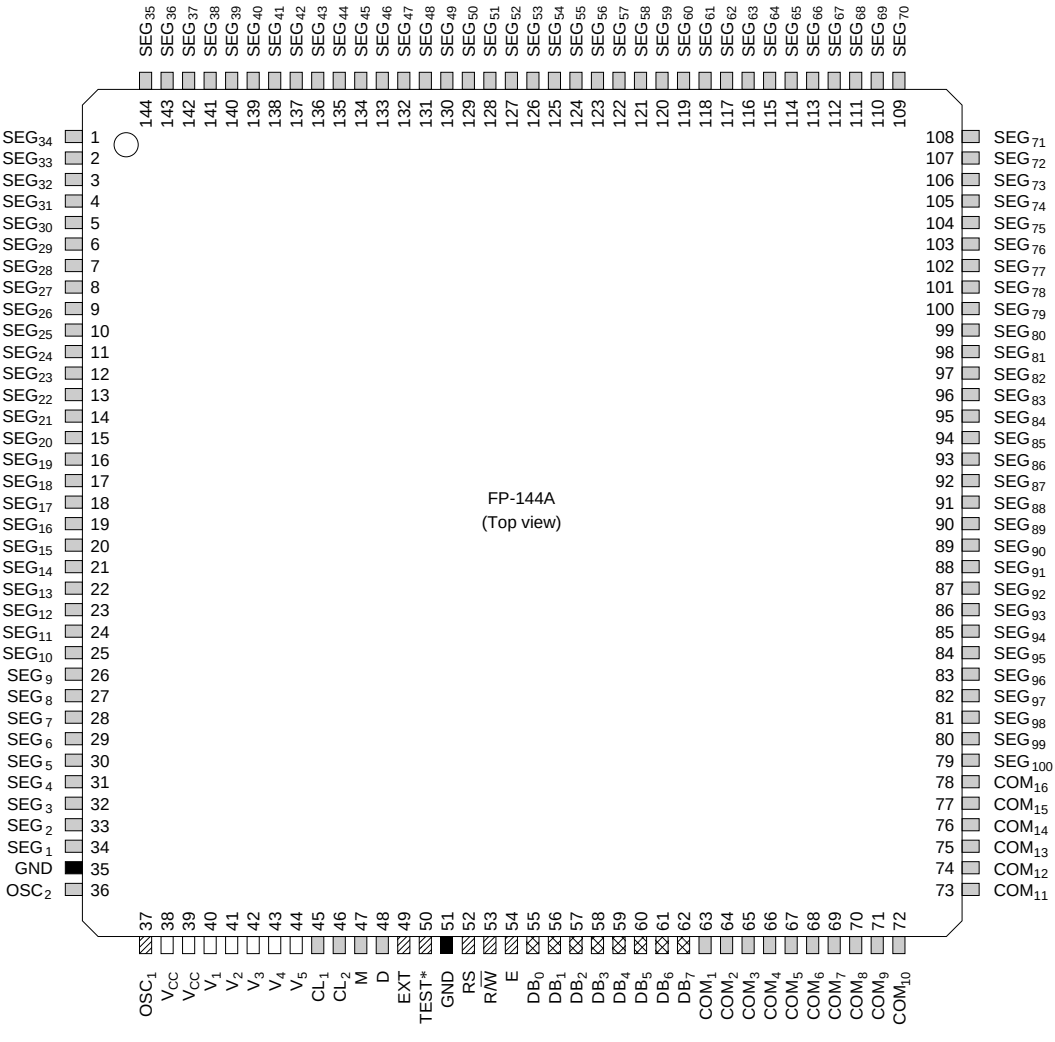
Pad No.	Pad Name	X (µm)	Y (µm)
1	SEG_{34}	–2475	2350
2	SEG_{33}	–2475	2205
3	SEG_{32}	–2475	2065
4	SEG_{31}	–2475	1925
5	SEG_{30}	–2475	1790
6	SEG_{29}	–2475	1655
7	SEG_{28}	–2475	1525
8	SEG_{27}	–2475	1395
9	SEG_{26}	–2475	1265
10	SEG_{25}	–2475	1135
11	SEG_{24}	–2475	1005
12	SEG_{23}	–2475	875
13	SEG_{22}	–2475	745
14	SEG_{21}	–2475	615
15	SEG_{20}	–2475	485
16	SEG_{19}	–2475	355
17	SEG_{18}	–2475	225
18	SEG_{17}	–2475	95
19	SEG_{16}	–2475	–35
20	SEG_{15}	–2475	–165
21	SEG_{14}	–2475	–295
22	SEG_{13}	–2475	–425
23	SEG_{12}	–2475	–555
24	SEG_{11}	–2475	–685
25	SEG_{10}	–2475	–815
26	SEG_{9}	–2475	–945
27	SEG_{8}	–2475	–1075
28	SEG_{7}	–2475	–1205
29	SEG_{6}	–2475	–1335
30	SEG_{5}	–2475	–1465
31	SEG_{4}	–2475	–1600
32	SEG_{3}	–2475	–1735
33	SEG_{2}	–2475	–1870
34	SEG_{1}	–2475	–2010
35	GND	–2475	–2180
36	OSC_2	–2475	–2325
37	OSC_1	–2445	–2475
38	V_{CC}	–2305	–2475
39	V_{CC}	–2165	–2475
40	V_1	–2025	–2475
41	V_2	–1875	–2475
42	V_3	–1745	–2475
43	V_4	–1595	–2475
44	V_5	–1465	–2475
45	CL_1	–1335	–2475
46	CL_2	–1185	–2475
47	M	–1055	–2475
48	D	–905	–2475
49	EXT	–775	–2475
50	TEST	–625	–2475
51	GND	–495	–2475
52	RS	–345	–2475
53	$R/\overline{W}$	–195	–2475
54	E	–45	–2475
55	DB_0	85	–2475
56	DB_1	235	–2475
57	DB_2	365	–2475
58	DB_3	515	–2475
59	DB_4	645	–2475
60	DB_5	795	–2475

Pad No.	Pad Name	X (µm)	Y (µm)
61	DB_6	925	–2475
62	DB_7	1075	–2475
63	COM_1	1205	–2475
64	COM_2	1335	–2475
65	COM_3	1465	–2475
66	COM_4	1595	–2475
67	COM_5	1725	–2475
68	COM_6	1855	–2475
69	COM_7	1990	–2475
70	COM_8	2125	–2475
71	COM_9	2265	–2475
72	COM_{10}	2410	–2475
73	COM_{11}	2475	–2290
74	COM_{12}	2475	–2145
75	COM_{13}	2475	–2005
76	COM_{14}	2475	–1865
77	COM_{15}	2475	–1730
78	COM_{16}	2475	–1595
79	SEG_{100}	2475	–1465
80	SEG_{99}	2475	–1335
81	SEG_{98}	2475	–1205
82	SEG_{97}	2475	–1075
83	SEG_{96}	2475	–945
84	SEG_{95}	2475	–815
85	SEG_{94}	2475	–685
86	SEG_{93}	2475	–555
87	SEG_{92}	2475	–425
88	SEG_{91}	2475	–295
89	SEG_{90}	2475	–165
90	SEG_{89}	2475	–35
91	SEG_{88}	2475	95
92	SEG_{87}	2475	225
93	SEG_{86}	2475	355
94	SEG_{85}	2475	485
95	SEG_{84}	2475	615
96	SEG_{83}	2475	745
97	SEG_{82}	2475	875
98	SEG_{81}	2475	1005
99	SEG_{80}	2475	1135
100	SEG_{79}	2475	1265
101	SEG_{78}	2475	1395
102	SEG_{77}	2475	1525
103	SEG_{76}	2475	1655
104	SEG_{75}	2475	1790
105	SEG_{74}	2475	1925
106	SEG_{73}	2475	2065
107	SEG_{72}	2475	2205
108	SEG_{71}	2475	2350
109	SEG_{70}	2320	2475
110	SEG_{69}	2175	2475
111	SEG_{68}	2035	2475
112	SEG_{67}	1895	2475
113	SEG_{66}	1760	2475
114	SEG_{65}	1625	2475
115	SEG_{64}	1495	2475
116	SEG_{63}	1365	2475
117	SEG_{62}	1235	2475
118	SEG_{61}	1105	2475
119	SEG_{60}	975	2475
120	SEG_{59}	845	2475

Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
121	SEG_{58}	715	2475	133	SEG_{46}	–845	2475
122	SEG_{57}	585	2475	134	SEG_{45}	–975	2475
123	SEG_{56}	455	2475	135	SEG_{44}	–1105	2475
124	SEG_{55}	325	2475	136	SEG_{43}	–1235	2475
125	SEG_{54}	195	2475	137	SEG_{42}	–1365	2475
126	SEG_{53}	65	2475	138	SEG_{41}	–1495	2475
127	SEG_{52}	–65	2475	139	SEG_{40}	–1625	2475
128	SEG_{51}	–195	2475	140	SEG_{39}	–1760	2475
129	SEG_{50}	–325	2475	141	SEG_{38}	–1895	2475
130	SEG_{49}	–455	2475	142	SEG_{37}	–2035	2475
131	SEG_{48}	–585	2475	143	SEG_{36}	–2175	2475
132	SEG_{47}	–715	2475	144	SEG_{35}	–2320	2475

Notes: 1. Coordinates originate from the chip center.
2. The above are preliminary specifications, and may be subject to change.

HD66702 Pin Arrangement



Note: * : Test pins to be grounded
□ : Power supply pins
■ : Power supply pins (ground)
▨ : Input pins
▭ : Output pins
⊠ : Input/Output pins

Pin Functions

Table 1 Pin Functional Description

Signal	I/O	Device Interfaced with	Function
RS	I	MPU	Selects registers 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/$\overline{W}$	I	MPU	Selects read or write 0: Write 1: Read
E	I	MPU	Starts data read/write
DB_4 to DB_7	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. DB_7 can be used as a busy flag.
DB_0 to DB_3	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the LCD-II/E20. These pins are not used during 4-bit operation.
CL_1	O	HD44100	Clock to latch serial data D sent to the HD44100H driver
CL_2	O	HD44100	Clock to shift serial data D
M	O	HD44100	Switch signal for converting the liquid crystal drive waveform to AC
D	O	HD44100	Character pattern data corresponding to each segment signal
COM_1 to COM_{16}	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM_9 to COM_{16} are non-selection waveforms at 1/8 duty factor and COM_{12} to COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1 to SEG_{100}	O	LCD	Segment signals
V_1 to V_5	—	Power supply	Power supply for LCD drive
V_{CC}, GND	—	Power supply	V_{CC}: +5 V or +3 V, GND: 0 V
TEST	I	—	Test pin, which must be grounded
EXT	I	—	0: Enables extension driver control signals CL_1, CL_2, M, and D to be output from its corresponding pins. 1: Drives CL_1, CL_2, M, and D as tristate, lowering power dissipation.
OSC_1, OSC_2	—	—	Pins for connecting the registers of the internal clock oscillation. When the pin input is an external clock, it must be input to OSC_1.

Function Description

Registers

The HD66702 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into DD RAM or CG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM or CG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66702 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output to DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DD RAM and CG RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DD RAM or CG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM or CG RAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and R/$\overline{W}$ = 1 (table 2).

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM or CG RAM)
1	1	DR read as an internal operation (DD RAM or CG RAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM. See figure 1 for the relationships between DD RAM addresses and positions on the liquid crystal display.

The DD RAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (figure 2)

  — Case 1: When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66702, 20 characters are displayed. See figure 3.

  When the display shift operation is performed, the DD RAM address shifts. See figure 3.

  — Case 2: For a 28-character display, the HD66702 can be extended using one HD44100 and displayed. See figure 4.

  When the display shift operation is performed, the DD RAM address shifts. See figure 4.

  — Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased through the use of two or more HD44100s can be considered as an extension of case #2.

  Since the increase can be eight digits per additional HD44100, up to 80 digits can be displayed by externally connecting eight HD44100s. See figure 5.

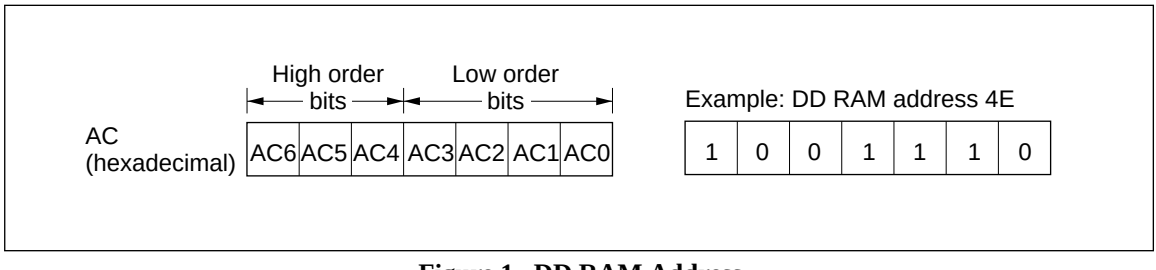


Figure 1 DD RAM Address

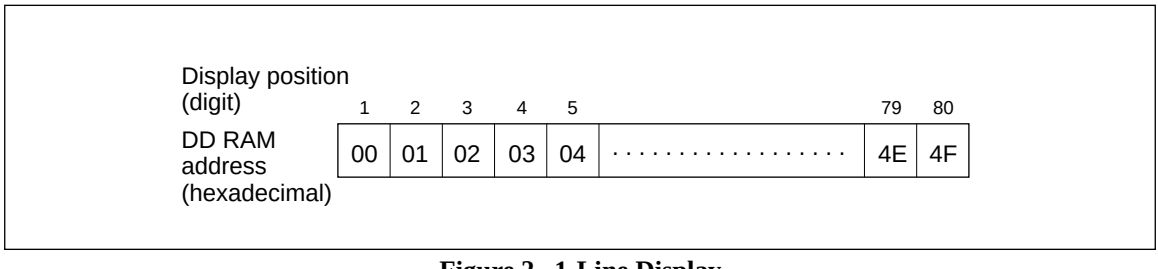


Figure 2 1-Line Display

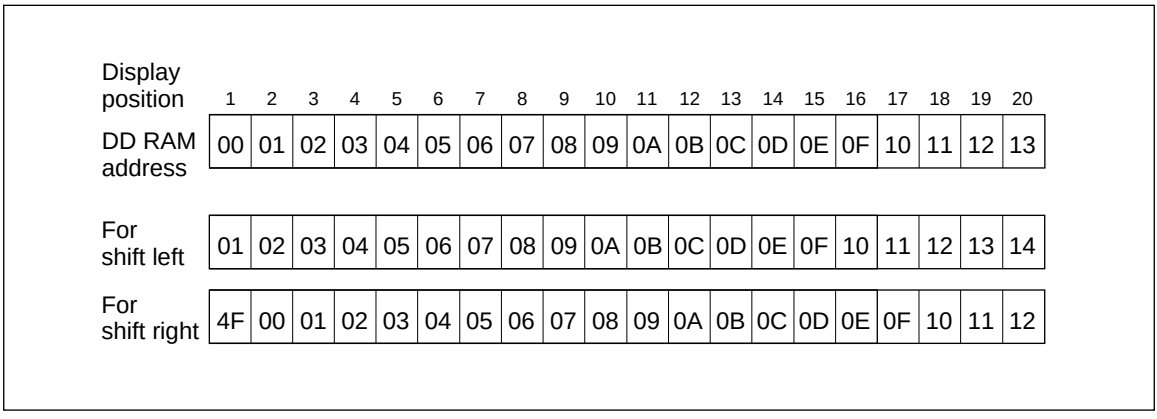


Figure 3 1-Line by 20-Character Display Example

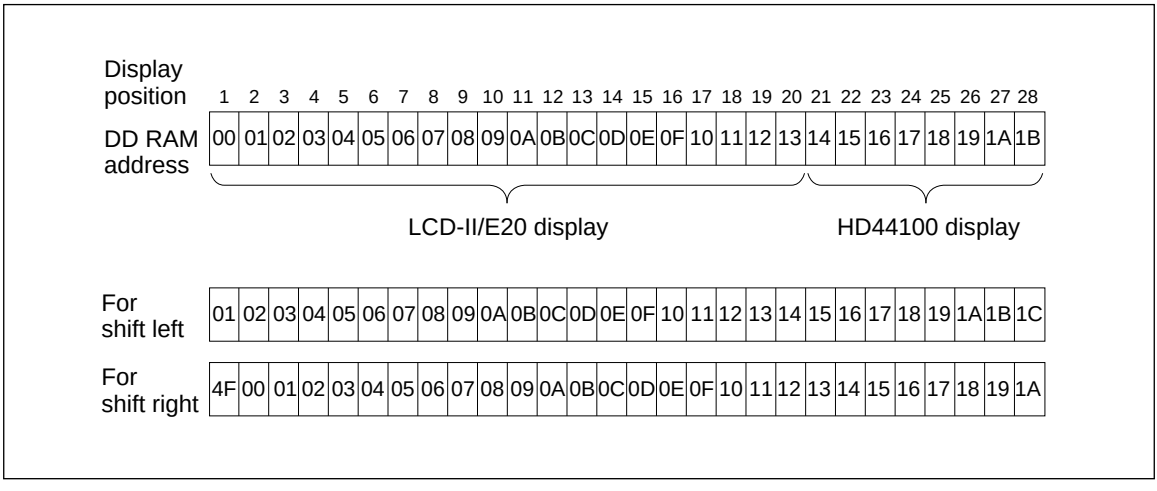


Figure 4 1-Line by 28-Character Display Example

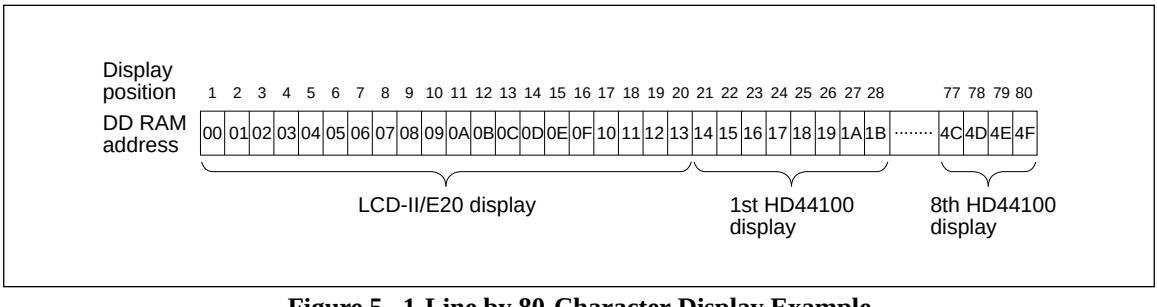


Figure 5 1-Line by 80-Character Display Example

- 2-line display (N = 1) (figure 6)

  — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD66702 is used, 20 characters × 2 lines are displayed. See figure 7.

  When display shift operation is performed, the DD RAM address shifts. See figure 7.

Display position	1	2	3	4	5		39	40
DD RAM address (hexadecimal)	00	01	02	03	04	· · · · · · · · · · · · · · · · · ·	26	27
	40	41	42	43	44	· · · · · · · · · · · · · · · · · ·	66	67

Figure 6 2-Line Display

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
For shift left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54
For shift right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52

Figure 7 2-Line by 20-Character Display Example

— Case 2: For a 28-character × 2-line display, the HD66702 can be extended using one HD44100. See figure 8.

When display shift operation is performed, the DD RAM address shifts. See figure 8.

— Case 3: The relationship between the display position and DD RAM address when the number of display digits is increased by using two or more HD44100s, can be considered as an extension of case #2. See figure 9.

Since the increase can be 8 digits × 2 lines for each additional HD44100, up to 40 digits × 2 lines can be displayed by externally connecting three HD44100s.

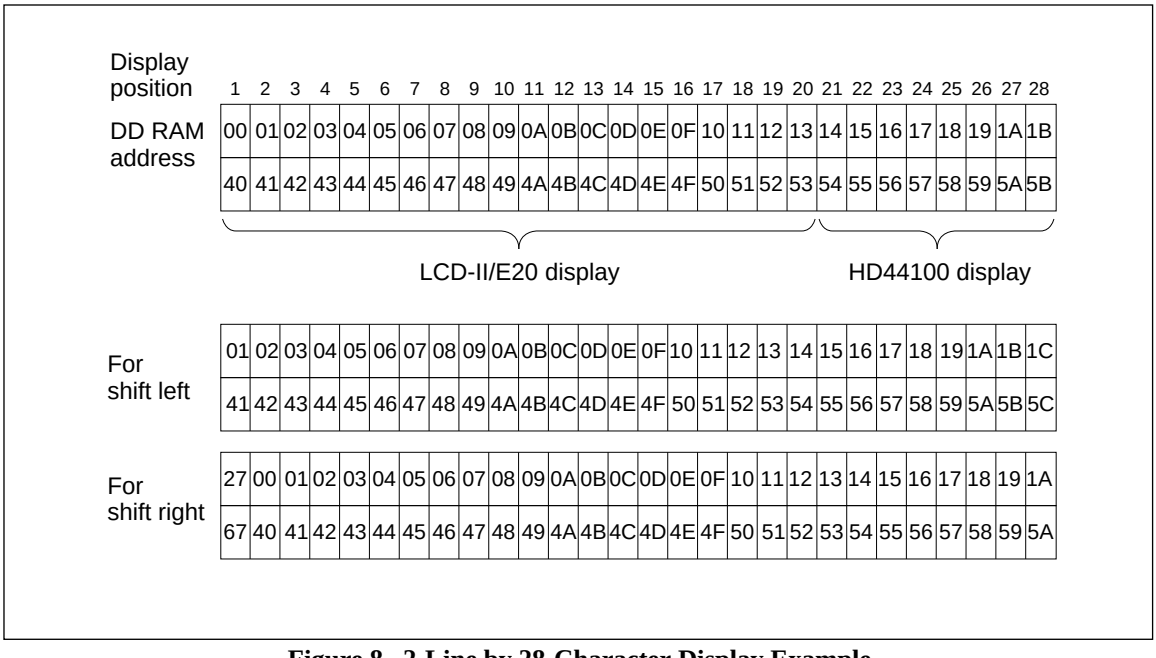


Figure 8 2-Line by 28-Character Display Example

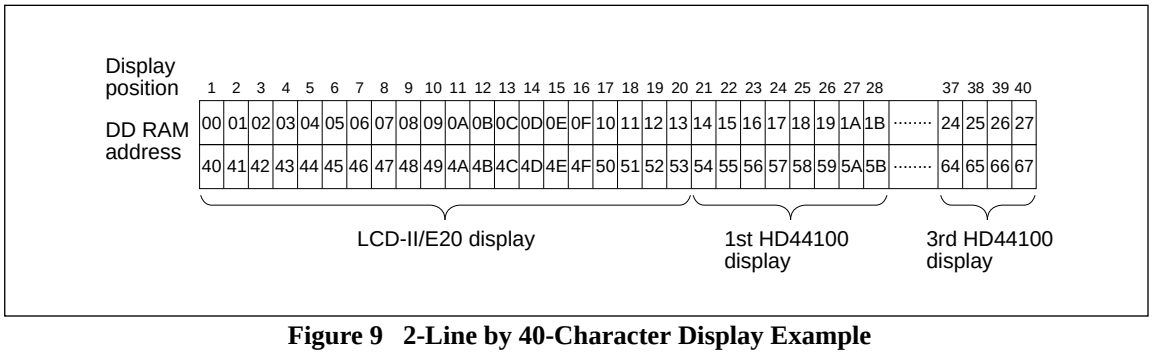


Figure 9 2-Line by 40-Character Display Example

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes (table 5). It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 7 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write the character codes at the addresses shown as the left column of table 5 to show the character patterns stored in CG RAM.

See table 6 for the relationship between CG RAM addresses and data and display patterns.

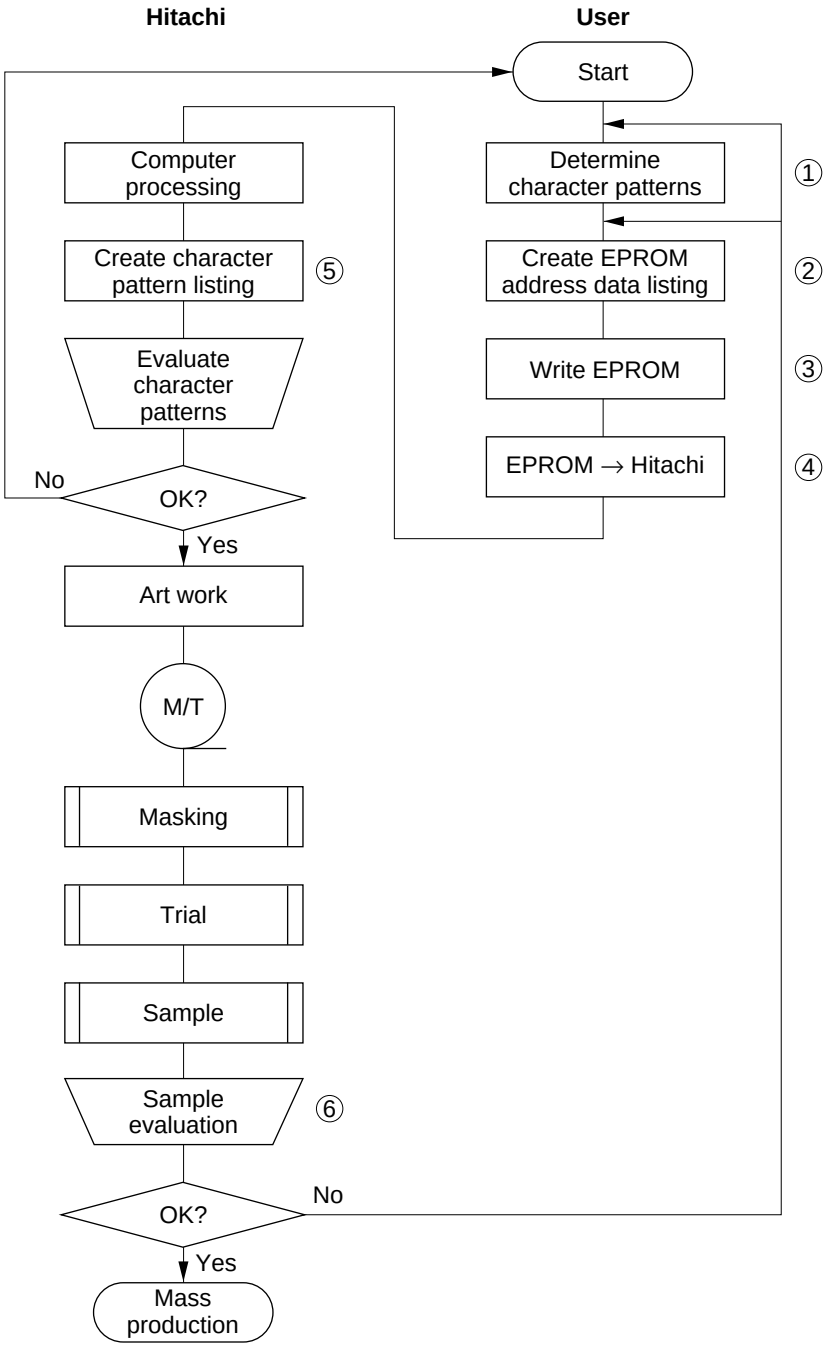
Areas that are not used for display can be used as general data RAM.

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 10 Character Pattern Development Procedure

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II/E20 character generator ROM can generate 160 5×7 dot character patterns and 32 5×10 dot character patterns for a total of 192 different character patterns.

— 5×7 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5×7 dot character pattern (table 3).

Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5×7 dots)

EPROM Address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	LSB O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Character code — Line position

← Fill line 8 (cursor position) with 0s

Notes:
1. EPROM addresses A_{10} to A_3 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Line 8 (cursor position) of the character pattern must be blanked with 0s.
6. EPROM data O_5 to O_7 are not used.

— 5 × 10 dot character pattern

EPROM address data and character pattern data correspond with each other to form a 5 × 10 dot character pattern (table 4).

— Handling unused character patterns

1. **EPROM data outside the character pattern area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.
2. **EPROM data in CG RAM area:** Ignored by the character generator ROM for display operation so 0 or 1 is arbitrary.
3. **EPROM data used when the user does not use any HD66702 character pattern:** According to the user application, handled in one of the two ways listed as follows.
   a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)
   b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 4 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM Address												Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		O_4	O_3	O_2	O_1	LSB O_0
								0	0	0		0	0	0	0	0
								0	0	1		0	0	0	0	0
								0	1	0		0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1		1	0	0	1	1
								1	0	0		1	0	0	0	1
								1	0	1		1	0	0	0	1
								1	1	0		0	1	1	1	1
								1	1	1		0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0		0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1		0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0		0	0	0	0	0

← Fill line 11 (cursor position) with 0s

Character code — Line position

Notes:
1. EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern lines 9, 10, and 11 to 0s.
2. EPROM addresses A_2 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. A lit display position (black) corresponds to a 1.
5. Blank out line 11 (cursor position) of the character pattern with 0s.
6. EPROM data O_5 to O_7 are not used.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A00)

Lower 4 Bits \ Upper 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Note: The user can specify any pattern for character-generator RAM.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A01)

Upper 4 Bits / Lower 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A02)

Upper 4 Bits / Lower 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

For 5 × 7 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low	7 6 5 4 3 2 1 0 High Low	
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * 0 0 0 0 0	Character pattern Cursor position
0 0 0 0 * 0 0 1	0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * 0 0 0 0 0	
0 0 0 0 * 1 1 1	1 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 0 1 1 1	* * *	

Notes: 1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).

2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left). Since CG RAM data bits 5 to 7 are not used for display, they can be used for general data RAM.
4. As shown tables 5 and 6, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Table 6 Relationship between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data) (cont)

For 5 × 10 dot character patterns

Character Codes (DD RAM data)	CG RAM Address	Character Patterns (CG RAM data)	
7 6 5 4 3 2 1 0 High Low	5 4 3 2 1 0 High Low	7 6 5 4 3 2 1 0 High Low	
0 0 0 0 * 0 0 *	0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0	* * * 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 1 1 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 * * * 0 0 0 0 0	Character pattern Cursor position
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * *	
0 0 0 0 * 1 1 *	0 0 0 0 0 0 0 1 1 0 0 1 1 0 1 0	* * * * * *	
	1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	* * * * * * * * * * * * * * * *	

Notes: 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits: 4 types).

2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.
   If the 11th line data is 1, 1 bits will light up the 11th line regardless of the cursor presence.
   Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area. This circuit also generates timing signals for the operation of the externally connected HD44100 driver.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the HD44100 driver. Character pattern data is sent serially through a 100-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs. The serial data can be sent to externally cascaded HD44100s used for displaying extended digit numbers.

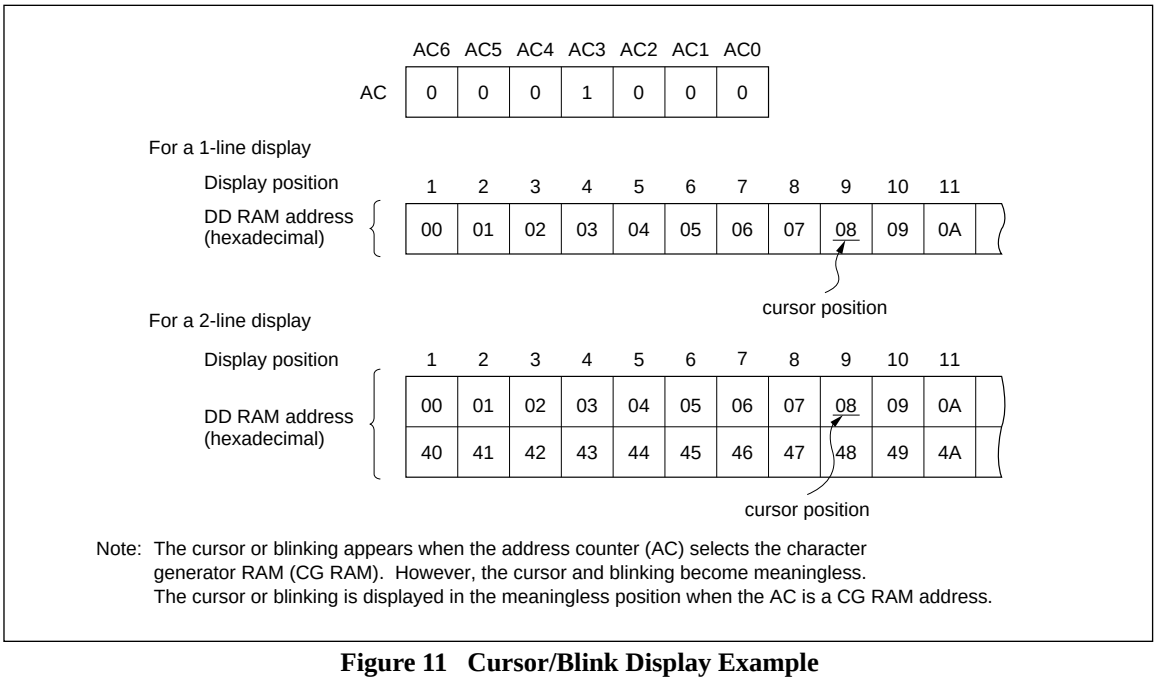
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66702 drives from the head display. The rest of the display, corresponding to latter addresses, are added with each additional HD44100.

Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DD RAM) address set in the address counter (AC).

For example (figure 11), when the address counter is 08H, the cursor position is displayed at DD RAM address 08H.



Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CG RAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CG RAM address.

Figure 11 Cursor/Blink Display Example

Interfacing to the MPU

The HD66702 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66702 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

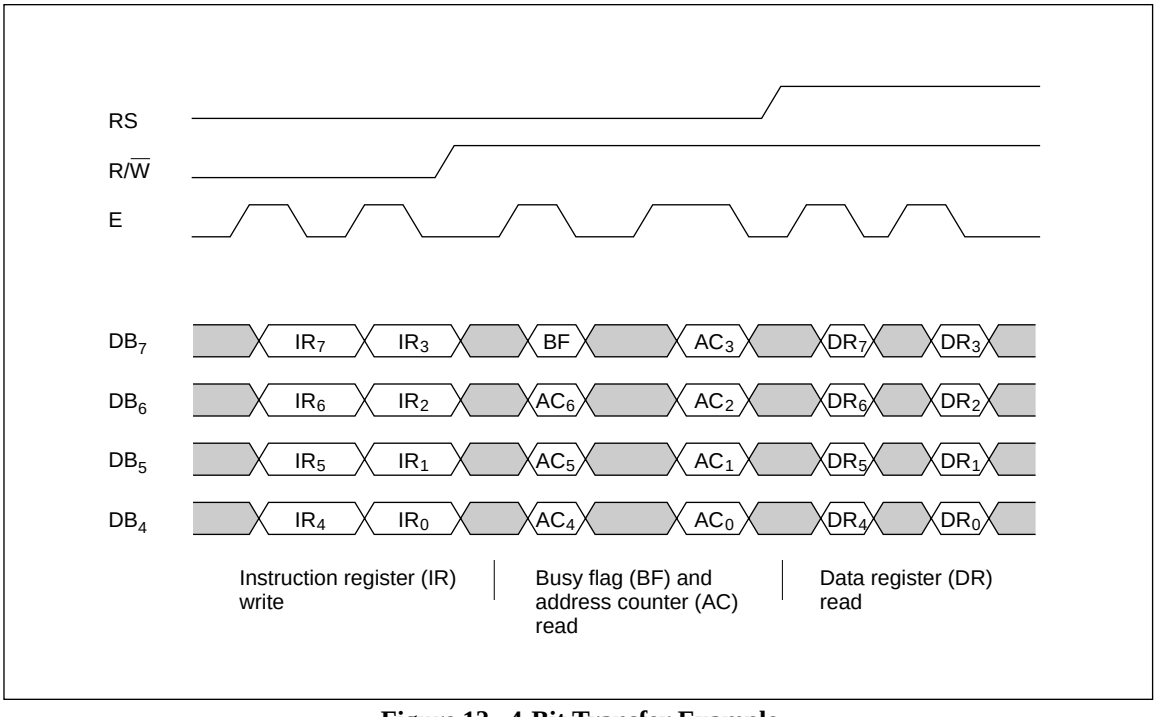


Figure 12 4-Bit Transfer Example

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66702 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 7 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66702. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66702 can be controlled by the MPU. Before starting the internal operation of the HD66702, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66702 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{W}$), and the data bus (DB_0 to DB_7), make up the HD66702 instructions (table 7). There are four categories of instructions that:

- Designate HD66702 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66702 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 12) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66702 is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD66702. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 7 for the list of each instruc-tion execution time.

Table 7 Instructions

Instruction	Code										Description	Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.28 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.28 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	31 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	31 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	31 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (L), and character font (F).	31 µs
Set CG RAM address	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	31 µs
Set DD RAM address	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	31 µs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs

Table 7 Instructions (cont)

Instruction	Code RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 320 kHz)
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	31 µs t_{ADD} = 4.7 µs*
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5 × 10 dots, F = 0: 5 × 7 dots BF = 1: Internally operating BF = 0: Instructions acceptable										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM addresses	Execution time changes when frequency changes Example: When f_{cp} or f_{OSC} is 270 kHz, $31\ \mu s \times \frac{320}{270} = 37\ \mu s$

Note: — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 13, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

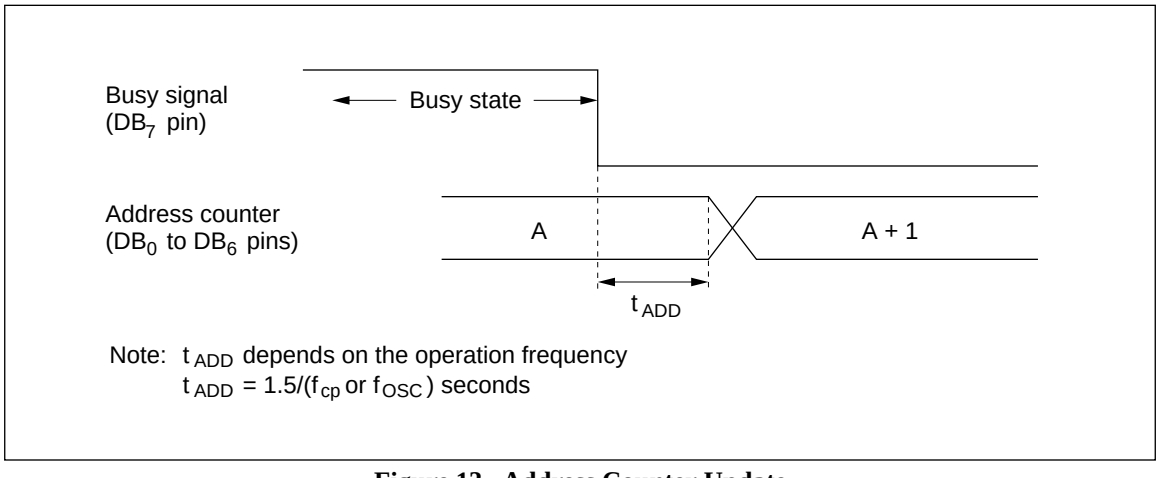


Figure 13 Address Counter Update

Instruction Description

Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

Display On/Off Control

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5×7 dot character font selection and in the 11th line for the 5×10 dot character font selection (figure 16).

B: The character indicated by the cursor blinks when B is 1 (figure 16). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 320-ms intervals when f_{cp} or f_{OSC} is 320 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 270 kHz, $320 \times 320/270 = 379.2$ ms.)

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

Function Set

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N: Sets the number of display lines.

F: Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

Set CG RAM Address

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

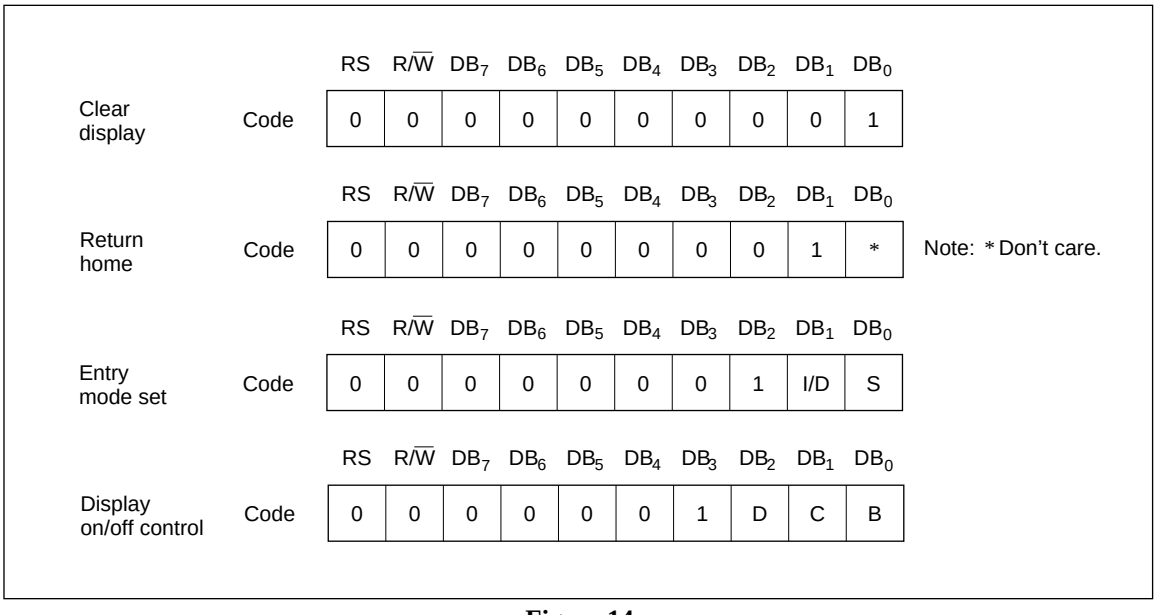


Figure 14

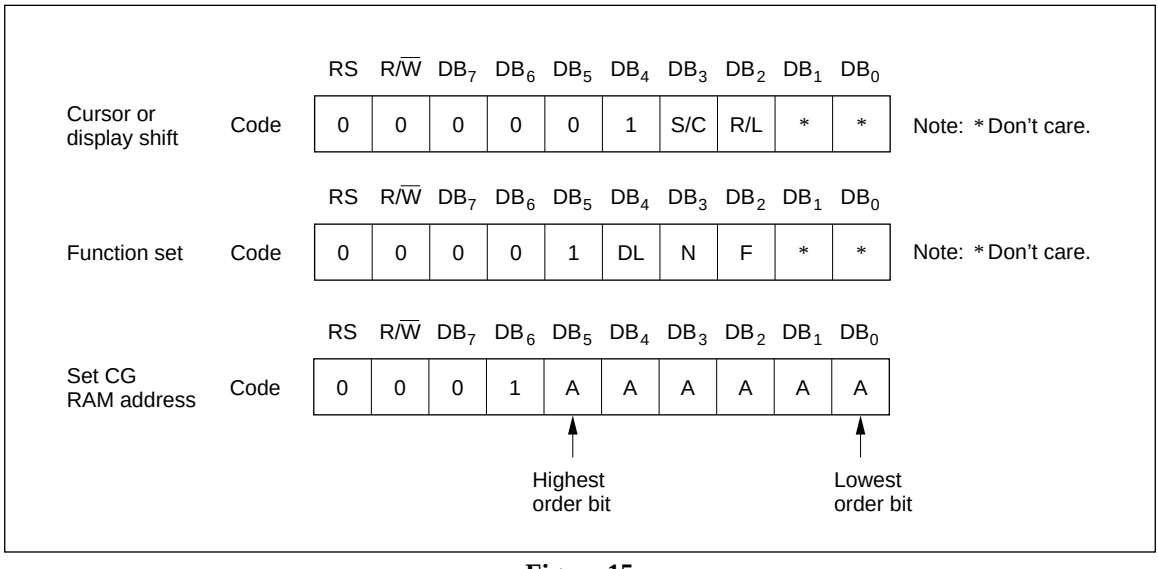


Figure 15

Set DD RAM Address

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

Table 8 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 9 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 7 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 7 dots	1/16	Cannot display two lines for 5 × 10 dot character font.

Note: * Indicates don't care.

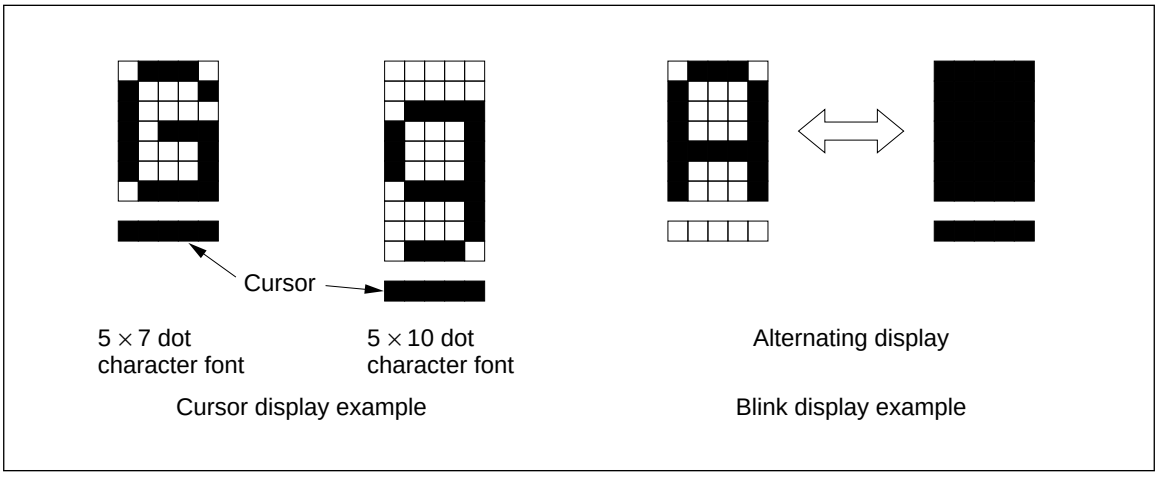


Figure 16 Cursor and Blinking

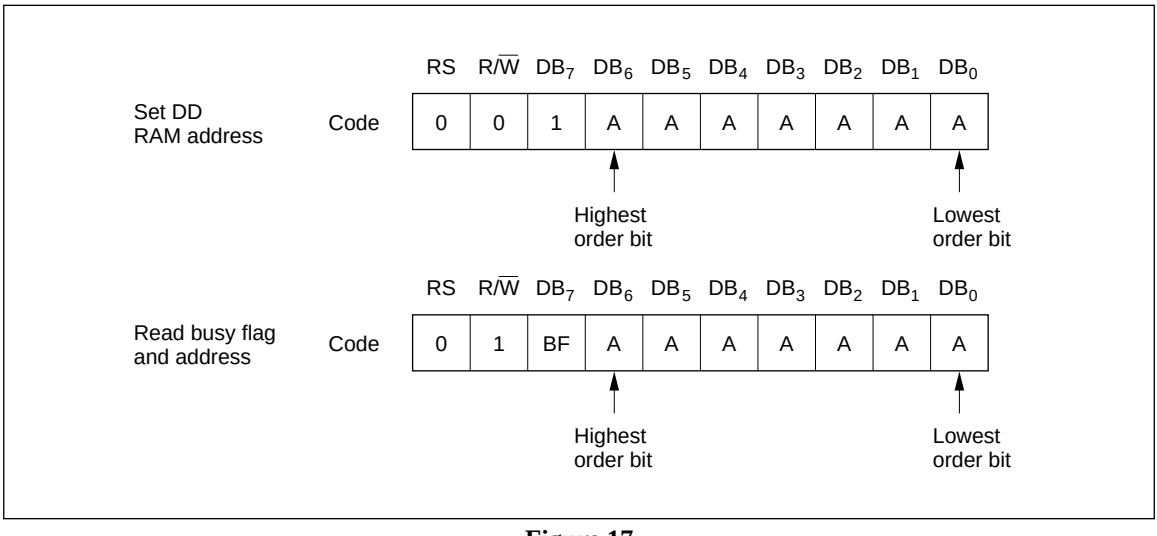


Figure 17

Write Data to CG or DD RAM

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

Read Data from CG or DD RAM

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

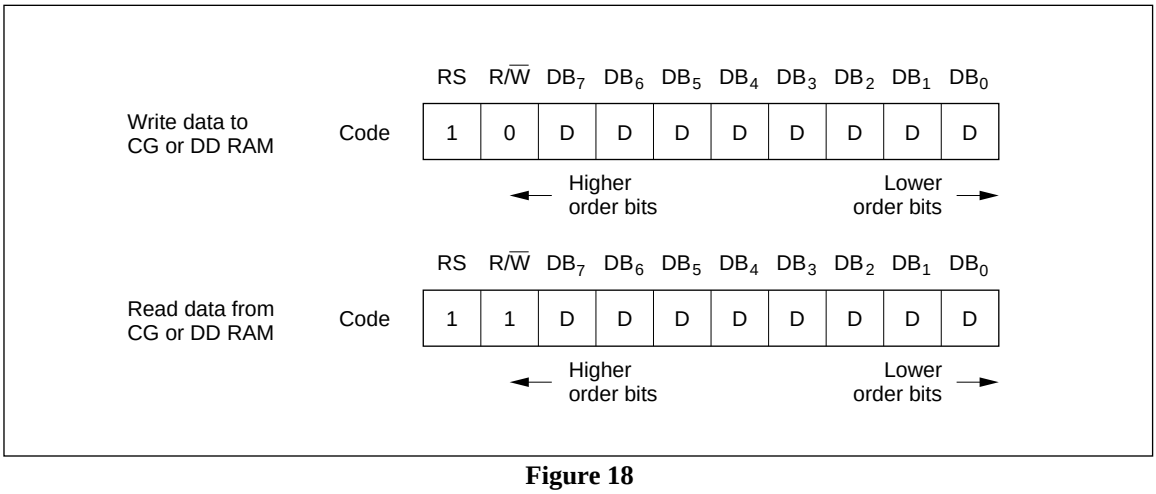


Figure 18

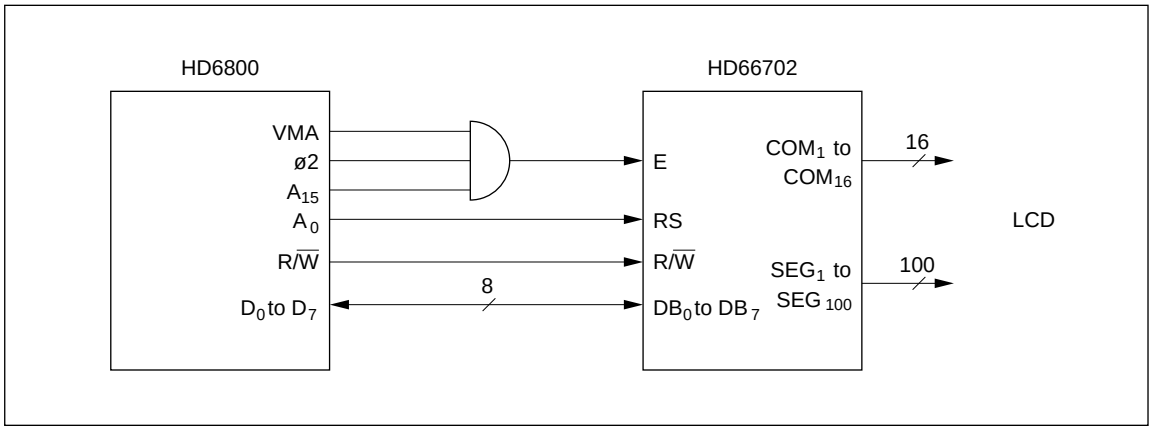


Figure 19 8-Bit MPU Interface

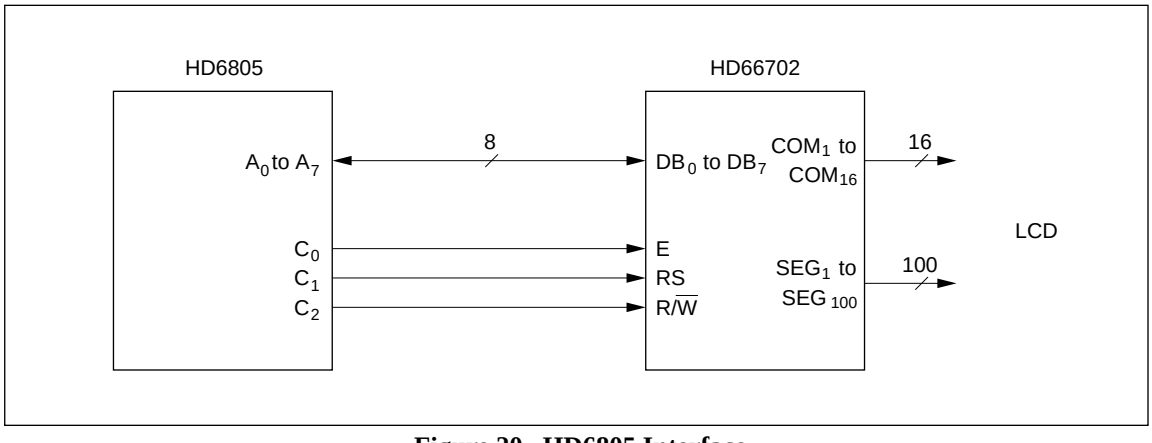


Figure 20 HD6805 Interface

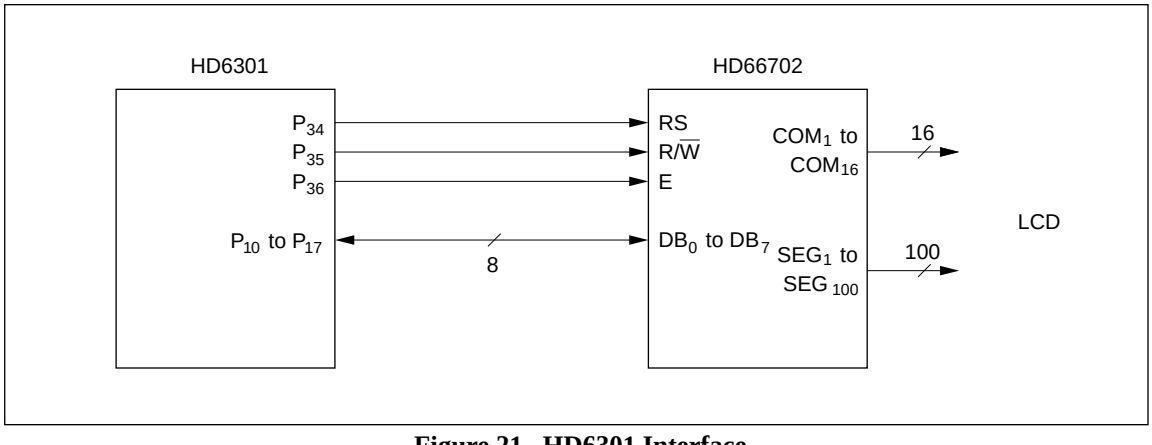


Figure 21 HD6301 Interface

Interfacing the HD66702

Interface to MPUs

- Interfacing to an 8-bit MPU through a PIA

  See figure 23 for an example of using a PIA or I/O port (for a single-chip microcomputer) as an interface device. The input and output of the device is TTL compatible.

In this example, PB_0 to PB_7 are connected to the data bus DB_0 to DB_7, and PA_0 to PA_2 are connected to E, R/$\overline{W}$, and RS, respectively.

Pay careful attention to the timing relationship between E and the other signals when reading or writing data using a PIA for the interface.

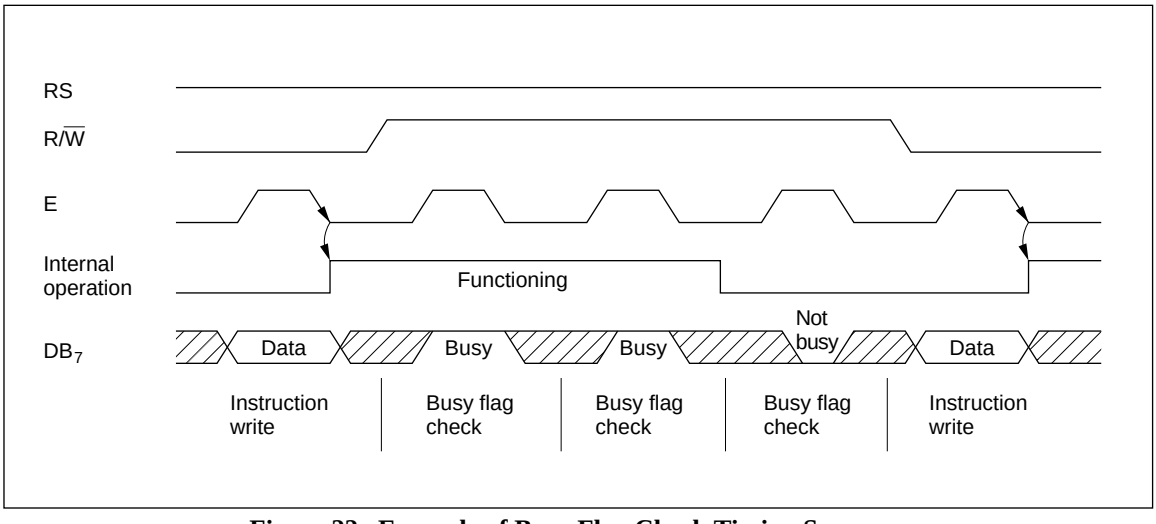


Figure 22 Example of Busy Flag Check Timing Sequence

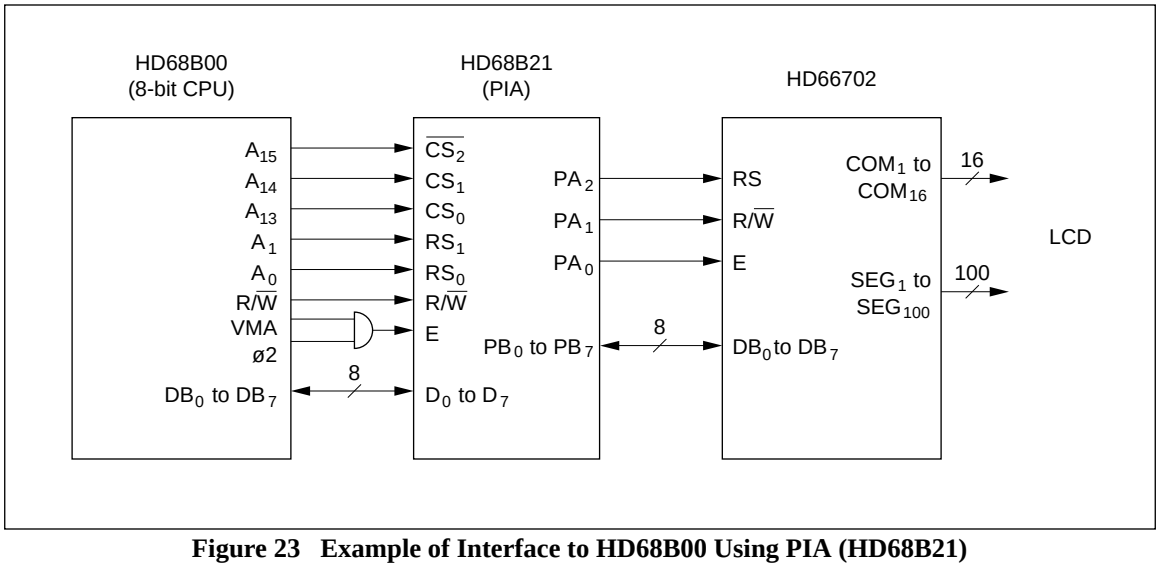


Figure 23 Example of Interface to HD68B00 Using PIA (HD68B21)

- Interfacing to a 4-bit MPU

  The HD66702 can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See figure 24.)

  See figure 25 for an interface example to the HMCS43C.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.

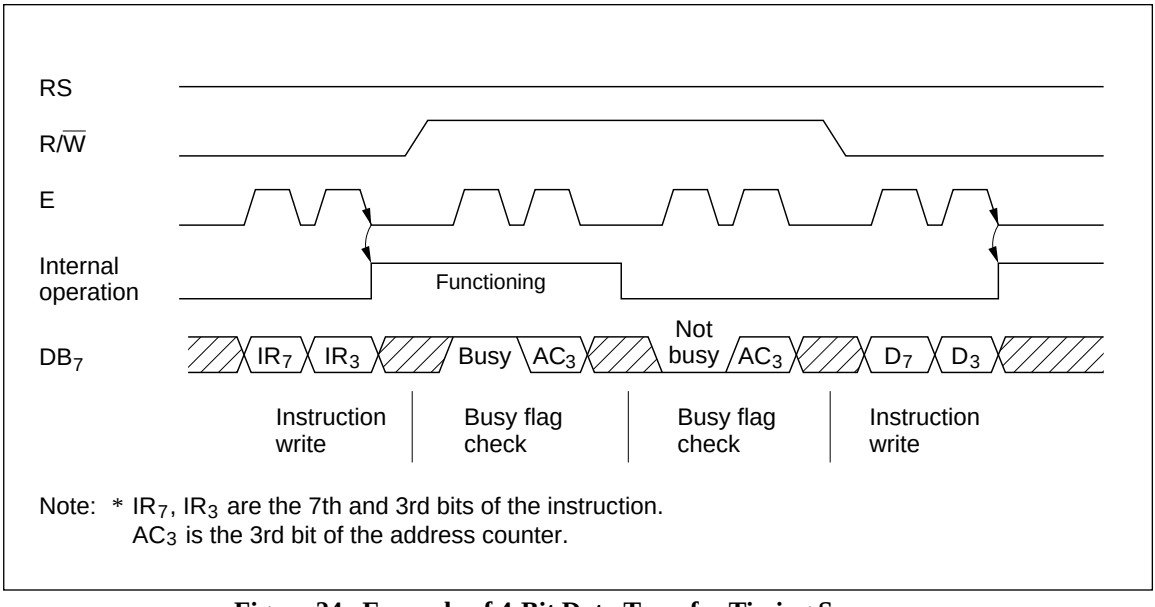


Figure 24 Example of 4-Bit Data Transfer Timing Sequence

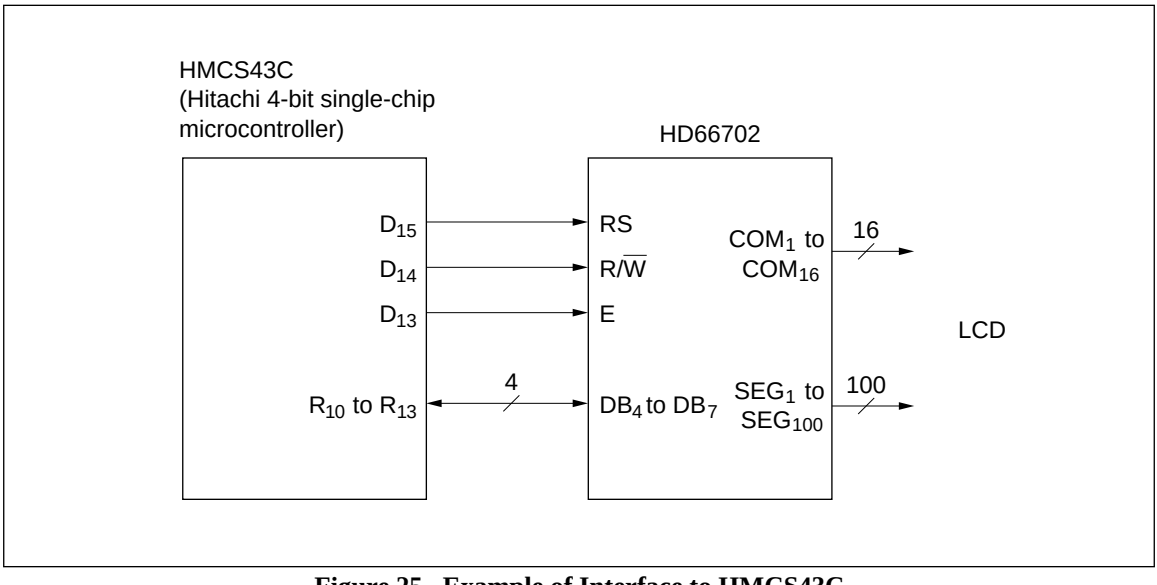


Figure 25 Example of Interface to HMCS43C

Interface to Liquid Crystal Display

Character Font and Number of Lines: The HD66702 can perform two types of displays, 5 × 7 dot and 5 × 10 dot character fonts, each with a cursor.

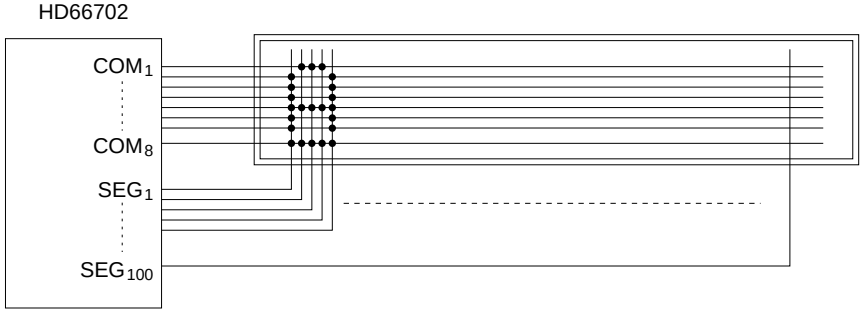
Up to two lines are displayed for 5 × 7 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (table 10).

The number of lines and font types can be selected by the program. (See table 7, Instructions.)

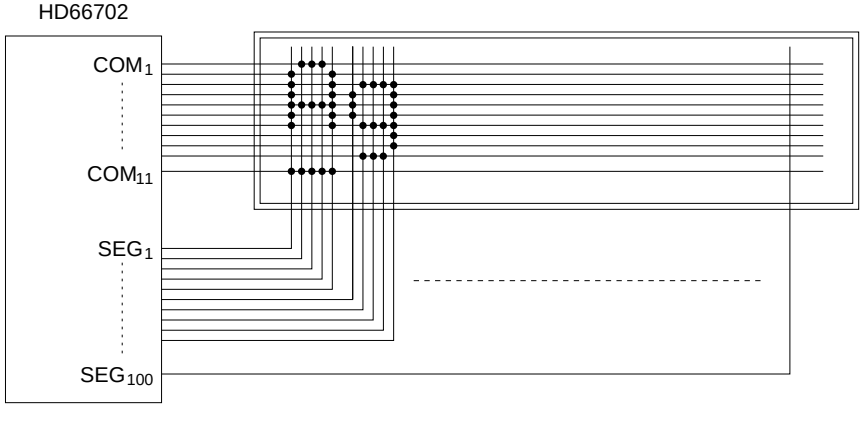
Connection to HD66702 and Liquid Crystal Display: See figure 26 for the connection examples.

Table 10 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + cursor	8	1/8
1	5 × 10 dots + cursor	11	1/11
2	5 × 7 dots + cursor	16	1/16



Example of a 5×7 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

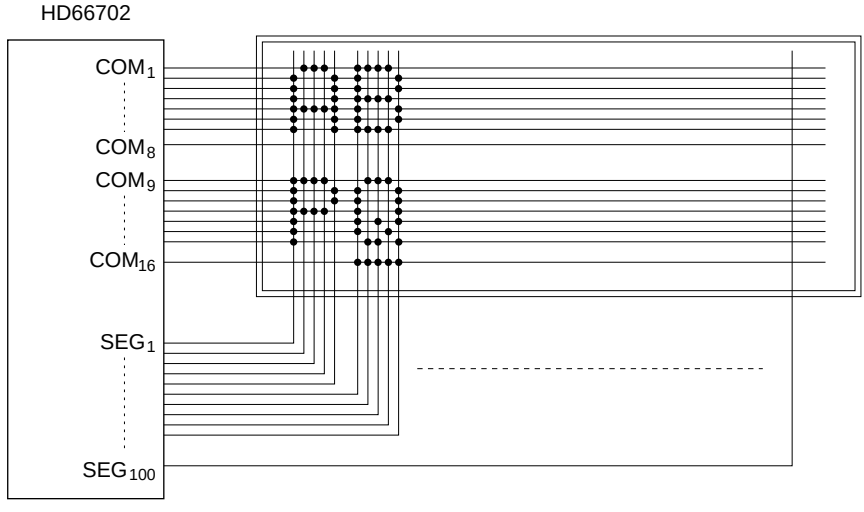


Example of a 5×10 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 26 Liquid Crystal Display and HD66702 Connections

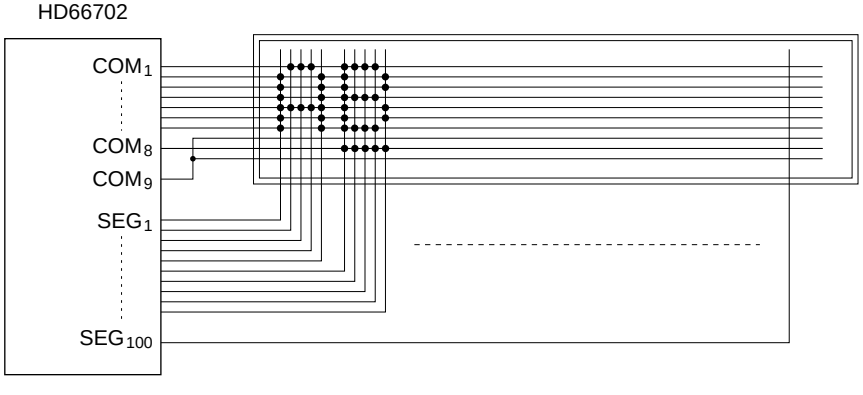
Since five segment signal lines can display one digit, one HD66702 can display up to 20 digits for a 1-line display and 40 digits for a 2-line display.

The examples in figure 26 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (figure 28).



Example of a 5×7 dot, 20-character × 2-line display (1/5 bias, 1/16 duty cycle)

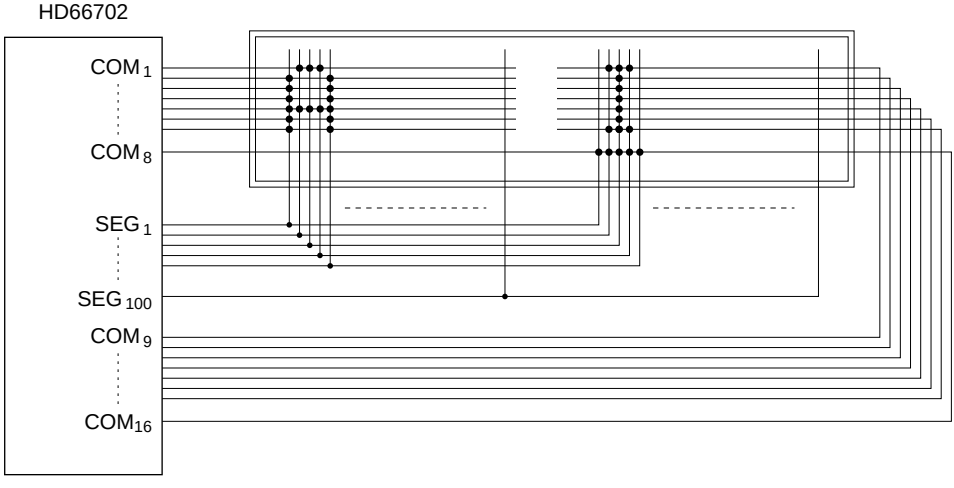
Figure 27 Liquid Crystal Display and HD66702 Connections (cont)



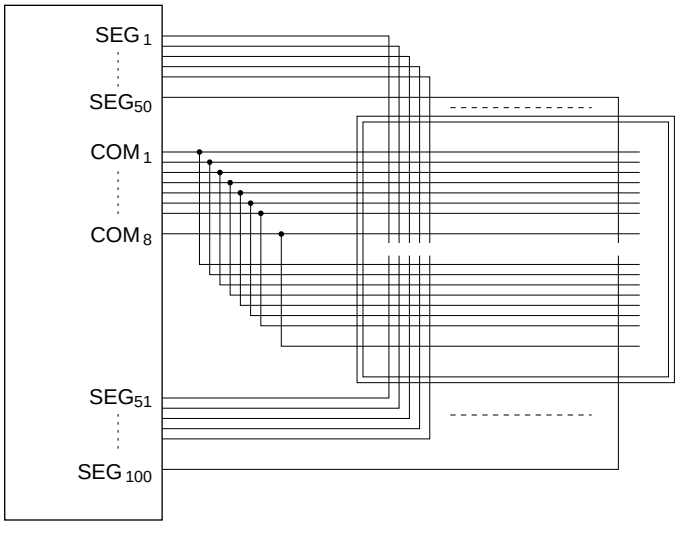
5 × 7 dot, 20-character × 1-line display (1/4 bias, 1/8 duty cycle)

Figure 28 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

Connection of Changed Matrix Layout: In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (figure 29) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DD RAM) addresses for 10 characters × 2 lines and for 40 characters × 1 line are the same as in figure 27.



5 × 7 dot, 40-character × 1-line display
(1/5 bias, 1/16 duty cycle)



5 × 7 dot, 10-character × 2-line display
(1/4 bias, 1/8 duty cycle)

Figure 29 Changed Matrix Layout Displays

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V_1 to V_5 of the HD66702 to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (table 11).

V_{LCD} is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V_1 to V_5 (figure 30).

Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Power Supply	1/4	1/5
V_1	V_{CC}–1/4 V_{LCD}	V_{CC}–1/5 V_{LCD}
V_2	V_{CC}–1/2 V_{LCD}	V_{CC}–2/5 V_{LCD}
V_3	V_{CC}–1/2 V_{LCD}	V_{CC}–3/5 V_{LCD}
V_4	V_{CC}–3/4 V_{LCD}	V_{CC}–4/5 V_{LCD}
V_5	V_{CC}–V_{LCD}	V_{CC}–V_{LCD}

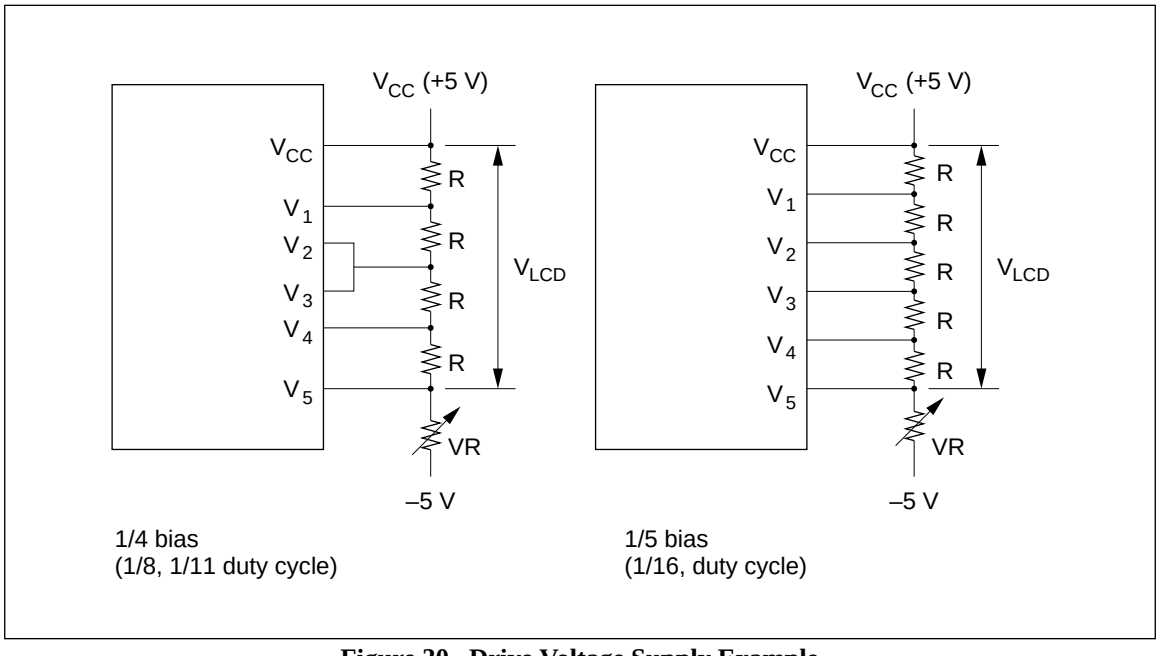


Figure 30 Drive Voltage Supply Example

Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of figure 31 apply only when the oscillation frequency is 320 kHz (one clock pulse of 3.125 µs).

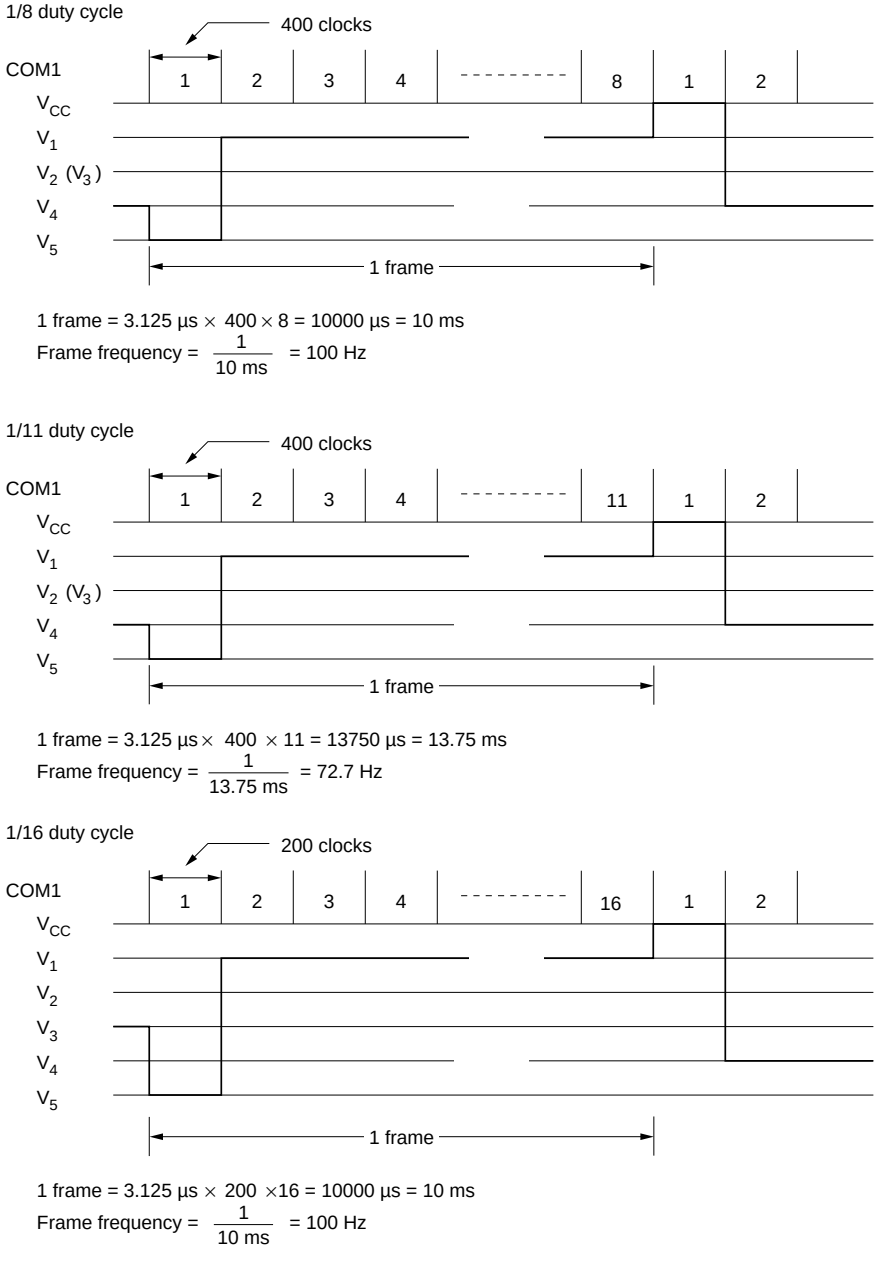


Figure 31 Frame Frequency

Connection with HD44100 Driver

By externally connecting an HD44100 liquid crystal display driver to the HD66702, the number of display digits can be increased. The HD44100 is used as a segment signal driver when connected to the HD66702. The HD44100 can be directly connected to the HD66702 since it supplies CL_1, CL_2, M, and D signals and power for the liquid crystal display drive (figure 32).

Caution: The connection of voltage supply pins V_1 through V_6 for the liquid crystal display drive is somewhat complicated. The EXT pin must be fixed low if the HD44100 is to be connected to the HD66702.

Up to eight HD44100 units can be connected for a 1-line display (duty factor 1/8 or 1/11) and up to three units for a 2-line display (duty factor 1/16). The RAM size limits the HD66702 to a maximum of 80 character display digits. The connection method for both 1-line and 2-line displays or for 5 × 7 and 5 × 10 dot character fonts can remain the same (figure 32).

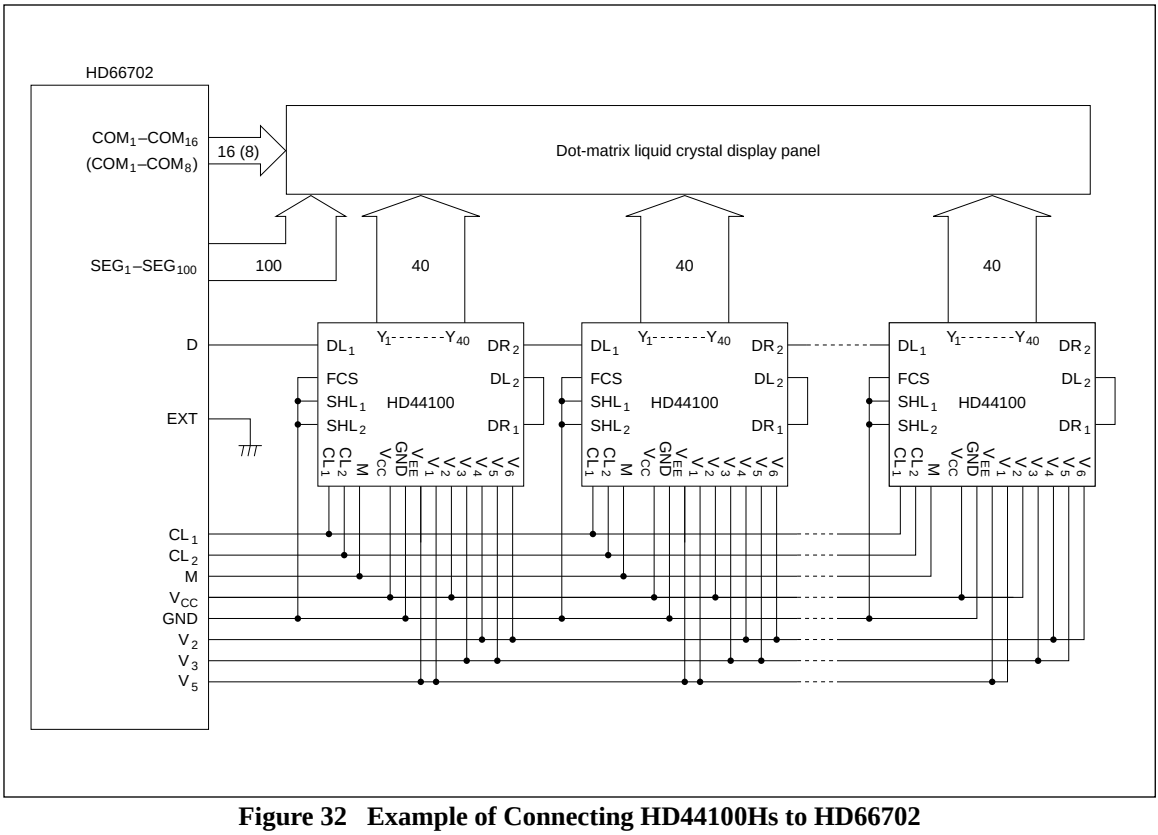


Figure 32 Example of Connecting HD44100Hs to HD66702

Instruction and Display Correspondence

- 8-bit operation, 20-digit × 1-line display with internal reset

Refer to table 12 for an example of an 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

Since the display shift operation changes only the display position with DD RAM contents unchanged, the first display data entered into DD RAM can be output when the return home operation is performed.

- 4-bit operation, 20-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (table 13). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see table 13). Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 20-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 20 characters in the first line, the DD RAM address must be again set after the 20th character is completed. (See table 14.) Note that the display shift operation is performed for the first and second lines. In the example of table 14, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/E20 must be initialized by instructions. (Because the internal reset does not function correctly when V_{CC} is 3 V, it must always be initialized by software.) See the section, Initializing by Instruction.

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	0	1	1	0	0	*	*		Sets to 8-bit operation and selects 1-line display and character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control	0	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HI_	Writes I.
7	⋮										⋮	
8	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
9	Entry mode set	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
10	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
11	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
12	. . . . .										. . . . .	
13	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20	. . . . .										. . . . .	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 13 4-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)							Initialized. No display.
2	Function set							Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
	0	0	0	0	1	0		
3	Function set							Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
	0	0	0	0	1	0		
	0	0	0	0	*	*		
4	Display on/off control						_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0		
	0	0	1	1	1	0		
5	Entry mode set						_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0		
	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM						H_	Writes H. The cursor is incremented by one and shifts to the right.
	1	0	0	1	0	0		
	1	0	1	0	0	0		

Note: The control is the same as for 8-bit operation beyond step #6.

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
1	Power supply on (the HD66702 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set	0	0	0	1	1	1	0	*	*		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	H_	Writes H. DD RAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	. . . . .										. . . . .	
7	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
8	Set DD RAM address	0	0	1	1	0	0	0	0	0	0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the second line.

Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Display	Operation
9	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	HITACHI M_	Writes M.
10	. . . . .										. . . . .	
11	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	1	1	HITACHI MICROCO_	Writes O.
12	Entry mode set 0	0	0	0	0	0	0	1	1	1	HITACHI MICROCO_	Sets mode to shift display at the time of write.
13	Write data to CG RAM/DD RAM 1	0	0	1	0	0	1	1	0	1	ITACHI ICROCOM_	Writes M. Display is shifted to the right. The first and second lines both shift at the same time.
14	. . . . .										. . . . .	
15	Return home 0	0	0	0	0	0	0	0	1	0	HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to figures 33 and 34 for the procedures on 8-bit and 4-bit initializations, respectively.

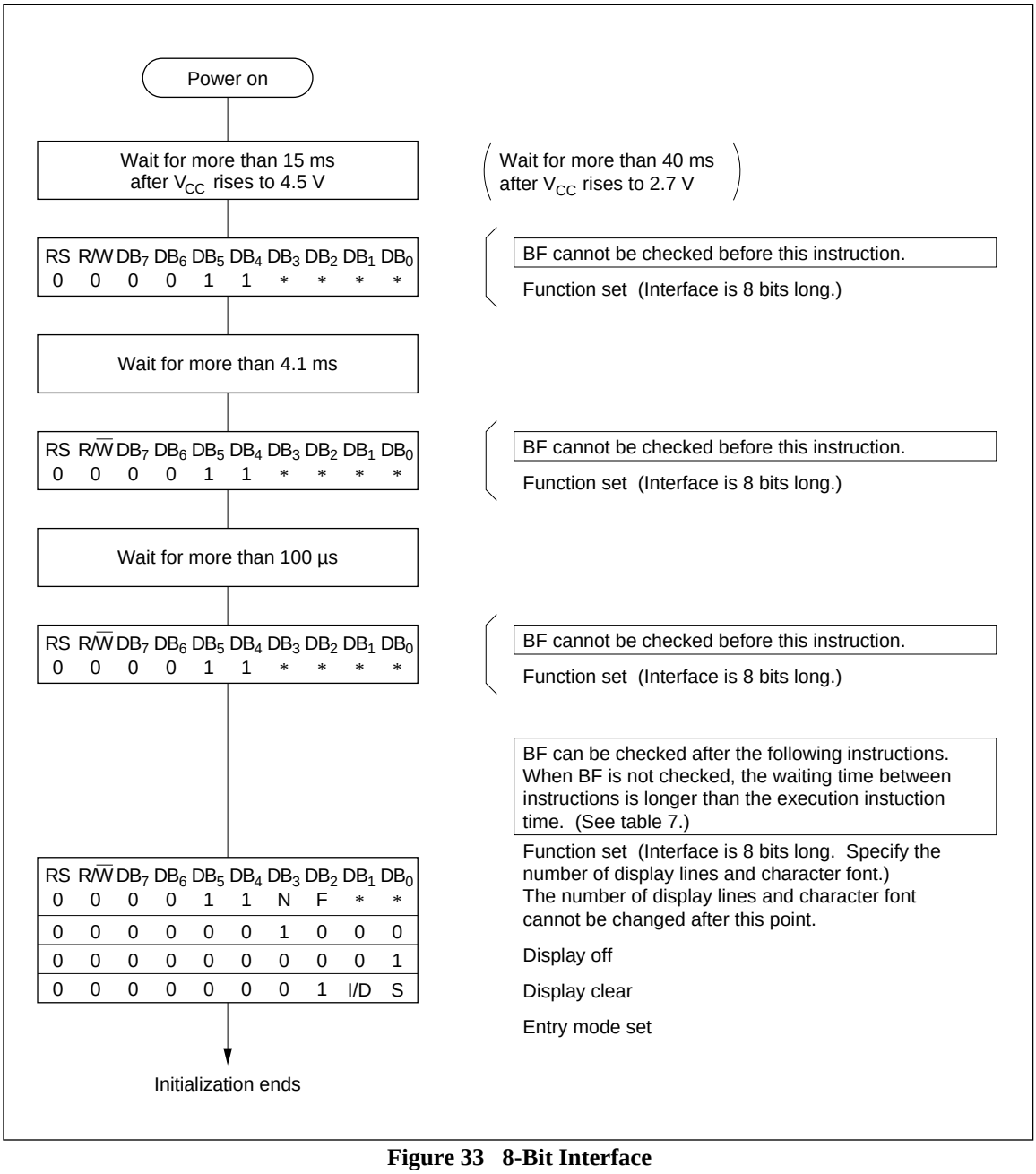


Figure 33 8-Bit Interface

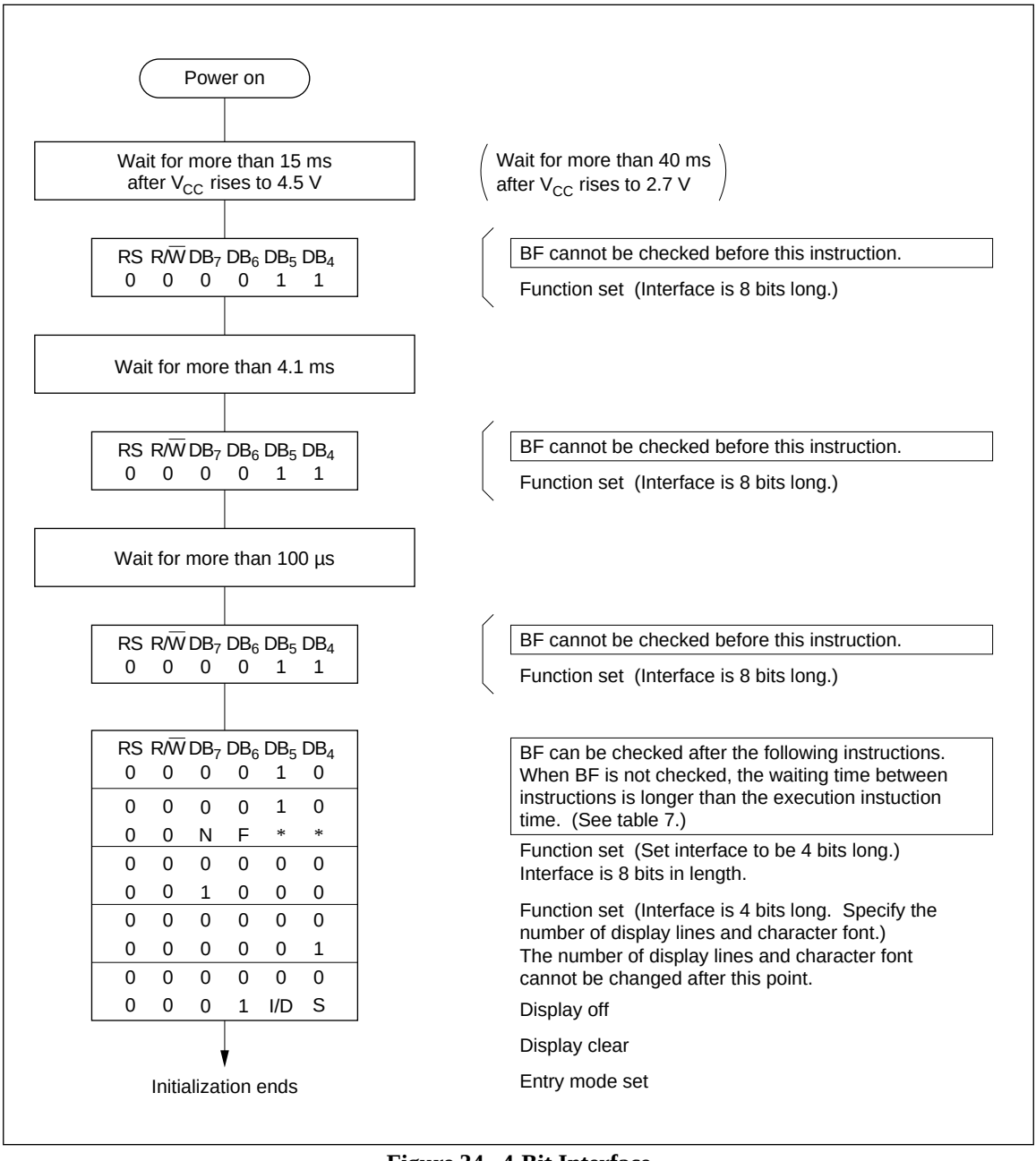


Figure 34 4-Bit Interface

[Low voltage version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +8.5	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.55	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$, D_0–D_7)	–Ip	10	50	120	µA	V_{CC} = 3 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	8.3	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	8.3	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.7 to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	240	320	390	kHz	R_f = 56 kΩ V_{CC} = 3 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	350		
Data hold time	t_{DHR}	10	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	200		

Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

[Standard Voltage Version]

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +8.5	2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability. Refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	2.2	—	V_{CC}	V		6, 17
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	0.6	V		6, 17
Input high voltage (2) (OSC_1)	V_{IH2}	V_{CC}–1.0	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	1.0	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	2.4	—	—	V	$–I_{OH}$ = 0.205 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.6 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	0.9 V_{CC}	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	0.1 V_{CC}	V	I_{OL} = 0.04 mA	8
Driver on resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	13
Driver on resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	13
Input leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RS, R/$\overline{W}$, D_0–D_7)	$–I_p$	50	125	250	µA	V_{CC} = 5 V	
Power supply current	I_{CC}	—	0.35	0.60	mA	R_f oscillation, external clock V_{CC} = 5 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	8.3	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	8.3	V	V_{CC}–V_5, 1/4 bias	16

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C[*3])

Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	t_{rcp}	—	—	0.2	µs		11
	External clock fall time	t_{fcp}	—	—	0.2	µs		11
R_f oscillation	Clock oscillation frequency	f_{OSC}	220	320	420	kHz	R_f = 68 kΩ V_{CC} = 5 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Bus Timing Characteristics

Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 35
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	320		
Data hold time	t_{DHR}	20	—	—		

Interface Timing Characteristics with External Driver

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 37
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

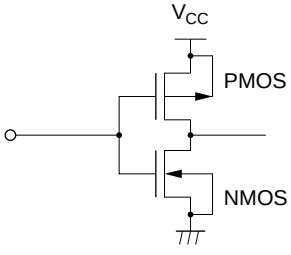
Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 38
Power supply off time	t_{OFF}	1	—	—		

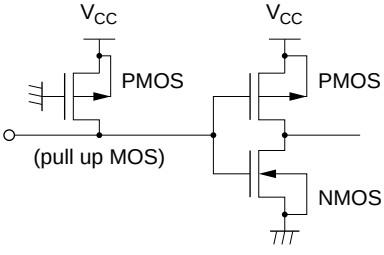
Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

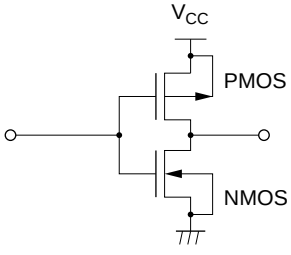
Input pin
Pin: E (MOS without pull-up)



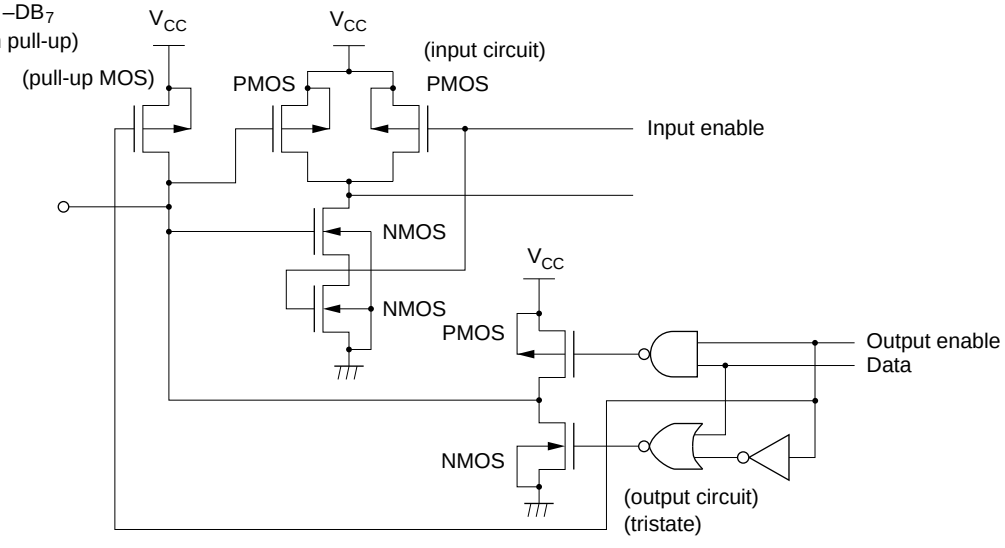
Pins: RS, R/$\overline{W}$ (MOS with pull-up)



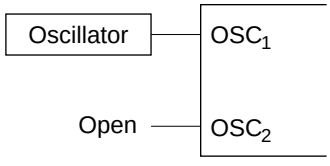
Output pin
Pins: CL_1, CL_2, M, D

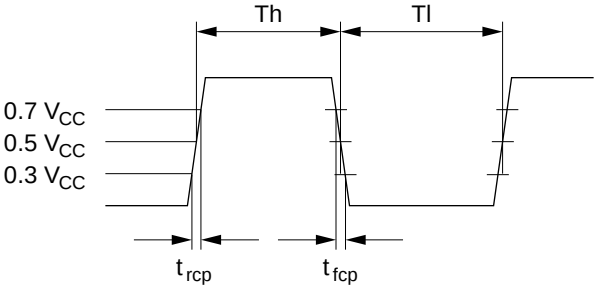


I/O Pin
Pins: DB_0–DB_7
(MOS with pull-up)



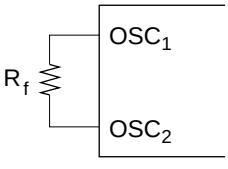
6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



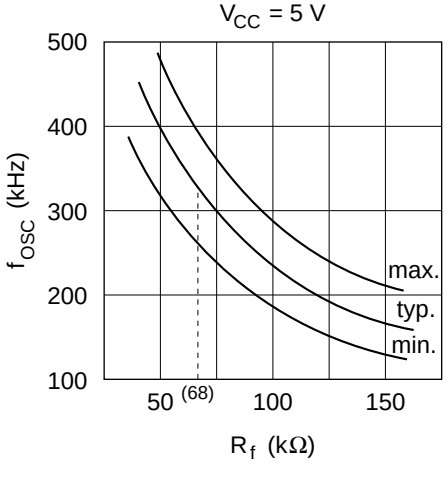


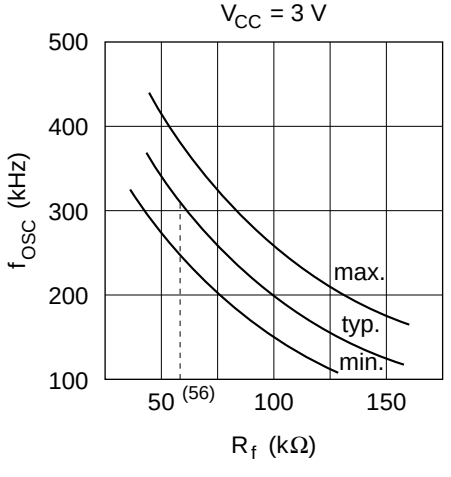
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor R_f.



R_f : 56 kΩ ± 2% (when V_{CC} = 3 V)
R_f : 68 kΩ ± 2% (when V_{CC} = 5 V)
Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.

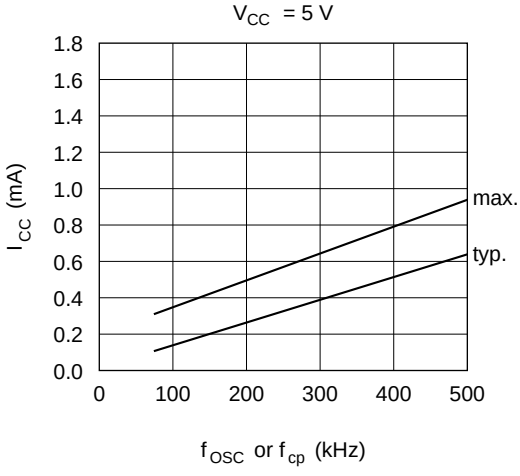


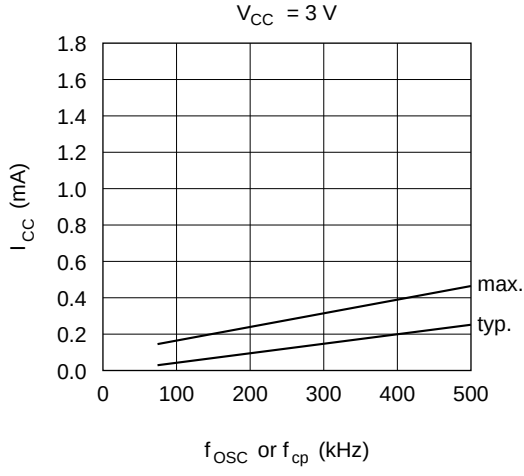


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_1 to COM_{16}).

    R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{100}).

14. The following graphs show the relationship between operation frequency and current consumption.

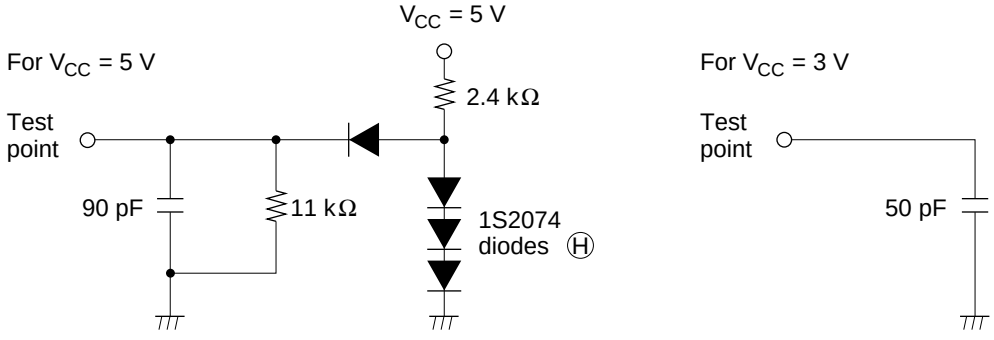




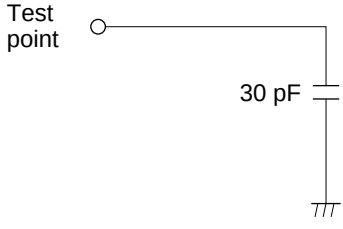
15. Applies to the OSC_1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.
17. The TEST pin should be fixed to GND and the EXT pin should be fixed to V_{CC} or GND.

Load Circuits

Data Bus DB_0 to DB_7



External Driver Control Signal: CL1, CL2, D, M



Timing Characteristics

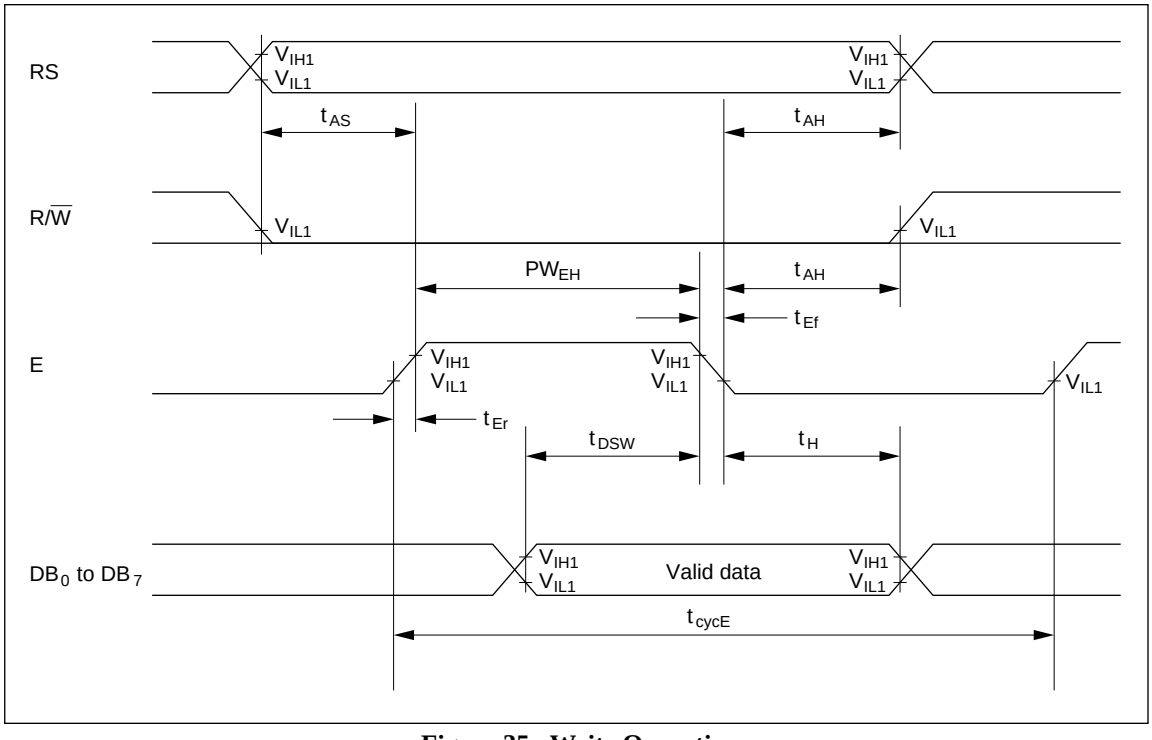


Figure 35 Write Operation

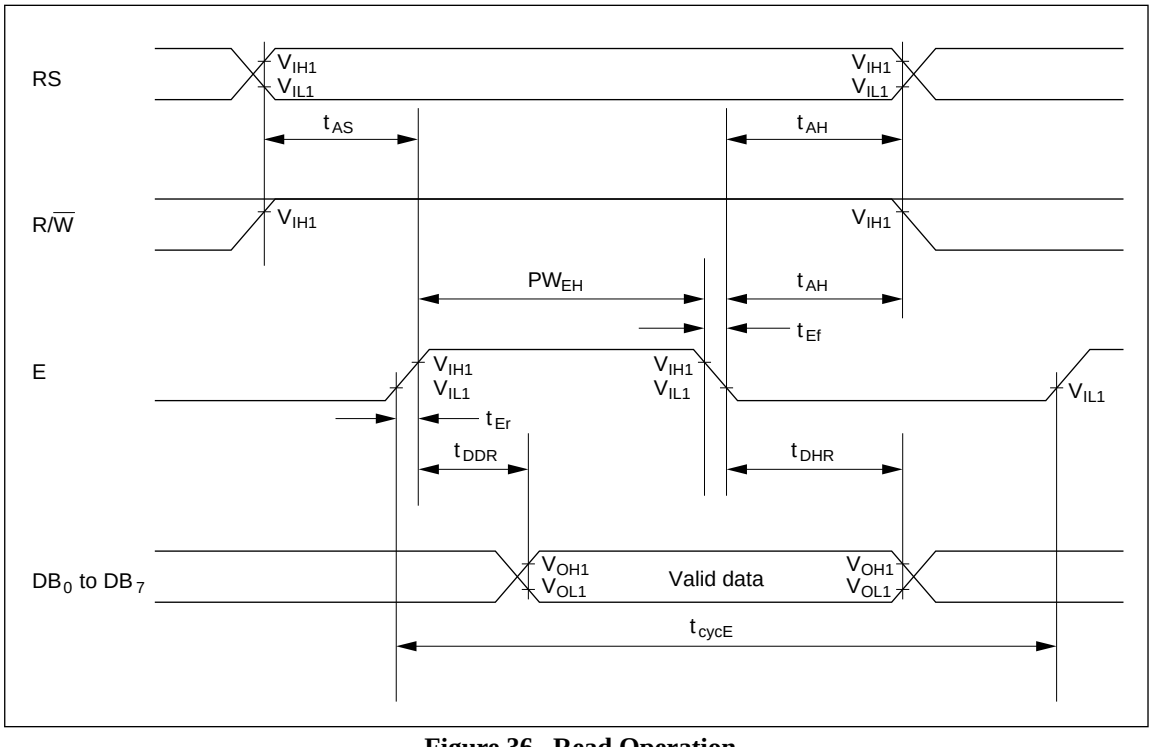


Figure 36 Read Operation

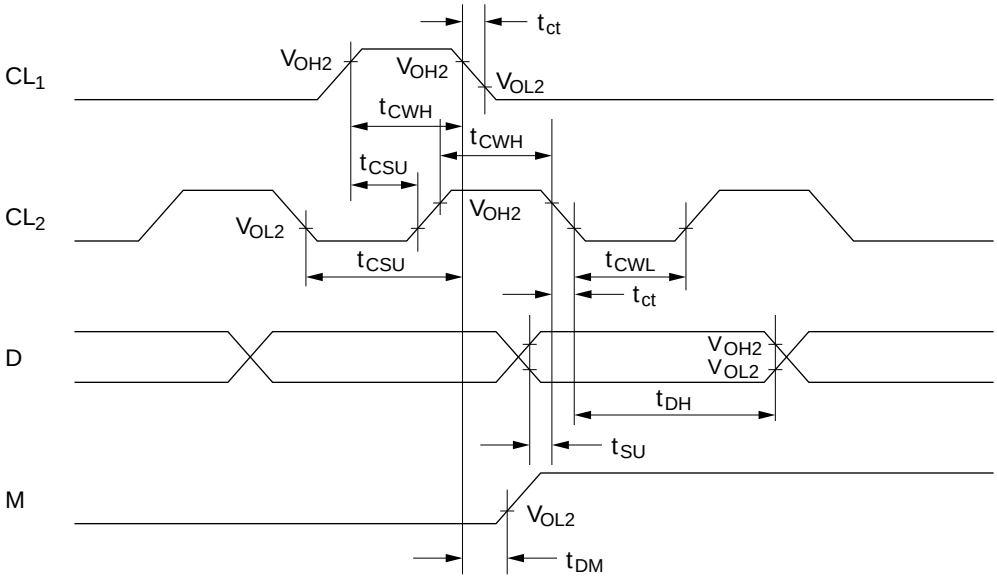
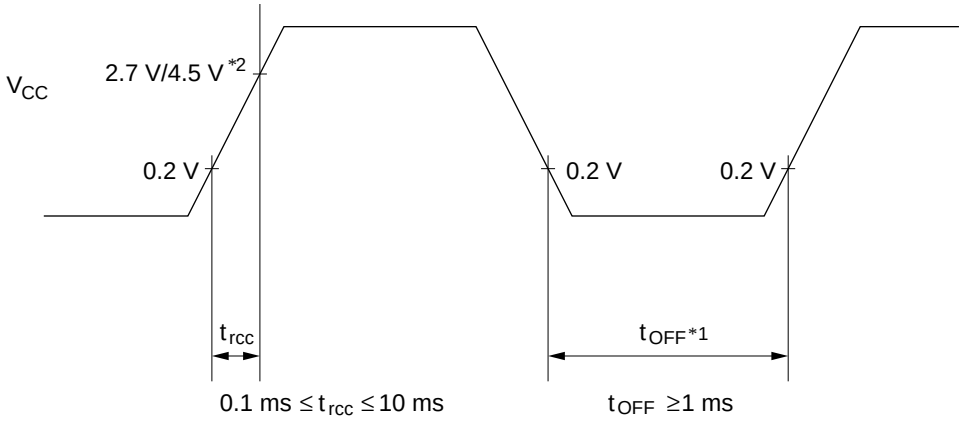


Figure 37 Interface Timing with External Driver



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. When the above condition cannot be satisfied, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 38 Internal Power Supply Reset