



PC Clock Generator

Features

- Generates up to 4 preset frequencies and buffers the reference frequency
- Requires only two external components: one 14.318 MHz crystal and one 0.1 μ F decoupling capacitor
- On-chip loop filter for clock generator
- Meets frequency requirements for x86 and Pentium™ CPUs
- Drop-in replacement for AV9107
- CMOS technology in 8-pin PDIP (300 mil) and SOIC (150 mil)
- 5V or 3.3V supply

Description

CH9007 is a PLL clock generator designed for personal computer applications, such as motherboards, graphics, and disk drives.

CH9007 generates a CPU clock from a preset ROM table and buffers the 14.318 MHz reference frequency. The CPU output frequencies are selected by the frequency select inputs, FS[1:0].

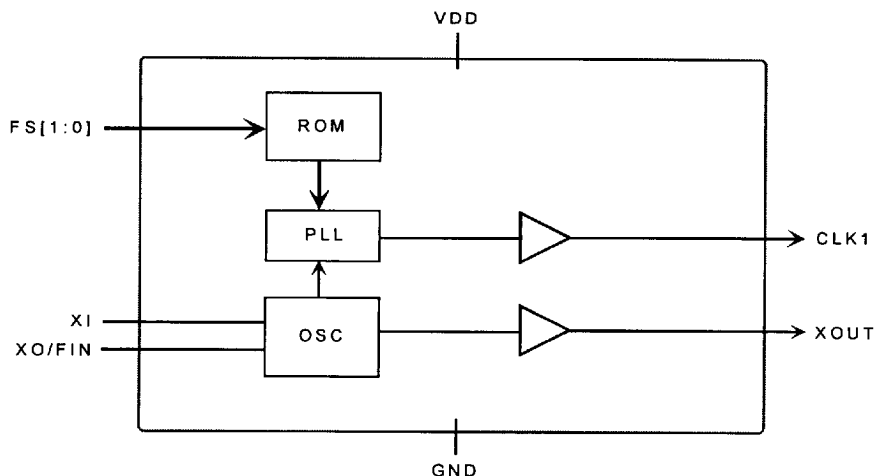


Figure 1: Block Diagram

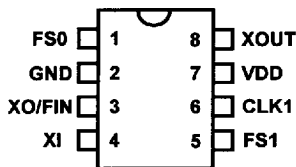


Figure 2: CH9007A and C

Table 1 • Pin Description CH9007A and C

Pin	Type	Symbol	Description
1, 5	In	FS0, FS1	Frequency select for CLK1 (no internal pull-up or pull-down)
2	Power	GND	Ground
3	Out / In	XO / FIN	Crystal output or external FREF input
4	In	XI	Crystal input
6	Out	CLK1	Clock1 output
7	Power	VDD	5V or 3.3V supply
8	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 2 • Frequencies for CH9007A and C (in MHz)

Frequency Select Inputs		Version A	Version C
FS1	FS0	CLK1	CLK1
0	0	40.0	25.0
0	1	50.0	33.3
1	0	66.6	40.0
1	1	80.0	50.0

Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	-0.5 to +7.0	V
VIN	Input voltage on any pin with respect to GND	-0.5 to VDD+0.5	V
TSTOR	Storage temperature	-55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: $T_A = 0^\circ\text{C} - 70^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @ $T_A = 25^\circ\text{C}$	Min	Typ	Max	Unit
VOH	Output high voltage	$V_{DD} = 4.75V$, $I_{OH} = 4mA$	2.4			V
VOL	Output low voltage	$V_{DD} = 4.75V$, $I_{OL} = 8mA$			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	μA
ILK	Input leakage current		-10		10	μA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD	Operating current	$V_{DD} = 5V$ CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		10 20		mA

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Table 5 • AC Specifications (Operating Conditions: $T_A = 0^\circ\text{C} - 70^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @ $T_A = 25^\circ\text{C}$	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	32	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, $V_{OUT} = 0.8V$ to $2.0V$			3	ns
TF	Output clock fall time	15 pF load, $V_{OUT} = 0.8V$ to $2.0V$			3	ns
TDC	Duty cycle	15 pF load	45	48/52	55	%
TJCC	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
TJLT	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		150	800	ps
TFT	Frequency transition time	8 - 80 MHz		10		ms
TPU	Power up time	From OFF to 100 MHz		15		ms

Table 6 • DC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
VOH	Output high voltage	$V_{DD} = 3.0\text{V}$, $I_{OH} = 1\text{mA}$	$V_{DD} - 0.5$			V
VOL	Output low voltage	$V_{DD} = 3.0\text{V}$, $I_{OL} = 2\text{mA}$			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
I _{PU}	Input pull-up current			3	10	μA
I _{LK}	Input leakage current		-10		10	μA
C _I	Input capacitance	Except XO / FIN, XI			10	pF
C _I	Input capacitance	Pins XO / FIN, XI		20		pF
I _{DD}	Operating current	$V_{DD} = 3.3\text{V}$ CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		5 10		mA

Table 7 • AC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
T _{IR}	Input clock rise time				20	ns
T _{IF}	Input clock fall time				20	ns
T _R	Output clock rise time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
T _F	Output clock fall time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
T _{DC}	Duty cycle	15 pF load	45	48/52	55	%
T _{JCC}	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
T _{JLT}	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		200	1000	ps
T _{FT}	Frequency transition time	8 – 80 MHz		10		ms
T _{PU}	Power up time	From OFF to 100 MHz		15		ms

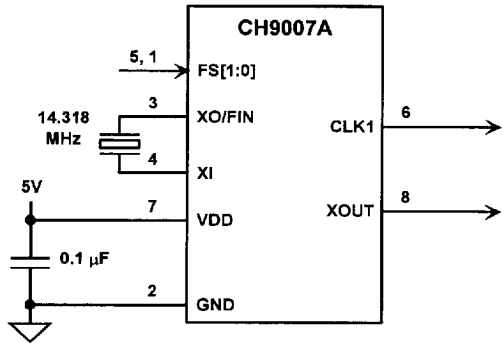


Figure 3: Application Schematic

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9007x-N	300 mil PDIP	8	5V
CH9007x-S	150 mil SOIC	8	5V
CH9007x-N-L	300 mil PDIP	8	3.3V
CH9007x-S-L	150 mil SOIC	8	3.3V
Note: x = frequency table version			