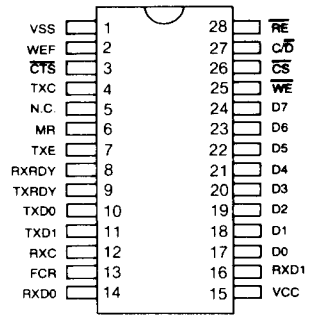
WD1993 Arinc 429 Receiver/Transmitter and Multi-Character Receiver/Transmitter

FINAL

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- TEMPERATURE RANGES 0°C to 70°C, — 1993-03, −40°C to +85°C — 1993-02, −55°C to +125°C — 1993-01



PIN DESIGNATION

DESCRIPTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol.

Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.

PIN DESCRIPTION

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	WEF *	WORD ERROR FLAG	This pin is an output, which when active indicates an error in either the transmitter or receiver has been detected. It reflects an underrun, overrun, parity or framing (receive word) error and is intended as an error interrupt. The Status Register should be read to determine the specific error.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ARINC MODE = 4 × bit rate
5	EGND	EXTERNAL GROUND	Requires external ground for proper operation.
6	MR	MASTER RESET	When active (V_{IH}), presets the WD1993 mode and command registers to the ARINC protocol. Master Reset also resets the data registers and places the WD1993 transmitter and receiver into idle states. After MR, the command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1993. RXRDY is enabled unless inhibited by setting command bit CR3 (RXRDYIN) to a logic "1." It is automatically enabled again after a receive sequence is completed.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1993 and can be used as an interrupt to the system.
10	TXD0	TRANSMIT DATA ZERO	This output drives the V/Z circuit when a logic zero is to be transmitted and is active for one-half bit time.
11	TXD1	TRANSMIT DATA ONE	This output drives the V/Z circuit when a logic one is to be transmitted and is active for one-half bit time.

* The following operation must be performed to clear the error in the Status Register and de-assert the Word Error Flag
1. Perform a Master Reset (MR) or;
2. Transfer a new character to the Receiver Holding Register after a reload of the Receiver Register.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR	FIRST CHARACTER READY	This output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	RXD0	RECEIVE DATA ZERO	RXD0 is driven by the line V/Z receiver circuit. When the V/Z circuit detects a logic zero, a TTL logic one (active for one-half bit time) is provided to the WD1993.
15	VCC	POWER SUPPLY	+ 5V DC
16	RXD1	RECEIVE DATA ONE	The RXD1 input is driven by the V/Z line receiver. Each time the V/Z circuit detects a logic one, a TTL level logic one (active for one-half bit time) is provided to this input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1993 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
25	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	When active (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	$\overline{CHIP\ SELECT}$	When active (V_{IL}), the device is selected. This enables communication between the WD1993 and a microprocessor.
27	C/$\overline{D}$	CONTROL/$\overline{DATA}$	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	$\overline{READ\ ENABLE}$	When active (V_{IL}), allows the CPU to read data or status information from the WD1993.

ARCHITECTURE

A block diagram of the WD1993 is shown in Figure 1.

As mentioned, the WD1993 is an eight bit bus-oriented device. Communication between the WD1993 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1993 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$), and Control or Data Select (C/$\overline{D}$).

Internal control of the WD1993 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol, along with the programmable multicharacter capabilities.

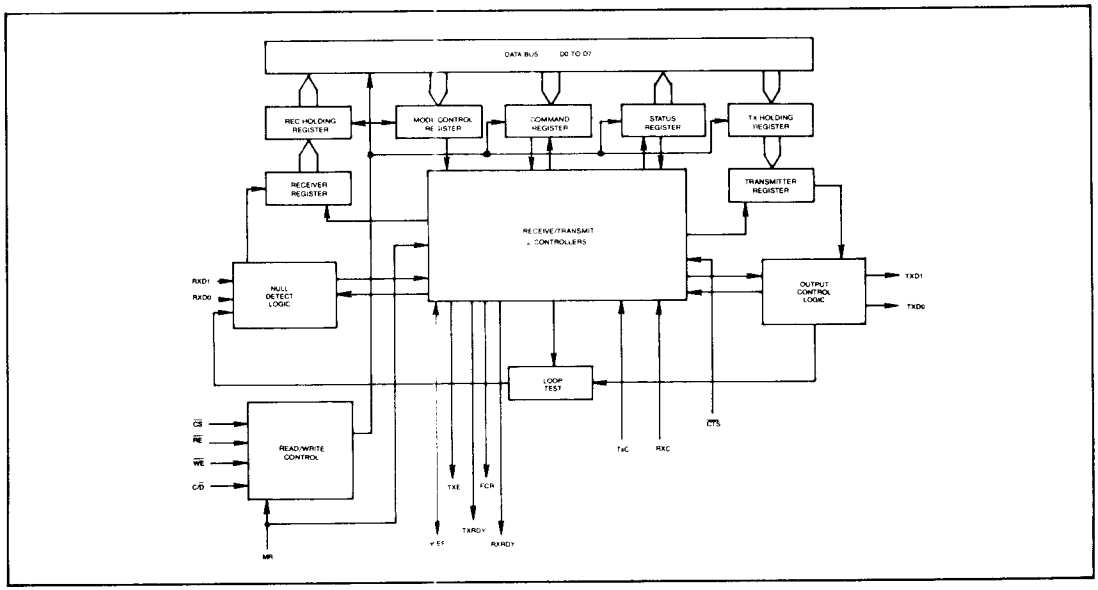


FIGURE 1. WD1993 BLOCK DIAGRAM

OPERATION

Upon master reset (MR), the device is programmed to transmit and receive four 8-bit contiguous characters with the 32nd bit inside odd parity. (ARINC protocol.)

A minimum four bit time space is automatically inserted after the character transmission. Two receiver inputs, RXD1/RXD0 and two transmitter outputs, TXD1/TXD0, are provided to interface with voltage—impedance (V/Z) circuits to translate ±10 volt ARINC line levels to 5 volt TTL logic levels. The transmit clock (TXC) and receive clock (RXC), in ARINC mode, are four times (4X) the bit rate desired.

The receiver monitors the received data input to detect a four bit time null, which delimits the word. If the communications link is broken during a word reception, the receiver will generate a word error flag to (WEF) to notify the CPU to request retransmission. When a null is detected, the receiver logic is reset and returned to an idle state awaiting the next word.

The Command Register is used to select features such as parity options, loop test capability, RXRDY flag enabling, transmitter and receiver enabling, and may also cause the WD1993 to return to the Mode instruction.

The Status Register contains information such as Transmitter Ready, Transmitter Empty, Receiver Ready, error conditions, and First Character Ready.

OPERATING DESCRIPTION

The WD1993 is primarily designed to operate in an 8 bit micro-processor environment. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and C/$\overline{D}$) should be connected to the microprocessor's data bus and system control bus.

The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a WD1943. A master reset pulse initializes the WD1993 and presets the control registers to the ARINC protocol.

The RXD1/RXD0 inputs are interfaced to the DITS data line via external level translators that provide TTL (5V) logic levels to the WD1993. The TXD1/TXD0 outputs are connected to high voltage (± 10V) driver circuits. Figures 16 and 17 show some typical ± 10V translator and driver circuits.

The TXRDY, RXRDY, FCR and WEF Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support WD1993 operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1993 is designed such that a control register write operation accesses the command instruction register.

The RXRDYIN bit of the command register is used to inhibit the RXRDY output pin for ARINC operations.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) When the Transmitter Holding Register has transferred its contents to the Transmitter Register for the character to be transmitted, it will activate the TXRDY (pin 9) output, to alert the CPU that the next 8-bit character can be accepted. When this new character is loaded into the Transmitter Holding Register (while the Transmitter Register is still transmitting its contents, thereby preventing the Transmitter Holding Register to transfer its character contiguously), TXRDY is not deactivated (reset low to a logic zero) when WRITE ENABLE ($\overline{WE}$) is deactivated (set high to a logic one), as shown by the dotted line in Figure 2. An underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

However, the WD1993 will delay the deactivation of TXRDY until the end of the fourth clock or the end of a data bit being transmitted (see Figure 2).

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the Receiver Register.

d) When the first character is completely assembled in the Receiver Register, the data is loaded into the Receive Holding Register and the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active. The CPU should read the data in the Receiver Holding Register to reset the FCR and first RXRDY. If the Arinc 429 character is accepted, three more RXRDY's will be generated for the three remaining bytes of this character, i.e., every time a byte is transferred from the Receiver Register to the Receiver Holding Register (see Figure 3, Data Accepted). The CPU should read the data prior to the reception of the next character (next RXRDY) or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

The first character in the Arinc protocol contains a label. The FCR and RXRDY Flags become active to indicate the reception of the first character of data. The CPU reads the first character and decides whether or not it wants to acquire the subsequent characters. If not, then the CPU performs a "control write" to the Command Register, setting the RXRDYIN (CR3) bit to a "1." This bit in Arinc mode should inhibit the RXRDY flag from interrupting the CPU during the reception of the 3 remaining characters. The RXRDYIN bit is then automatically reset upon completion of the receive sequence and RXRDY is enabled again (see Figure 3, Conforming Data Rejection).

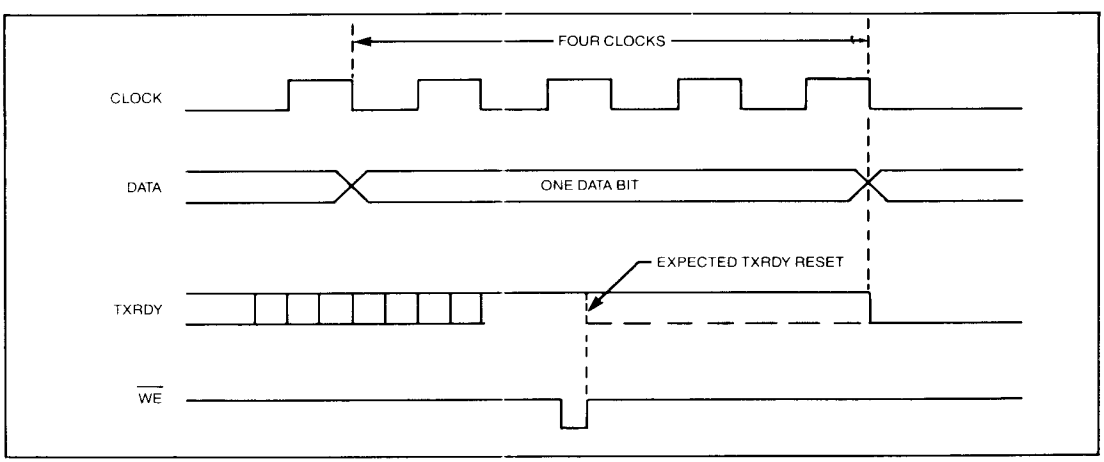


FIGURE 2

The WD1993 however generates a RXRDY after the null character (see Note), thereby conceivably misleading the CPU that a first 8 bit character (label) of the following 32 bit ARINC 429 character, has been assembled in the Receiver Register and transferred to the Receiver Holding Register, ready to be read (see Figure 3, "WD1993 Data Rejection").

A solution to overcome this misreading, is to gate (AND) the FCR and RXRDY outputs to interpret this combination as a valid RXRDY for the Label.

NOTE: A NULL character is the four bit (all zero's) character which is used in the ARINC 429 protocol to synchronize, differentiate and signify the start of the 32 bit ARINC 429 characters.

LOOP TEST MODE

As mentioned, the WD1993 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and $\overline{CTS}$ should be "V_{IL}". The receiver inputs are ignored and the transmitter outputs are sending nulls. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

For basic testing, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ARINC BACKGROUND

Aeronautical Radio Inc. (ARINC) publishes the ARINC 429 specification. This document defines the air transport industries standards for the transfer of digital data between avionics systems elements. This specification was adopted by The Airlines Electronic Engineering Committee April 11, 1978. By the adoption of this specification the foundation is set for a standard protocol governing all intersystems equipment (Line Replaceable Units).

MARK 33 DIGITAL INFORMATION TRANSFER SYSTEM (DITS)

Basic Philosophy

Transmit from a designated output port over a single twisted and shielded pair of wires to designated receiver.

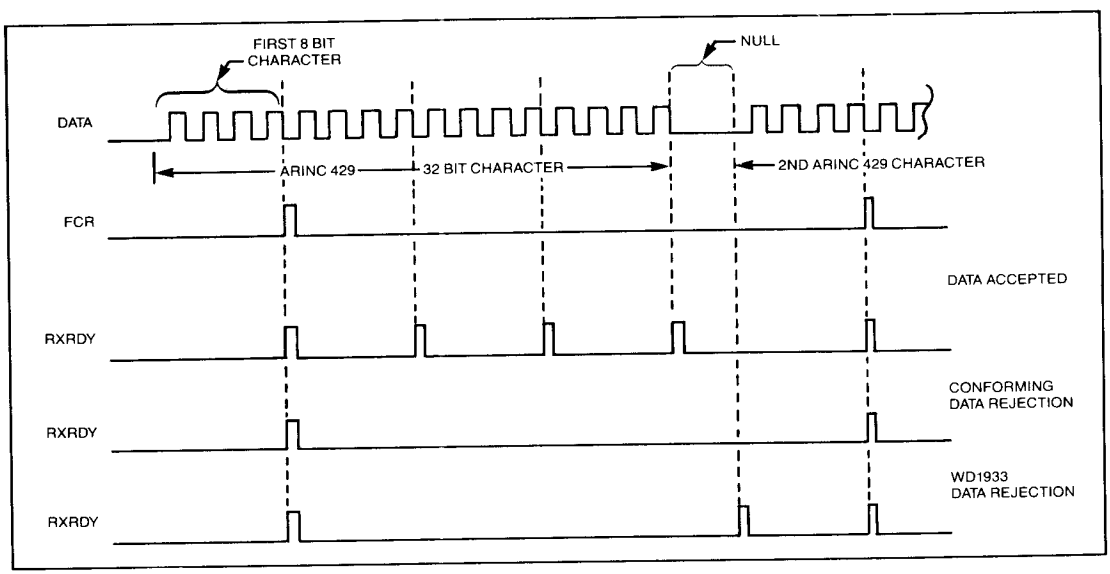


FIGURE 3

Bidirectional data flow not permitted on a given pair.

Data Transfer
- Numeric
- Iso Alphabet #5
- Graphic

Data Format
- 32 bits or less (unused bit positions should be filled with binary zeros or valid data pad bits).
- Bit #32 is assigned to parity.

Modulation
- Return to Zero (RZ)

Transmit Voltage Levels

high	+10	±0.5V
null	0	±0.5V
low	−10	±0.5V

Receiver Voltage Levels:

	(in absence of noise)	(noisy environment)
high	+6.0V to +10V	+5.0V to +13V
low	−6.0V to +10V	−5.0V to −13V

No damage to receiver up to 20 vac rms between A & B; +28, A to Gnd; −28, B to Gnd.

Data Rate
- 100 kilo bit per second ± 1%
- Low speed 12 to 14.5 kilo bit per second ± 1%

Word Synchronization
- All zero gap of a minimum of 4 bit times

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
NA	IR	NA	LTE	RXRDYIN	REN	NA	TEN

TEN	Transmit ENable
1	Enabled
0	Disabled

NA	Not Used

REN	Receive ENable
1	Enabled
0	Disabled

RXRDYIN	RXRDY Inhibit
1	Inhibit RXRDY output flag
0	Normal transmitter operation enable RXRDY output flag

LTE	Loop Test ENable
1	Local loop-back mode
0	Normal Operation

NA	Not Used

IR	Internal Reset
1	Returns WD1993 to mode instruction format
0	Stays in Command Register

NA	Not Used

The WD1993 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Command Register
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	FCR	WEF	OE	PE	TXE	RXRDY	TXRDY

TXRDY — Transmitter Ready
1 — Active (THR can be reloaded)
0 — Inactive (transmitter is busy)

RXRDY — Receiver Ready
1 — Active (RHR should be read)
0 — Inactive

TXE — Transmitter Empty
1 — Transmitter idle
0 — Transmitter active

PE — Parity Error
1 — Parity Error reported
0 — No error

OE — Overrun Error
1 — RHR has been written over with a new character before previous character was read.
0 — No error

FE — Framing Error
1 — Indicates improper receive sequence detected.
0 — No error

FCR — First Character Ready
1 — This bit indicates the receiver has just completed assembly of the 1st character in a multi-character sequence and that the data is contained in the RHR.
0 — First character not ready.

UE — Underrun Error
1 — Indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0 — No error

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −55°C to +125°C (Plastic Package)
−65°C to +150°C (Ceramic Package)
Voltage on any Pin with Respect to Ground . −0.3V to +7V
Power Dissipation ..... 400 MW
Lead Temperature (soldering 10 sec) ..... 300 °C

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			50	uA	Data Bus is in High Impedence State
				10	uA	
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	V_{CC} = 5.25V No Load

CAPACITANCE

T_A = 25°C; V_{CC} = GND = ØV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

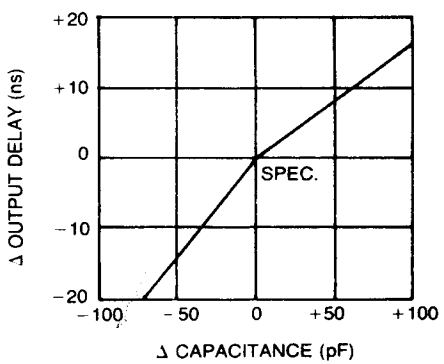


FIGURE 4. OUTPUT DELAY vs CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS					
Read Cycle	**(Reference Figure 6)**				
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50 pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50 pF
		25		ns	C_L = 15 pF
WRITE CYCLE	**(Reference Figure 7)**				
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
OTHER TIMINGS	**(Reference Figures 8-12)**				
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency	DC	800	KHz	
t_{RX}	Receiver Input Clock Frequency	DC	800	KHz	
t_{DTY}	TXRDY Delay from $\overline{WE}$	200ns	2 Clock Periods		
t_{DRY}	RXRDY Delay from Center of Last Data Bit (FCR Delay from Center of Data Bit)		½ Clock Period		
t_{DTE}	TXE Delay from TXRDY		½ Clock Period		

FIGURE 5. TEST POINTS FOR A.C. TIMING

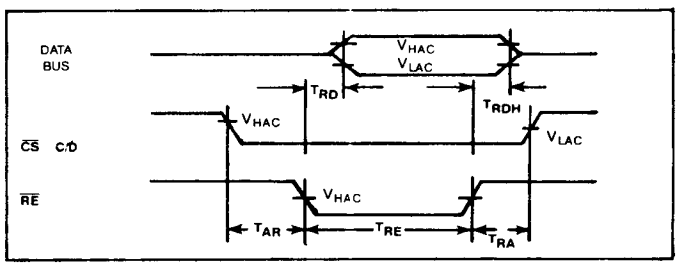


FIGURE 6. READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V and with test load circuit.

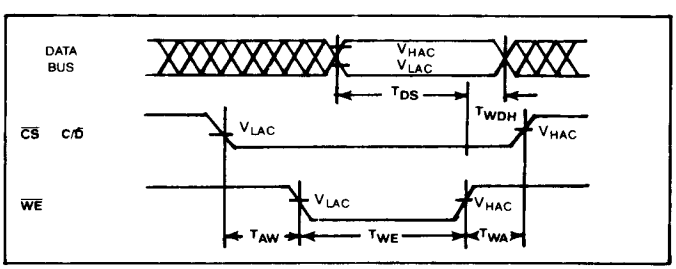


FIGURE 7. WRITE CYCLE TIMING

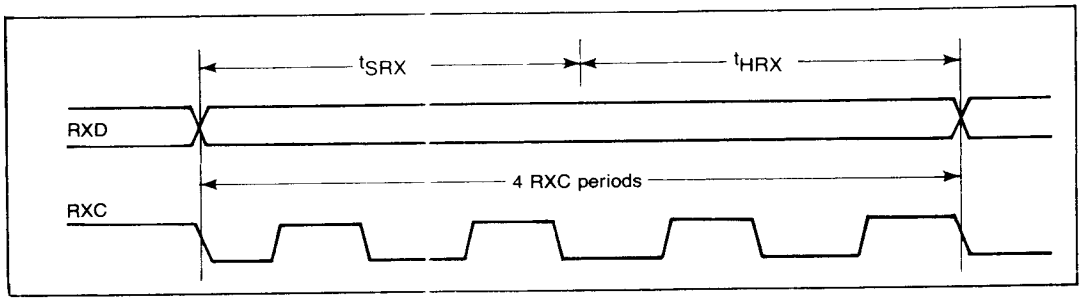


FIGURE 8. RECEIVER CLOCK AND DATA TIMINGS

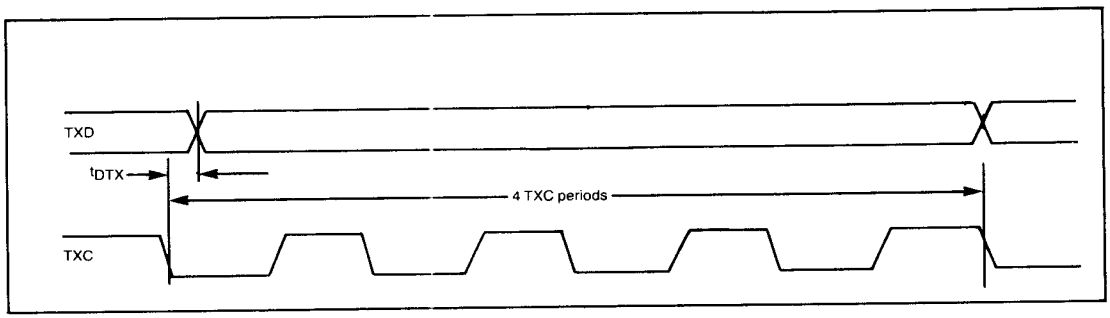


FIGURE 9. TRANSMITTER CLOCK AND DATA TIMINGS

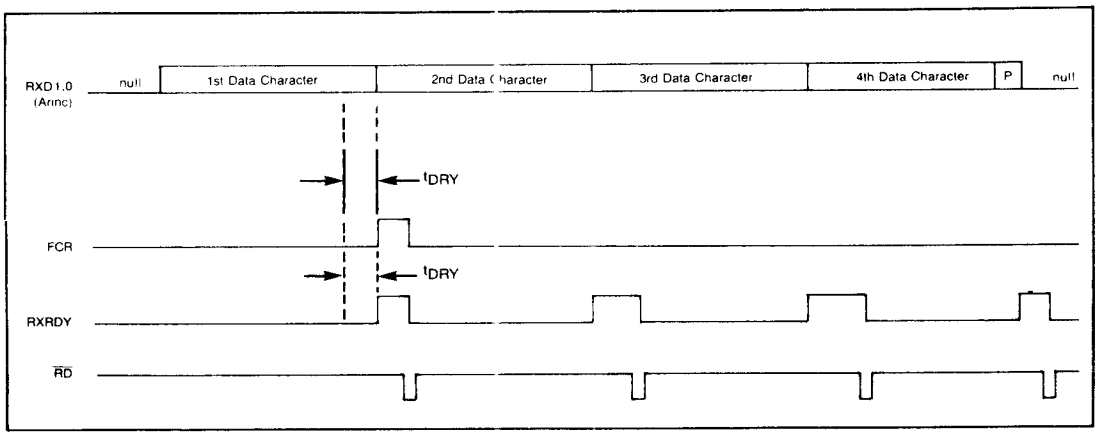


FIGURE 10. RXRDY AND FCR TIMING

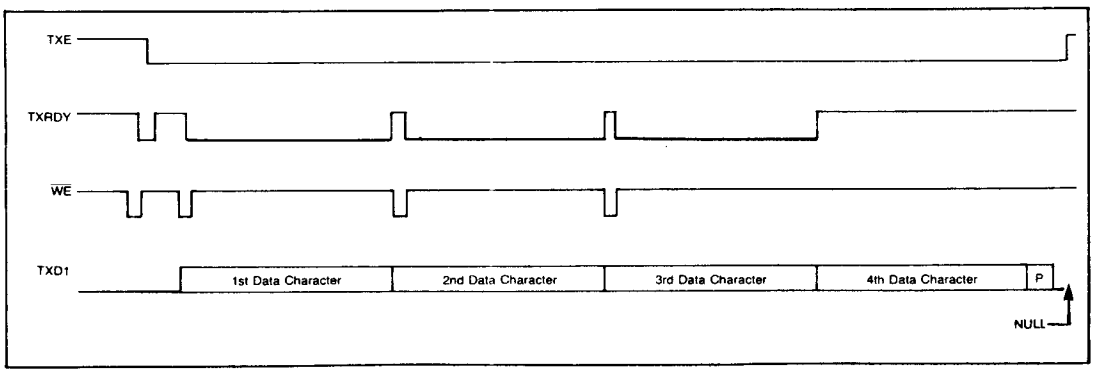


FIGURE 11. RXRDY AND TXE TIMINGS (4 Character Sequence)

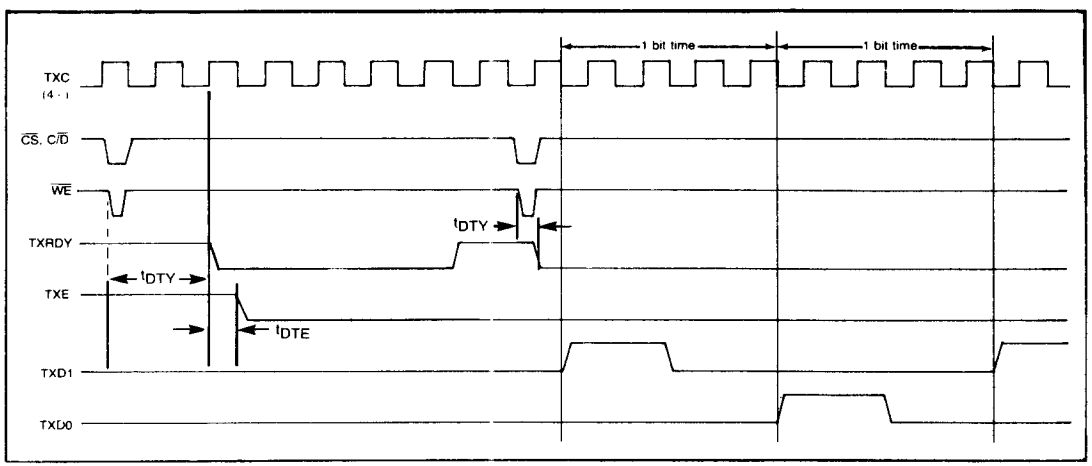


FIGURE 12. TRANSMITTER TIMINGS (ARINC MODE)

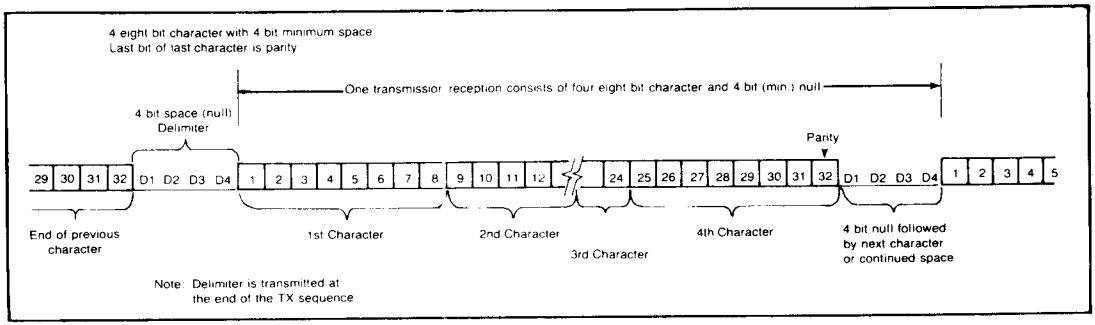


FIGURE 12. ARINC 429

The V/Z Receiver converts ±10 volt levels to TTL logic levels. It is composed of logic one and zero comparators. A logic one (RXD1) TTL output is derived when voltage rising to 1 (VR1) threshold is crossed and terminated at voltage falling to 1 (VF1). A logic zero (RXD0) TTL output is generated between voltage falling to zero (VFO) and voltage rising from zero (VRO). When input thresholds are not exceeded, neither output is active. The V/Z output can drive one TTL input.

The return to zero (RZ) format is shown below

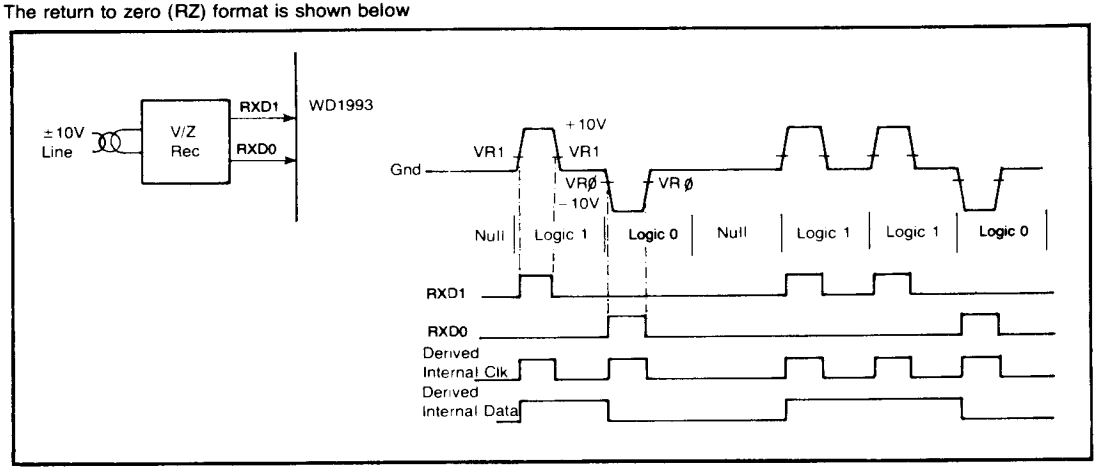


FIGURE 13. ARINC RECEIVER CIRCUIT

The V/Z Driver convert TTL logic levels into ± 10 volt levels. The TXD1 and TXD0 outputs of the WD1993 are used to drive the line drivers. Each output can drive one TTL load. When the outputs are not active, the line Driver should return to zero.

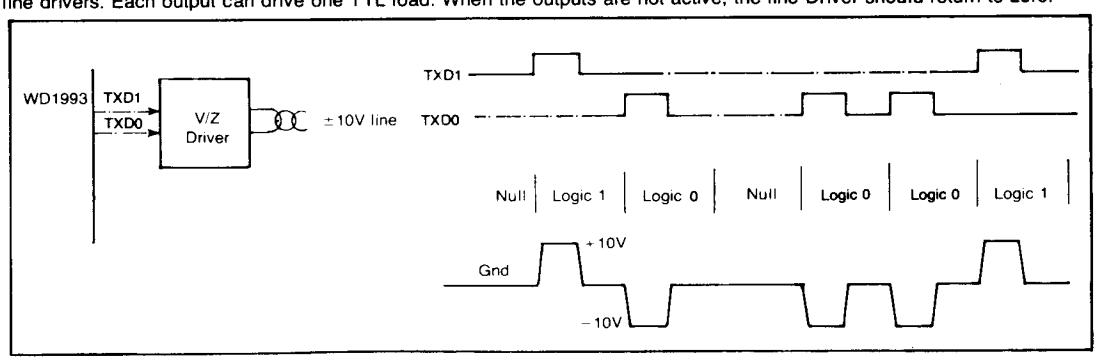


FIGURE 14. ARINC DRIVER CIRCUIT

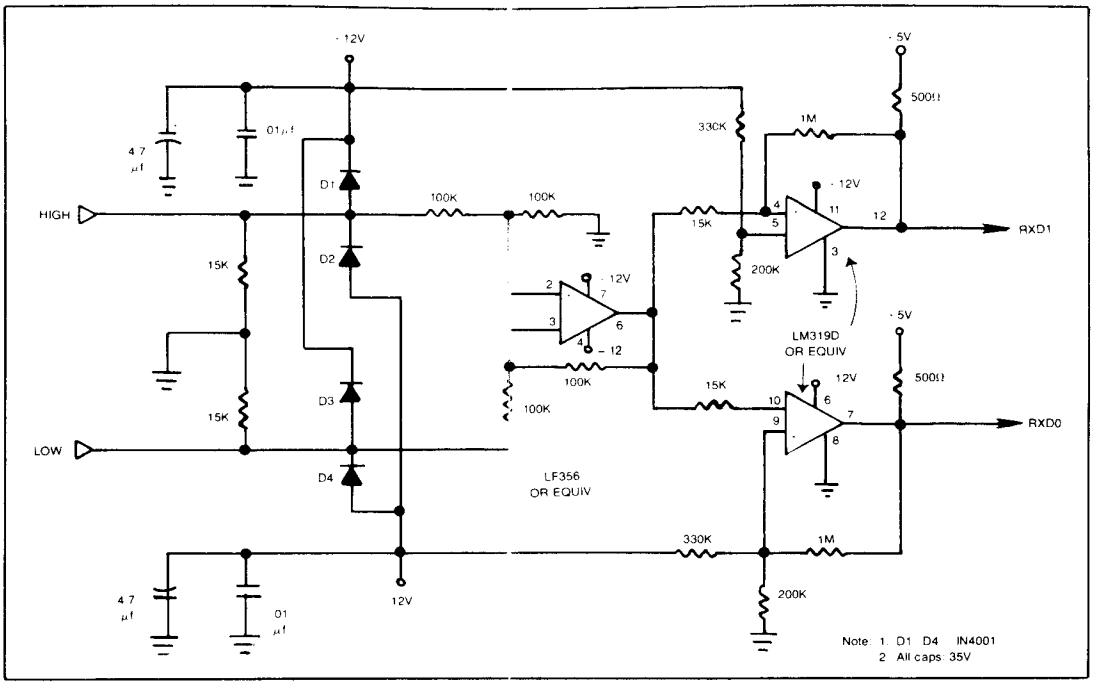


FIGURE 15. ARINC 429 LINE LEVEL TRANSLATOR (RECEIVER)

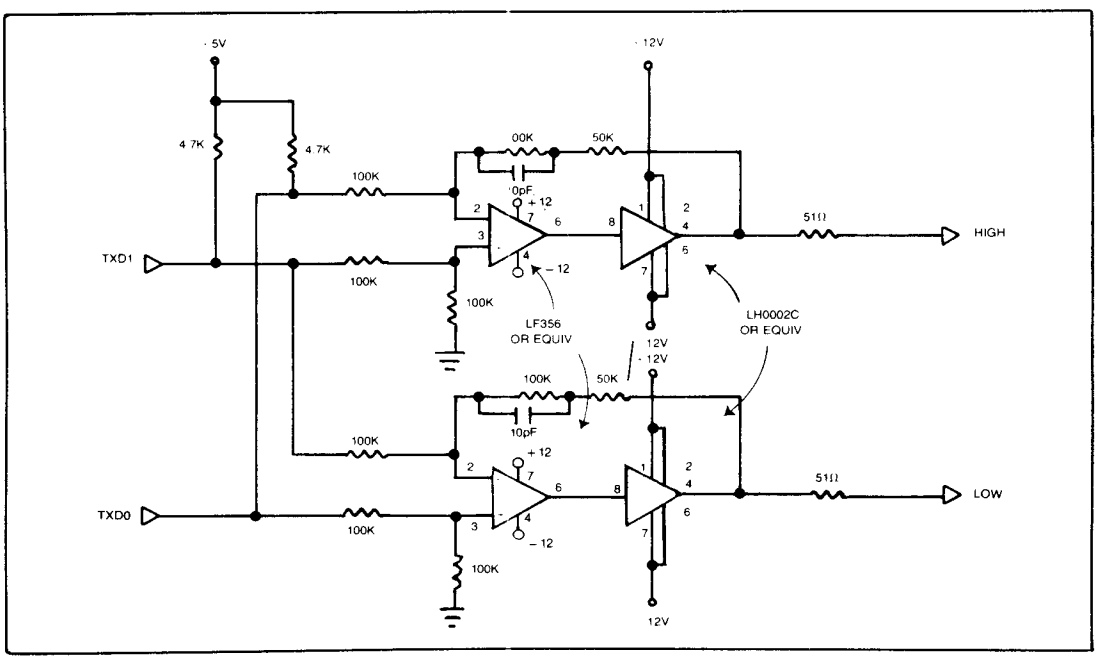


FIGURE 16. ARINC 429-1 LINE DRIVER