

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

D2434, OCTOBER 1980 - REVISED SEPTEMBER 1986

- AM26LS32A Meets EIA Standards RS-422-A and RS-423-A
- AM26LS32A Has $\pm 7\text{-V}$ Common-Mode Range With $\pm 200\text{-mV}$ Sensitivity
- AM26LS33A Has $\pm 15\text{-V}$ Common-Mode Range With $\pm 500\text{ mV}$ Sensitivity
- Input Hysteresis . . . 50 mV Typical
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- Complementary Output Enable Inputs
- Input Impedance . . . 12 k Ω Min
- Designed to Be Interchangeable With Advanced Micro Devices AM26LS32C and AM26LS33C

description

The AM26LS32A and AM26LS33A are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

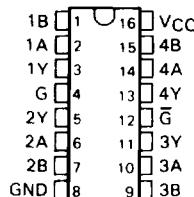
Compared to the AM26LS32C and the AM26LS33C, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and the AM26LS33AM are characterized for operation over the full military temperature range of -55°C to 125°C.

AM26LS32AC, AM26LS33AC . . . D, J, OR N PACKAGE

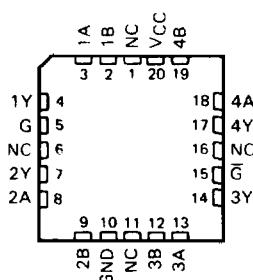
AM26LS32AM, AM26LS33AM . . . J PACKAGE

(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE

(TOP VIEW)



NC = No internal connection

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES G \bar{G}	OUTPUT
$V_{ID} \geq V_{TH}$	H X	H
	X L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H X	?
	X L	?
$V_{ID} \leq V_{TL}$	H X	L
	X L	L
X	L H	Z

H = high level, L = low level, X = irrelevant

Z = high impedance (off), ? = indeterminate

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

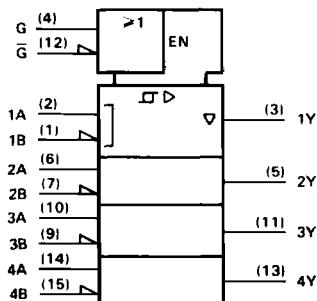
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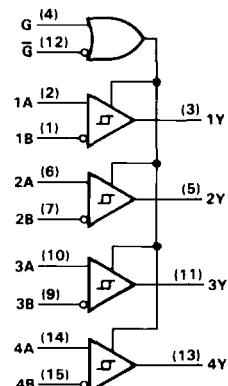
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QUADRUPLE DIFFERENTIAL LINE RECEIVERS

logic symbol[†]

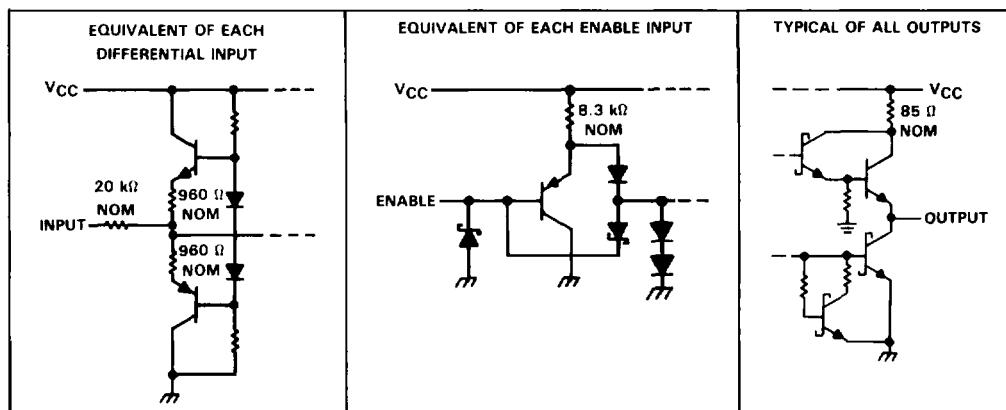


logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, any differential input	± 25	± 25	V
Differential input voltage (see Note 2)	± 25	± 25	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free air temperature range	0 to 70	-55 to 125	°C
Storage temperature range	-65 to 150	-65 to 150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D or N package	260	°C
Case temperature for 60 seconds	FK package	260	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J package	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.

2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ C$	DERATING FACTOR ABOVE $T_A = 25^\circ C$	$T_A = 70^\circ C$	$T_A = 125^\circ C$
	POWER RATING		POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (C-SUFFIX)	1025 mW	8.2 mW/°C	656 mW	—
J (M-SUFFIX)	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM AM26LS33AC, AM26LS33AM			± 7			± 7	V
High-level output current, I_{OH}				-440			-440	μA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0	70	-55	125			°C



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electrical characteristics over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{TH} Differential input high-threshold voltage	$V_O = V_{O\text{Hmin}}$, $I_{OH} = -440 \mu\text{A}$	AM26LS32A	0.2	0.5	V
		AM26LS33A			
V_{TL} Differential input low-threshold voltage	$V_O = 0.45 \text{ V}$, $I_{OL} = 8 \text{ mA}$	AM26LS32A	-0.2 [‡]	-0.5 [‡]	V
		AM26LS33A			
V_{Hys} Hysteresis, $V_{T+} - V_{T-}$ [§]			50		mV
V_{IK} Enable input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = 1 \text{ V}$,	'32AC, '33AC	2.7		V
	$V_{I(O)} = 0.8 \text{ V}$, $I_{OH} = -440 \mu\text{A}$	'32AM, '33AM	2.5		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = -1 \text{ V}$,	$I_{OL} = 4 \text{ mA}$	0.4		V
	$V_{I(O)} = 0.8 \text{ V}$	$I_{OL} = 8 \text{ mA}$	0.45		
I_{OZ} Off-state (high-impedance-state) output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$	20		μA
		$V_O = 0.4 \text{ V}$	-20		
I_I Line input current	$V_I = 15 \text{ V}$, Other input at -10 V to 15 V		1.2		mA
	$V_I = -15 \text{ V}$, Other input at -15 V to 10 V		1.7		
I_{IEN} Enable input current	$V_I = 5.5 \text{ V}$		100		μA
I_{IH} High-level enable current	$V_I = 2.7 \text{ V}$		20		μA
I_{IL} Low-level enable current	$V_I = 0.4 \text{ V}$		0.36		mA
r_i Input resistance	$V_{IC} = -15 \text{ V}$ to 15 V, One input to AC ground	12	15		k Ω
I_{OS} Short-circuit output current [¶]	$V_{CC} = \text{MAX}$	-15	-85		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All outputs disabled	52	70		mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, and $V_{IC} = 0$.

[‡]The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} . See Figures 10 and 11.

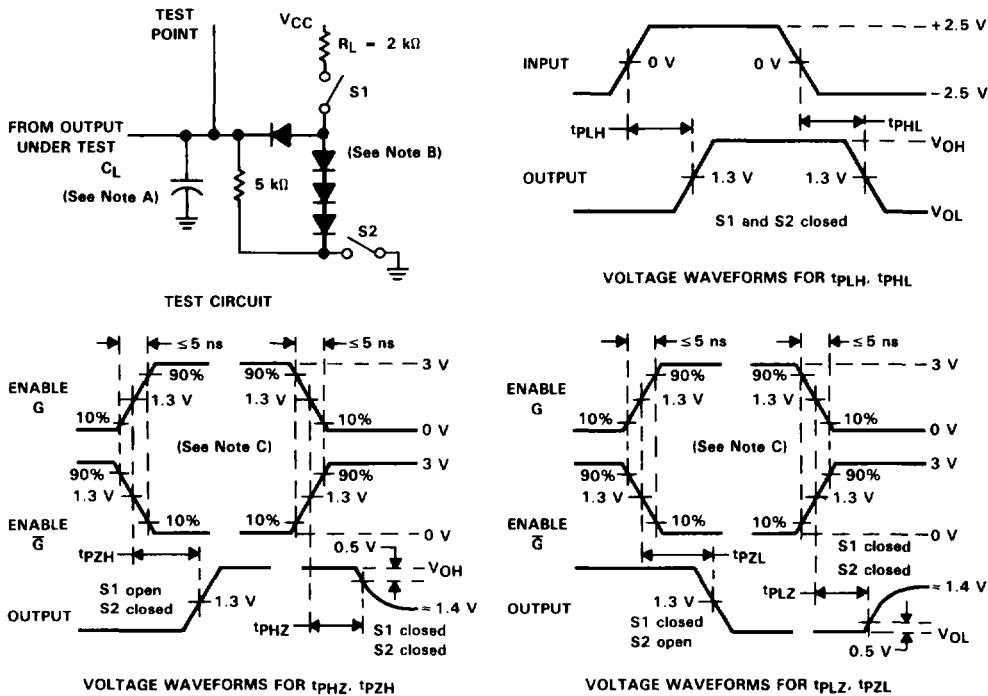
[¶]Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, See Figure 1	20	35		ns
t_{PHL} Propagation delay time, high-to-low-level output		22	35		ns
t_{PZH} Output enable time to high level	$C_L = 15 \text{ pF}$, See Figure 1	17	22		ns
t_{PZL} Output enable time to low level		20	25		ns
t_{PHZ} Output disable time from high level	$C_L = 5 \text{ pF}$, See Figure 1	21	30		ns
t_{PLZ} Output disable time from low level		30	40		ns

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Enable G is tested with \bar{G} high; \bar{G} is tested with G low.

FIGURE 1

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QUADRUPLE DIFFERENTIAL LINE RECEIVERS**

TYPICAL CHARACTERISTICS

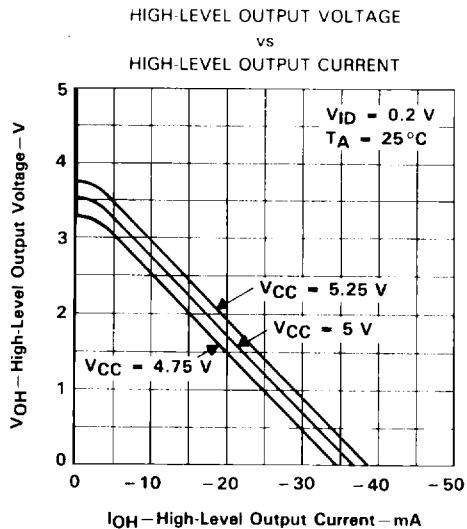


FIGURE 2

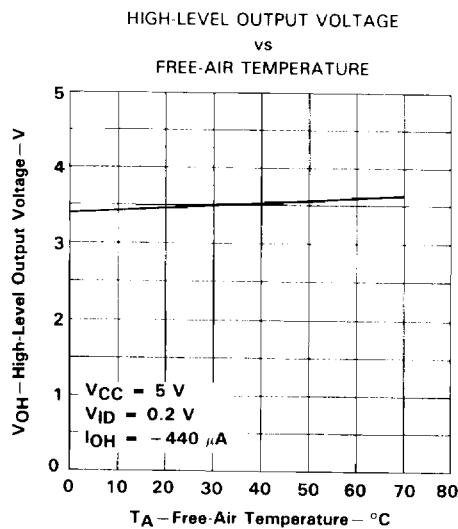


FIGURE 3

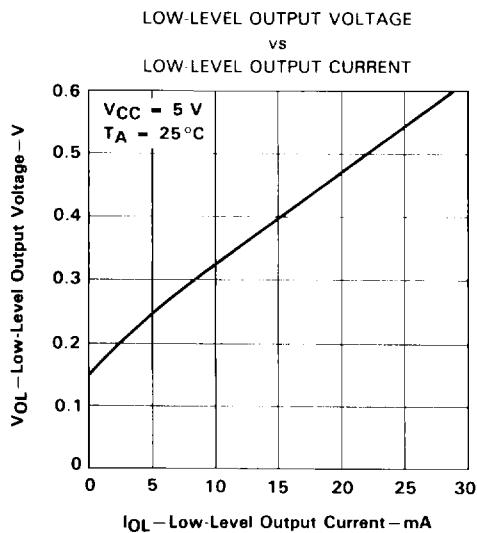


FIGURE 4

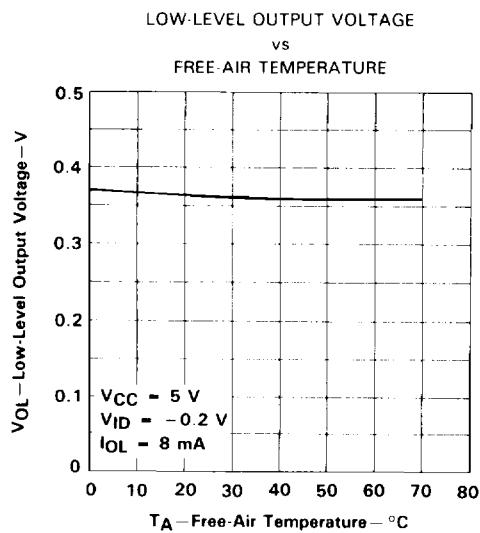


FIGURE 5

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

TYPICAL CHARACTERISTICS

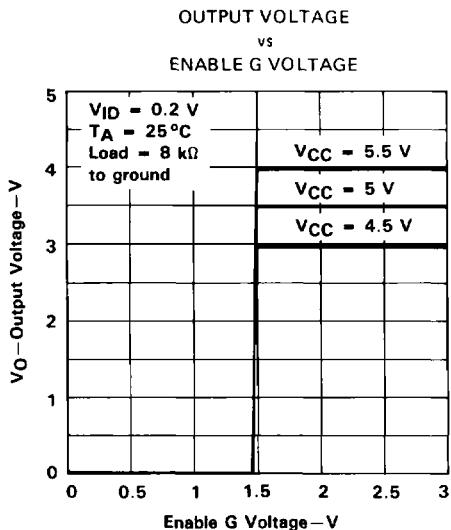


FIGURE 6

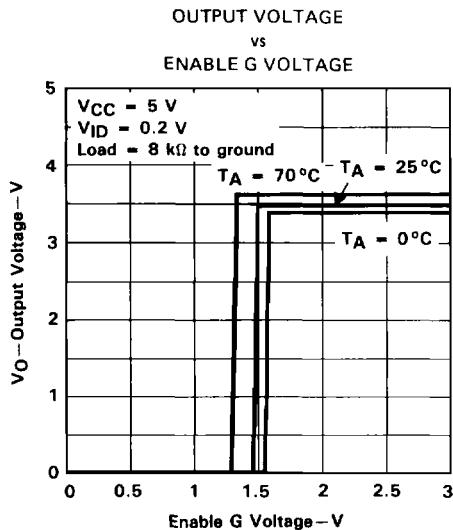


FIGURE 7

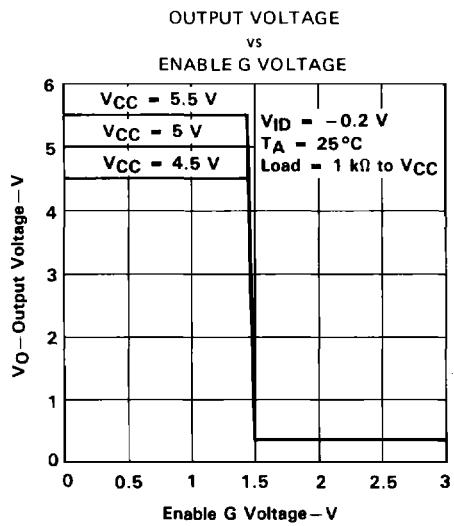


FIGURE 8

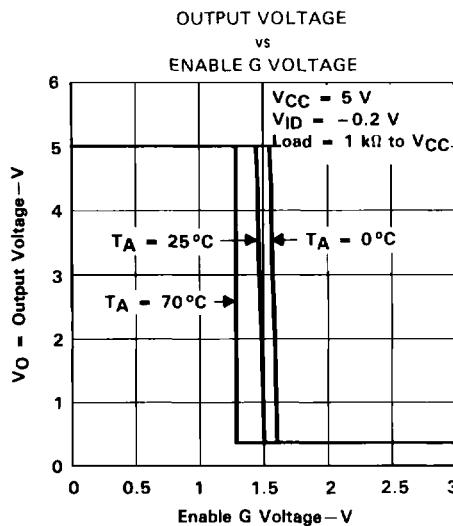


FIGURE 9

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TYPICAL CHARACTERISTICS

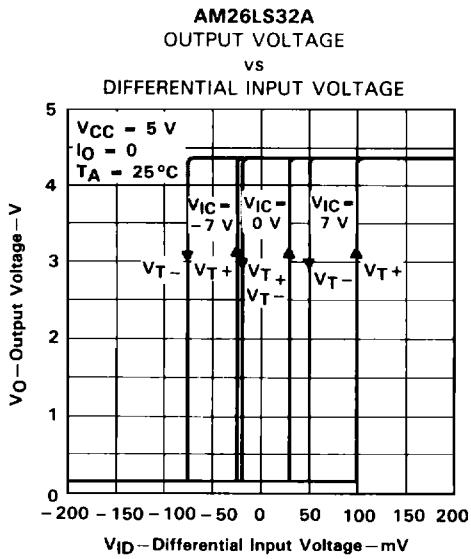


FIGURE 10

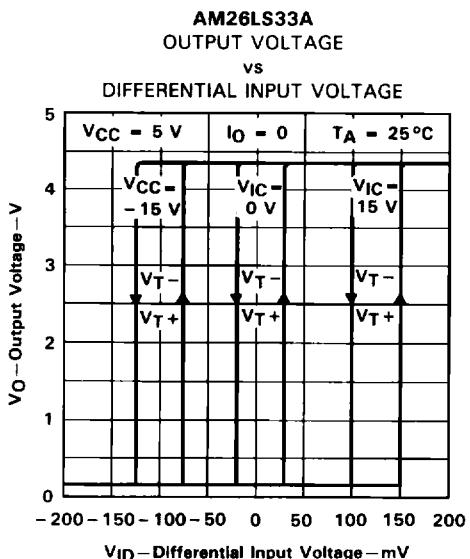


FIGURE 11

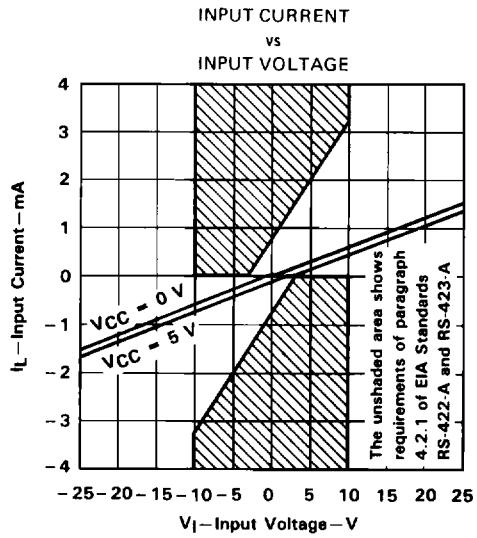


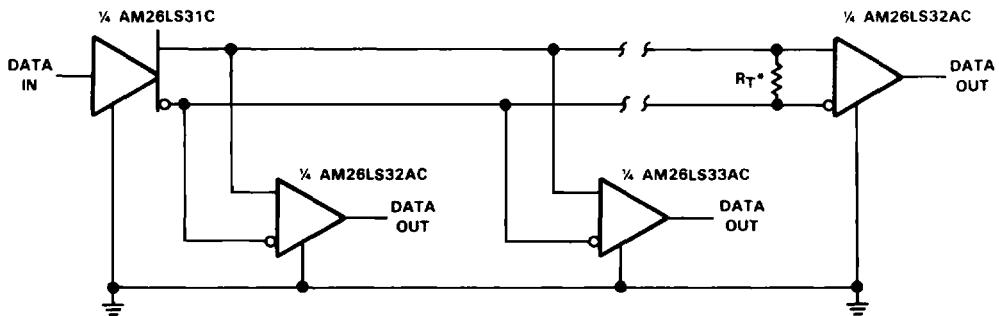
FIGURE 12

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**AM26LS32AM, AM26LS33AM, AM26LS32AC, AM26LS33AC
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APPLICATION INFORMATION



* R_T equals the characteristic impedance of the line.

FIGURE 13. CIRCUIT WITH MULTIPLE RECEIVERS