AN8388S, AN8388SR

4 Ch. Linear Driver IC for CD Player

■ Overview

The AN8388S and AN8388SR employ 4 ch. H-bridge system that they are suitable for driving motor or actuator of CD player. Also they employ the surface mounting type package superior in radiation characteristics.

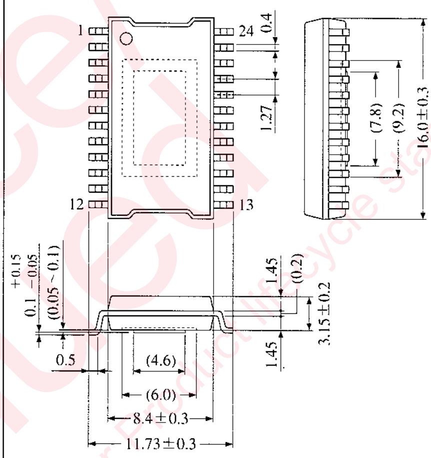
■ Features

- Wide output D-range is available regardless of reference supply on the system.
- 4 ch. BTL Driver built-in. Particularly suitable for driver of actuator or motor of about 8 Ω load.
- PC (Power Control) feature built-in
- Thermal shut down circuit (with hysteresis) built-in
- Control for proper heat of IC by separating the power supplies for signal line and output line.

■ Application

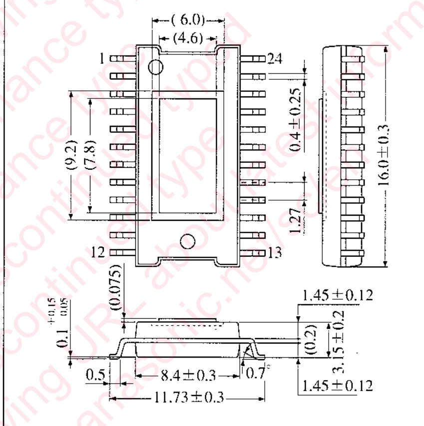
- CD player, CD-ROM
- For drive of motor

AN8388S Unit : mm



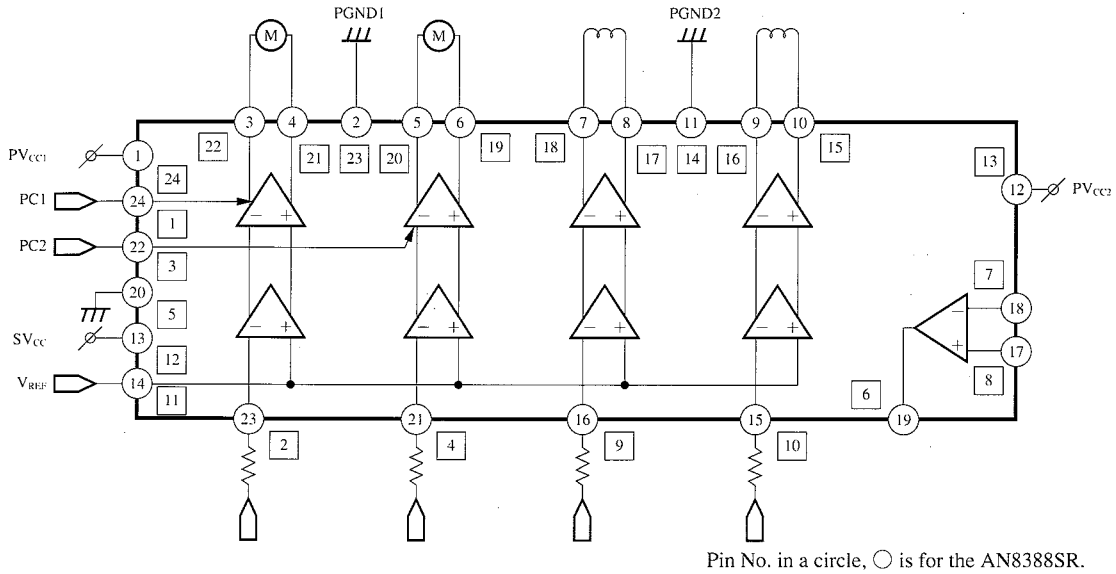
24-lead SOP fin package (HSOP024-P-0450)

AN8388SR Unit : mm



24-lead SOP fin package (HSOP024-P-0450)

■ Block Diagram



Pin No. in a circle, ○ is for the AN8388SR.
Pin No. in a square, □ is for the AN8388S.

■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	SV_{CC}	16	V
Supply Current	I_{CC}	—	mA
Power Dissipation Note)	P_D	2083	mW
Operating Ambient Temperature	T_{opr}	−30 ~ +85	℃
Storage Temperature	T_{stg}	−55 ~ +150	℃

Note) For surface mounting on 50×50×1.2mm glass epoxy board

■ Recommended Operating Range (Ta=25℃)

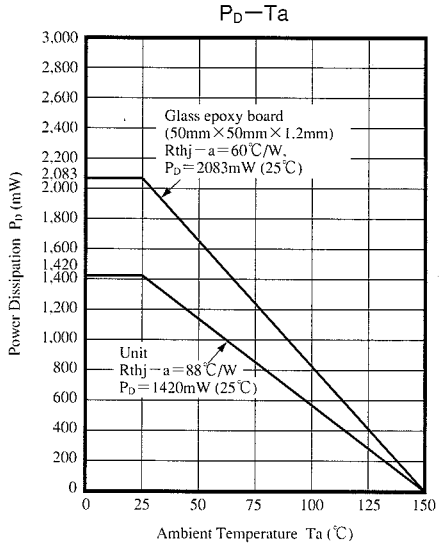
Parameter	Symbol	Range
Operating Supply Voltage Range	V_{CC}	4.5V ~ 15V
	PV_{CC}	

■ Electrical Characteristics (Ta=25℃±2℃)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Total Circuit Current	I_{tot}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$	10	25	40	mA
Reset Circuit						
Reset Operation Release Supply Voltage	V_{RST}	$R_L=8\Omega$	—	—	4.5	V
Driver 1						
Input Offset Voltage	V_{IOF1}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−10	—	10	mV
Output Offset Voltage	V_{OOF1}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−60	—	60	mV
Gain (+)	G_{1+}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	14	17	21	dB
(+) (−) Relative Gain	ΔG_1	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−1.7	0	1.7	dB
Limit Voltage (+)	V_{L1+}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	4.4	4.9	5.4	V
Limit Voltage (−) Note 1)	V_{L1-}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	0.93	1.0	1.07	—
Dead Zone Width	V_{DZ1}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−10	—	20	mV
PC Operation Threshold H	V_{PC1H}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	3	—	—	V
Drivers 2 to 4						
Input Offset Voltage	V_{IOF}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−10	—	10	mV
Output Offset Voltage	V_{OOF}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−60	—	60	mV
Gain (+)	G_+	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	14	17	21	dB
(+) (−) Relative Gain	ΔG	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	0.93	1.0	1.07	—
Limit Voltage (+) Note 2)	V_{L+}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	0.93	1.0	1.07	—
Limit Voltage (−) Note 1)	V_{L-}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	0.93	1.0	1.07	—
Dead Zone Width	V_{DZ}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	−10	—	20	mV
PC Operation Threshold H	V_{PCH}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$, $R_L=8\Omega$, $R_{IN}=10k\Omega$	3	—	—	V
Operational amplifier Offset Voltage	V_{OF-OP}	$PV_{CC1}=PV_{CC2}=SV_{CC}=8V$	−40	—	40	mV
Heat Protection Circuit						
Operation Temperature Equilibrium Value Note 3)	T_{THD}		(—)	(160)	(—)	℃
Operation Temperature Hysteresis Width Note 3)	ΔT_{THD}		(—)	(65)	(—)	℃

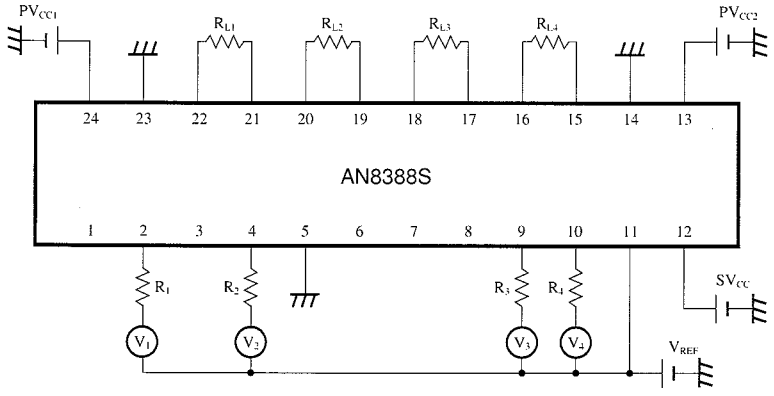
Note1) Relative voltage ratio of limit voltage (−) to limit voltage (+) for each channel.
Note2) Relative voltage ratio of limit voltage (+) of Drivers 2 to 4 to limit voltage (+) of Driver 1
Note3) Characteristic value in parentheses is a reference value for design but not a guaranteed value.

■ Characteristic Curve



■ Cautions for use

• AN8388S



When the AN8388S is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin㉔.

$$I_{P1}=\frac{|V_{22-21}|}{R_{L1}}+\frac{|V_{20-19}|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin⑬.

$$I_{P2}=\frac{|V_{18-17}|}{R_{L3}}+\frac{|V_{16-15}|}{R_{L4}}$$

(3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1}, R_{L2}, R_{L3}, and R_{L4} is as follows:

$$\Delta P_d=(PV_{CC1}-|V_{22-21}|)\times\frac{|V_{22-21}|}{R_{L1}}+(PV_{CC1}-|V_{20-19}|)\times\frac{|V_{20-19}|}{R_{L2}}$$
$$+(PV_{CC2}-|V_{18-17}|)\times\frac{|V_{18-17}|}{R_{L3}}+(PV_{CC2}-|V_{16-15}|)\times\frac{|V_{16-15}|}{R_{L4}}$$

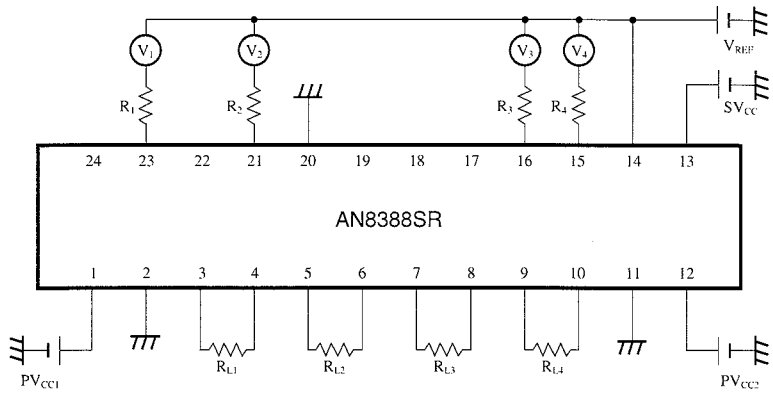
(4) Dissipation increase (ΔP_S) inside the IC (signal block supplied from Pin⑫) caused by loads R_{L1}, R_{L2}, R_{L3}, and R_{L4} is almost as follows:

$$\Delta P_S=V_{CC}\times\left(\frac{|V_1|}{R_1}+\frac{|V_2|}{R_2}+\frac{|V_3|}{R_3}+\frac{|V_4|}{R_4}\right)\times 10+\frac{V_{CC}}{100}\times\left(\frac{|V_{22-21}|}{R_{L1}}+\frac{|V_{20-19}|}{R_{L2}}+\frac{|V_{18-17}|}{R_{L3}}+\frac{|V_{16-15}|}{R_{L4}}\right)$$

(5) Dissipation increase inside the IC during driver running is $\Delta P_d+\Delta P_S$.

■ Cautions for use

• AN8388SR



When the AN8388SR is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin①.

$$I_{P1}=\frac{|V_{3-4}|}{R_{L1}}+\frac{|V_{5-6}|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin⑫.

$$I_{P2}=\frac{|V_{7-8}|}{R_{L3}}+\frac{|V_{9-10}|}{R_{L4}}$$

(3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is as follows:

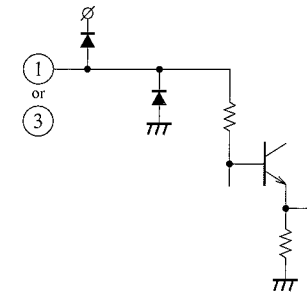
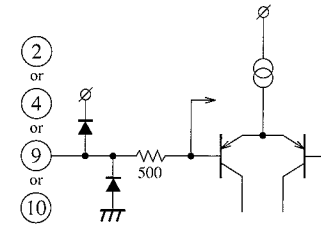
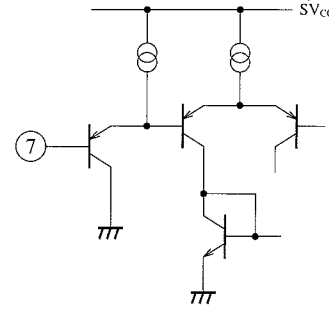
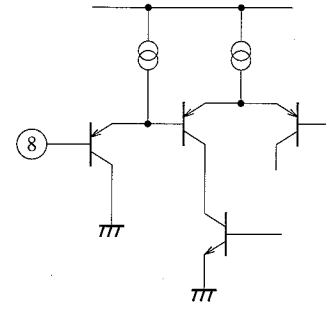
$$\Delta P_d=(PV_{CC1}-|V_{3-4}|)\times\frac{|V_{3-4}|}{R_{L1}}+(PV_{CC1}-|V_{5-6}|)\times\frac{|V_{5-6}|}{R_{L2}}$$
$$+(PV_{CC2}-|V_{7-8}|)\times\frac{|V_{7-8}|}{R_{L3}}+(PV_{CC2}-|V_{9-10}|)\times\frac{|V_{9-10}|}{R_{L4}}$$

(4) Dissipation increase (ΔP_S) inside the IC (signal block supplied from Pin⑬) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is almost as follows:

$$\Delta P_S=V_{CC}\times\left(\frac{|V_1|}{R_1}+\frac{|V_2|}{R_2}+\frac{|V_3|}{R_3}+\frac{|V_4|}{R_4}\right)\times 10+\frac{V_{CC}}{100}\times\left(\frac{|V_{3-4}|}{R_{L1}}+\frac{|V_{5-6}|}{R_{L2}}+\frac{|V_{7-8}|}{R_{L3}}+\frac{|V_{9-10}|}{R_{L4}}\right)$$

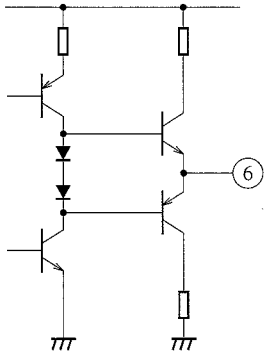
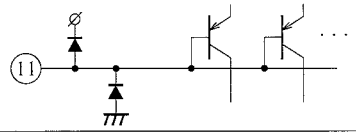
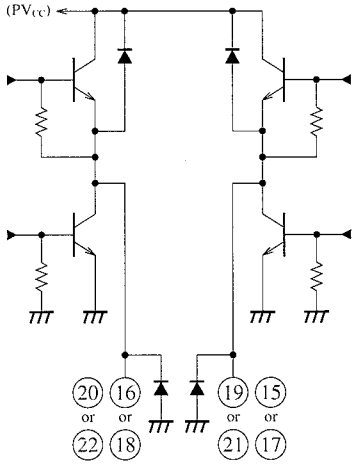
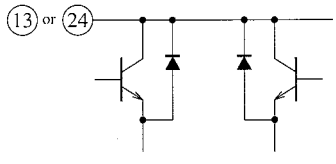
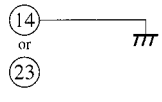
(5) Dissipation increase inside the IC during driver running is, $\Delta P_d+\Delta P_S$.

■ Pin Description

Pin No. AN8388S	Pin No. AN8388SR	Symbol	I/O	DC voltage (V_{CC}/8V)	Pin Description	Equivalent Circuit
1	24	PC1	I	0V	PC (power cut) input pin controlling the output of ㉑ and ㉒	
3	22	PC2	I	0V	PC (power cut) input pin controlling the output of ⑲ and ⑳	
2	23	IN1	I	2.5V	Error input pin of Driver 1	
4	21	IN2	I	2.5V	Error input pin of Driver 2	
9	16	IN3	I	2.5V	Error input pin of Driver 3	
10	15	IN4	I	2.5V	Error input pin of Driver 4	
7	18	IN−	I	— V	Reverse rotation input pin of operational amplifier	
8	17	IN+	I	— V	Normal rotation input pin of operational amplifier	
12	13	SV_{CC}	I	8V	SV_{CC} pin for control circuit of driver, not connected to power V_{CC} pin.	
5	20	SGND	I	0V	SGND pin for control circuit of driver	

Note) The pin numbers shown in the equivalent circuit diagram are only for the AN8388S. For the AN8388SR, they must be replaced.

■ Pin Description (Cont.)

Pin No. AN8388S	Pin No. AN8388SR	Symbol	I/O	DC voltage (V_{CC}/8V)	Pin Description	Equivalent Circuit
6	19	OPO	O	— V	Operational amplifier output pin	
11	14	V_{REF}	I	2.5V	V_{REF} input pin	
22	3	D1−	O	0V	Reverse rotation output pin of Driver 1	
21	4	D1+	O	0V	Normal rotation output pin of Driver 1	
20	5	D2−	O	0V	Reverse rotation output pin of Driver 2	
19	6	D2+	O	0V	Normal rotation output pin of Driver 2	
18	7	D3−	O	0V	Reverse rotation output pin of Driver 3	
17	8	D3+	O	0V	Normal rotation output pin of Driver 3	
16	9	D4−	O	0V	Reverse rotation output pin of Driver 4	
15	10	D4+	O	0V	Normal rotation output pin of Driver 4	
24	1	PV_{CC1}	I	8V	Power V_{CC} pin, supplying the current flowing for output power transistors of ⑲, ⑳, ㉑, and ㉒	
13	12	PV_{CC2}	I	8V	Power V_{CC} pin, supplying the current flowing for output power transistors of ⑮, ⑯, ⑰, and ⑱	
23	2	PGND1	I	0V	PGND pin for output transistors of ⑲, ⑳, ㉑, and ㉒	
14	11	PGND2	I	0V	PGND pin for output transistors of ⑮, ⑯, ⑰, and ⑱	

Note) The pin numbers shown in the equivalent circuit diagram are only for the AN8388S. For the AN8388SR, they must be replaced.

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