8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89480/MB89480L Series

MB89485/485L/P485/P485L/PV480

■ DESCRIPTION

The MB89480 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as 21-bit time-base timer, watch prescaler, PWC timer, PWM timer, 8/16-bit timer/counter, 6-bit PPG, LCD controller/driver, external interrupt 1 (edge), external interrupt 2 (level), 10-bit A/D converter, UART/SIO, buzzer, watchdog timer reset.

The MB89480 series is designed suitable for LCD remote controller as well as in a wide range of applications for consumer product.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Package used
  QFP package and SH-DIP package for MB89P485/P485L, MB89485/485L
  MQFP package for MB89PV480
- High-speed operating capability at low voltage
- Minimum execution time: 0.32 µs/12.5MHz

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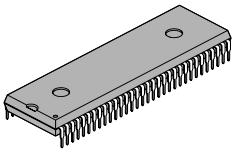
■ PACKAGE

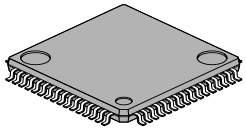
64-pin Plastic SH-DIP



(DIP-64P-M01)

(DIP-64P-M01)

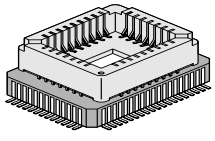
64-pin Plastic QFP



(FPT-64P-M09)

(FPT-64P-M09)

64-pin Ceramic MQFP



(MQP-64C-P01)

(MQP-64C-P01)

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- F²MC-8L family CPU core

  Instruction set optimized for controllers { Multiplication and division instructions; 16-bit arithmetic operations; Test and branch instructions; Bit manipulation instructions, etc.

- Six timers
  PWC timer (also usable as a interval timer)
  PWM timer
  8/16-bit timer/counter x 2
  21-bit timebase timer
  watch prescaler
- Programmable pulse generator
  6-bit PPG with program-selectable pulse width and period
- External interrupts
  Edge detection (Selectable edge) : 4 channels
  Low-level interrupt (Wake-up function) : 8 channels
- A/D converter (4 channels)
  10-bit successive approximation type
- UART/SIO
  Synchronous/asynchronous data transfer capable
- LCD controller/driver
  max. 31 segments output x 4 commons
  booster for LCD driving (selected by mask option)
- Buzzer
  7 frequency types are selectable by software
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Watch mode (Everything except the watch prescaler stops to reduce the power comsumption to an extremely low level.)
  Subclock mode
- Watch dog timer reset
- I/O ports: max. 42 channels

■ PRODUCT LINEUP

Parameter \ Part number	MB89485L	MB89485	MB89P485L	MB89P485	MB89PV480
Classification	Mass production products (mask ROM product)		OTP		Piggy-back
ROM size	16K x 8-bit (internal ROM)		16K x 8-bit (internal PROM with read protection *2)		32K x 8-bit (external ROM)*1
RAM size	512 x 8 bits				1K × 8 bits

*1 : Use MBM27C256A as the external ROM.

*2 : Read protection feature is selected by part number, detail please refer to MASK OPTIONS.

Parameter \ Part number	MB89485L	MB89485	MB89P485L	MB89P485	MB89PV480
CPU functions	Number of instructions: : 136 Instruction bit length: : 8 bits Instruction length: : 1 to 3 bytes Data bit length: : 1, 8, 16 bits Minimum execution time: : 0.32 µs/12.5 MHz Minimum interrupt processing time: : 2.88 µs/12.5 MHz				
Ports	I/O ports (CMOS) : 11 pins N-channel open drain I/O ports : 28 pins Output ports (N-channel open drain) : 2 pins Input port : 1 pin Total : 42 pins				
21-Bit Time-based timer	Interrupt period (0.66ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz				
Watchdog timer	Reset period (167.8 ms to 335.5 ms) at 12.5 MHz				
Pulse width count timer	2 channels 8-bit one-shot timer operation (supports underflow output, operating clock period: 1, 4, 32 tinst, external) 8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 tinst, external) 8-bit pulse width measurement operation (supports continuous measurement, H width, L width, rising edge to rising edge, falling edge to falling edge measurement and both edge measurement)				
PWM timer	8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 tinst, external) 8-bit resolution PWM operation				
6- Bit programmable pulse generator	Can generate square pulse with programmable period.				
8/16-Bit timer/ counter 11,12	Can be operated either as a 2-channel 8-bit timer/counter (Timer 11 and Timer 12, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 11 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable				
8/16-Bit timer/ counter 21,22	Can be operated either as a 2-channel 8-bit timer/counter (Timer 21 and Timer 22, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 21 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable				
External interrupt	4 independent channels (selectable edge, interrupt vector, request flag) 8 channels (low level interrupt)				
A/D converter	10-bit resolution × 4 channels A/D conversion function (conversion time: 60 tinst) Supports repeated activation by internal clock.				
LCD controller/driver	Common output: 4 (max.) Segment output: 31 (max.) (selected resistor ladder) 26 (max.) (selected booster) Bias power supply pins: 4 LCD display RAM size: 31 × 4 bits Dividing resistor/booster: selected by mask option				
UART/SIO	Synchronous/asynchronous data transfer capable (Max. baud rate: 97.656 Kbps at 12.5 MHz) (7 and 8 bits with parity bit ; 8 and 9 bits without parity bit)				
Buzzer output	7 frequency types are selectable by software.				

Part number / Parameter	MB89485L	MB89485	MB89P485L	MB89P485	MB89PV480
Standby mode	Sleep mode, stop mode, watch mode, subclock mode.				
Process	CMOS				
Operating Voltage	2.2V ~ 3.6V	2.2V ~ 5.5V	2.7V ~ 3.6V	3.5V ~ 5.5V	2.7V ~ 5.5V

Note: 1 tinst = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

■ PACKAGE AND CORRESPONDING PRODUCTS

Device / Package	MB89485/485L	MB89P485/P485L	MB89PV480
DIP-64P-M01	O	O	X
FPT-64P-M09	O	O	X
MQP-64C-P01	X	X	O

O : Availabe
X : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

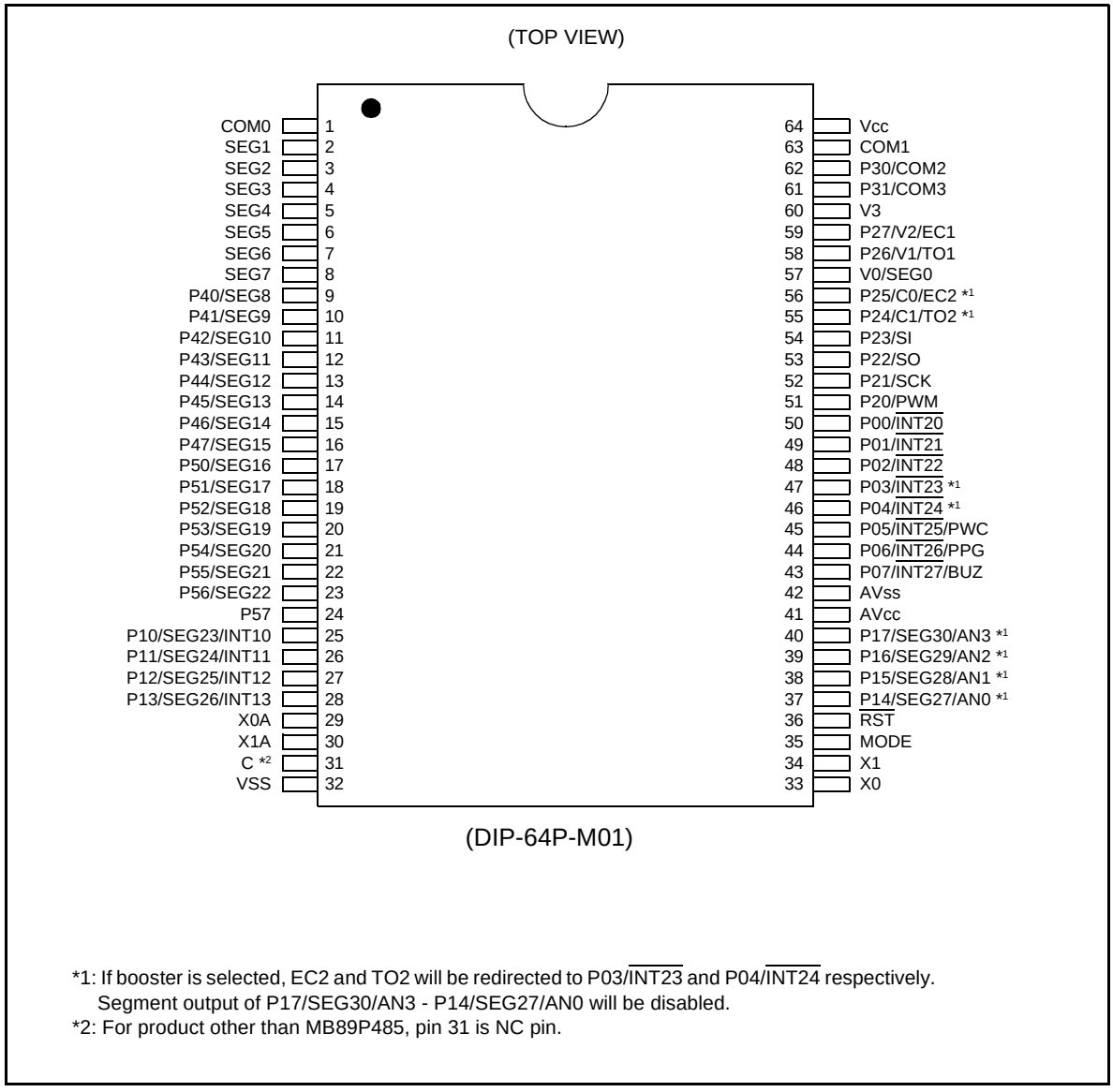
2. Current Consumption

- For the MB89PV480, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than that for the mask ROM product. However, the current consumption are roughly the same in sleep or stop mode.
- For more information, see “■ Electrical Characteristics.”

3. Oscillation stabilization time after power-on reset

- For MB89PV480,MB89P485L and MB89485L, there is no power-on stabilization time after power-on reset.
- For MB89P485, there is power-on stabilization time after power-on reset.
- For MB89485, the power-on stabilization time can be selected.
- For more information, refer to “■ Mask Option”.

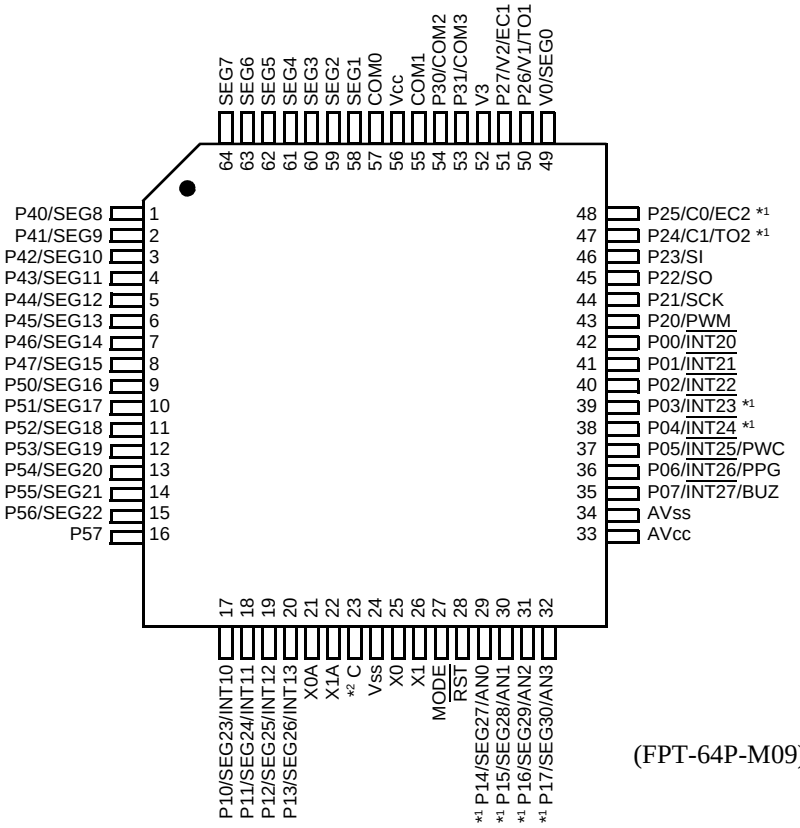
■ PIN ASSIGNMENT



(DIP-64P-M01)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively.
Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.
*2: For product other than MB89P485, pin 31 is NC pin.

(TOP VIEW)

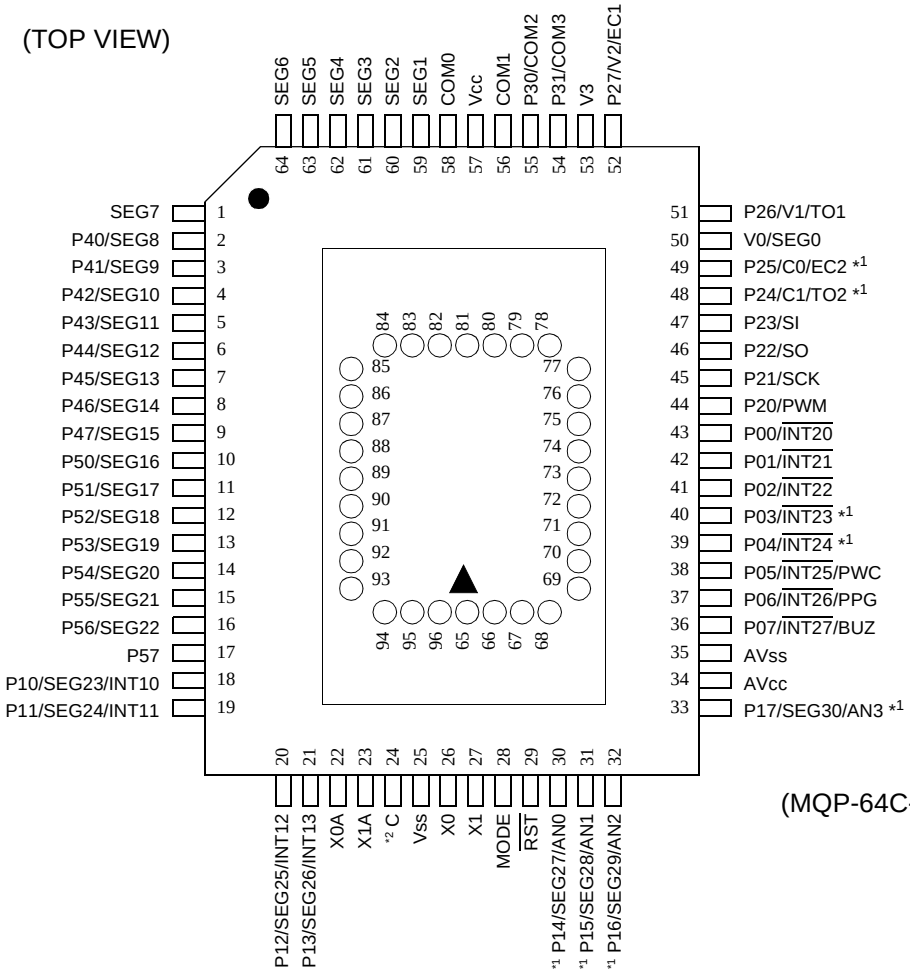


(FPT-64P-M09)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.

*2: For product other than MB89P485, pin 23 is NC pin.

(TOP VIEW)



(MQP-64C-P01)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.

*2: Pin 24 is NC pin.

Pin assignment on package top

Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol	Pin No.	Pin Symbol
65	N.C.	73	A2	81	N.C.	89	$\overline{\text{OE}}$
66	V_{pp}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{\text{CE}}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: As connected internally, do not use.

■ PIN DESCRIPTION

Pin Number			Pin Name	I/O Circuit Type	Function
SH-DIP*1	MQFP*2	QFP*3			
33	26	25	X0	A	Connection pins for a crystal or other oscillator. An external clock can be connected to X0. In this case, leave X1 open.
34	27	26	X1		
29	22	21	X0A	A	Connection pins for a crystal or other oscillator. An external clock can be connected to X0A. In this case, leave X1A open.
30	23	22	X1A		
35	28	27	MODE	B	Input pins for setting the memory access mode. Connect directly to V_{SS}.
36	29	28	$\overline{RST}$	C	Reset I/O pin. The pin is a N-ch open-drain type with pull-up resistor and a hysteresis input. The pin outputs a “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits.
50 ~ 48	43 ~ 41	42 ~ 40	P00/$\overline{INT20}$ ~ P02/$\overline{INT22}$	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input.
47	40	39	P03/$\overline{INT23}$	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input, and shared with 8/16-bit timer/counter 21, 22 input when booster is selected.
46	39	38	P04/$\overline{INT24}$	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input, and shared with 8/16-bit timer/counter 21, 22 output when booster is selected.
45	38	37	P05/$\overline{INT25}$/ PWC	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input, and PWC input.
44	37	36	P06/$\overline{INT26}$/ PPG	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input, and 6-bit PPG output.
43	36	35	P07/$\overline{INT27}$/ BUZ	D	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with external interrupt 2 input and buzzer output.
25 ~ 28	18 ~ 21	17 ~ 20	P10/SEG23/ INT10 ~ P13/SEG26/ INT13	F / K	General-purpose N-ch Open-drain I/O port. A hysteresis input. The pin is shared with external interrupt 1 input and LCD segment output.
37 ~ 40	30 ~ 33	29 ~ 32	P14/SEG27/ AN0 ~ P17/SEG30/ AN3	G / K	General-purpose N-ch Open-drain I/O port. An analog input. The pin is shared with A/D converter input and LCD segment output. LCD segment output will be disabled when booster is selected.

*1: DIP-64P-M01
*2: MQP-64C-P01
*3: FPT-64P-M09

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Pin Number			Pin Name	I/O Circuit Type	Function
SH-DIP*1	MQFP*2	QFP*3			
51	44	43	P20/PWM	E	General-purpose CMOS I/O port. The pin is shared with PWM output.
52	45	44	P21/SCK	E	General-purpose CMOS I/O port. The pin is shared with UART/SIO clock I/O.
53	46	45	P22/SO	E	General-purpose CMOS I/O port. The pin is shared with UART/SIO data output.
54	47	46	P23/SI	D	General-purpose CMOS I/O port. The pin is shared with UART/SIO data input.
55	48	47	P24/C1/TO2	H	General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer 21,22 output (It is redirected to P04/INT24 when booster is selected), and as a capacitor connecting pin when booster is selected.
56	49	48	P25/C0/EC2	F	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with 8/16-bit timer 21,22 input (It is redirected to P03/INT23 when booster is selected), and as a capacitor connecting pin when booster is selected.
58	51	50	P26/V1/TO1	H	General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer 11,12 output, and LCD power driving pin.
59	52	51	P27/V2/EC1	F	General-purpose CMOS I/O port. A hysteresis input. The pin is shared with 8/16-bit timer 11,12 input, and LCD power driving pin.
62	55	54	P30/COM2	I / K	General-purpose N-ch Open-drain output port. The pin is shared with the LCD common output
61	54	53	P31/COM3	I / K	General-purpose N-ch Open-drain output port. The pin is shared with the LCD common output
9 ~ 16	2 ~ 9	1 ~ 8	P40/SEG8 ~ P47/SEG15	H / K	General-purpose N-ch Open-drain I/O port. The pin is shared with LCD segment output.
17 ~ 23	10 ~ 16	9 ~ 15	P50/SEG16 ~ P56/SEG22	H / K	General-purpose N-ch Open-drain I/O port. The pin is shared with LCD segment output.
24	17	16	P57	J	General-purpose CMOS input port.

*1: DIP-64P-M01
*2: MQP-64C-P01
*3: FPT-64P-M09

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Pin Number			Pin Name	I/O Circuit Type	Function
SH-DIP*1	MQFP*2	QFP*3			
2 ~ 8	59 ~ 64, 1	58 ~ 64	SEG1 ~ SEG7	K	LCD segment output only pins.
1, 63	58, 56	57, 55	COM0 ~ COM1	K	LCD common output only pins.
60	53	52	V3	—	LCD driving power supply pin.
57	50	49	V0/SEG0	— / K	LCD driving power supply pin when booster is selected. LCD segment output when booster is not selected.
31	24	23	C	—	Capacitor connection pin *4
64	57	56	V_{CC}	—	Power supply pin (+3V or +5V).
32	25	24	V_{SS}	—	Power supply pin (GND).
41	34	33	AV_{CC}	—	A/D converter power supply pin.
42	35	34	AV_{SS}	—	A/D converter power supply pin. Use at the same voltage level as V_{SS}.

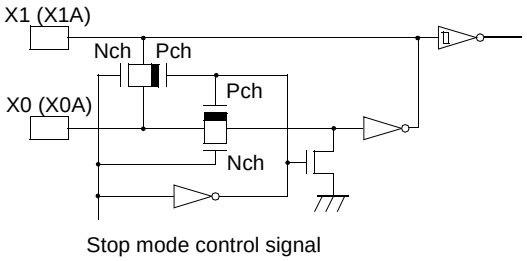
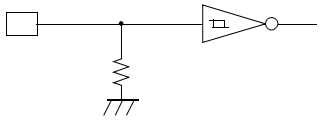
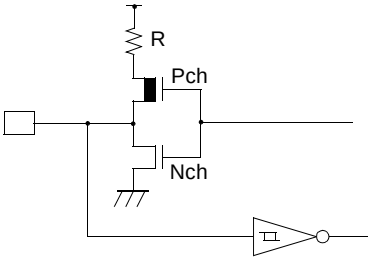
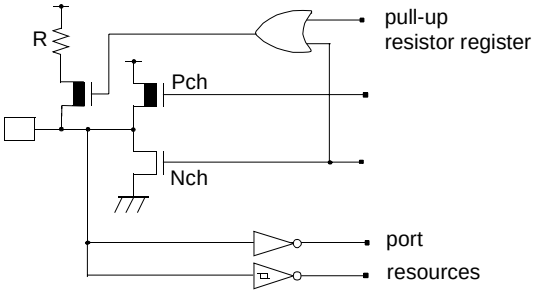
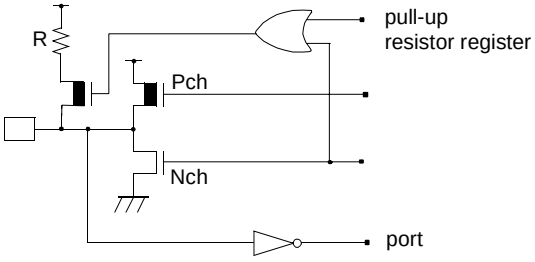
*1: DIP-64P-M01
*2: MQP-64C-P01
*3: FPT-64P-M09
*4: When MB89485/485L, MB89P485L or MB89PV480 is used, this pin will become a N.C. pin. When MB89P485 is used, connect this pin to an external 0.1uF capacitor to ground.

• External EPROM Socket (MB89PV480 only)

Pin Numbe MQFP*1	Pin Name	I/O	Function
95 94 67 91 88 92 93 68 69 70 71 72 73 74 75	A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins.
86 85 84 83 82 79 78 77	O8 O7 O6 O5 O4 O3 O2 O1	I	Data input pins.
65 76 81 90	N.C.	—	Internally connected pins. Always leave open.
66	V_{pp}	O	“H” level output pin.
80	V_{SS}	O	Power supply pin (GND).
87	$\overline{CE}$	O	Chip enable pin for the EPROM. Outputs “H” in standby mode.
89	$\overline{OE}$	O	Output enable pin for the EPROM. Always outputs “L”.
96	V_{CC}	O	Power supply pin for the EPROM.

*1: MQP-64C-P01

■ I/O CIRCUIT TYPE

Circuit Class	Circuit	Remarks
A		• Main/Sub clock circuit
B		• Hysteresis input • The pull-down resistor Approx. 50kΩ. (not available in MB89P485/ P485L)
C		• The pull-up resistance (P-channel) Approx. 50 kΩ. • Hysteresis input
D		• CMOS output • CMOS input • Hysteresis input • Selectable pull-up resistor Approx. 50 kΩ
E		• CMOS output • CMOS input • Selectable pull-up resistor Approx. 50 kΩ

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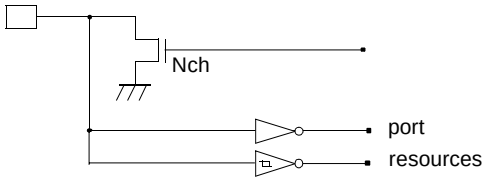
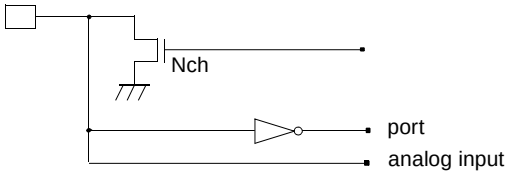
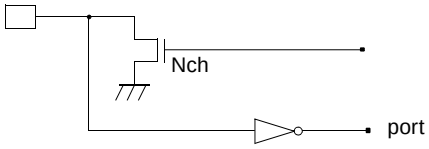
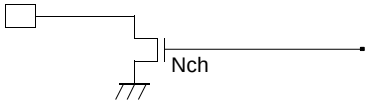
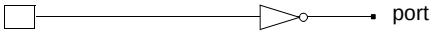
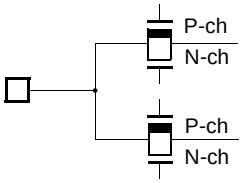
F		• N-ch open-drain output • CMOS input • Hysteresis input
G		• N-ch open-drain output • CMOS input • Analog input
H		• N-ch open-drain output • CMOS input
I		• N-ch open-drain output
J		• CMOS input
K		• LCD segment output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC}) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

■ PROGRAMMING OTPROM IN MB89P485/P485L WITH SERIAL PROGRAMMER

1. Programming the OTPROM with serial programmer

- All OTP products can be programmed with serial programmer

2. Programming the OTPROM

- To program the OTPROM using EPROM programmer AF200 (manufacturer: Yokogawa Digital Computer Corp.).

  Inquiry : Yokogawa Digital Computer Corp. : TEL (81)-42-333-6224

- To program the OTPROM using FUJITSU MCU programmer MB91919-001.

  Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

  FAX (65)-2810220

3. Programming Adaptor for OTPROM

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adapter listed below.

Package	Compatible socker adaptor
DIP-64P-M01	MB91919-812
FPT-64P-M09	MB91919-813

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770

FAX (65)-2810220

4. OTPROM Content Protection

For product with OTPROM content protection feature (MB89P485-103, MB89P485-104), OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM ($FFFC_H$) is assigned to be used for preventing the read access of OTPROM content. If the protection code "00_H" is written in this address ($FFFC_H$), the OTPROM content cannot be read by any serial programmer.

Note: The program written into the OTPROM cannot be verified once the OTPROM protection code is written ("00_H" in $FFFC_H$). It is advised to write the OTPROM protection code at last.

5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING OTPROM IN MB89P485/P485L WITH GENERAL PURPOSE EPROM PROGRAMMER

1. Programming OTPROM with general purpose EPROM programmer

- Only products without protection feature (i.e. MB89P485/P485L-101 and MB89P485/P485L-102) can be programmed with general purpose EPROM programmer. Product with protection feature (i.e. MB89P485/P485L-103 and MB89P485/P485L-104) cannot be programmed with general purpose programmer.

2. ROM Writer Adapters and Recommended ROM Writers

- The following shows ROM writer adapters and recommended ROM writers.

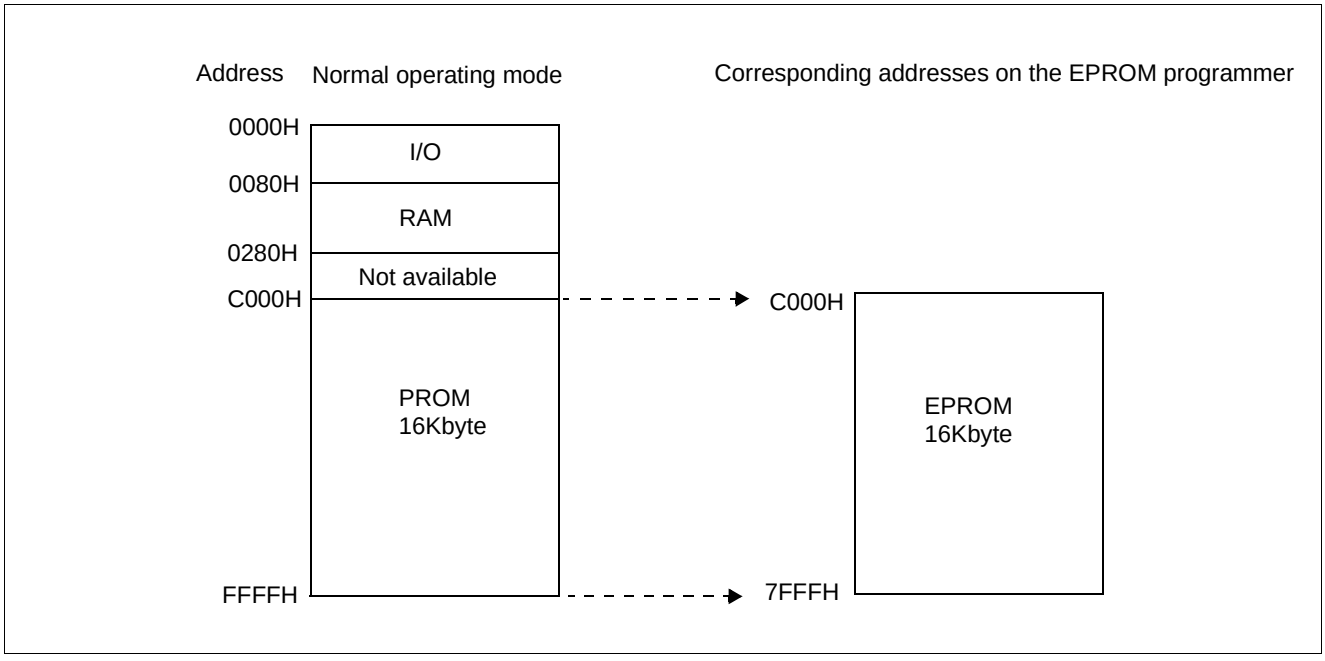
Package name	Applicable adapter model	Recommended writer maker and writer
	Fujitsu Microelectronics Asia Pte Ltd.	Minato electronics Co., Ltd.
		MODEL1890A
DIP-64P-M01	MB91919-604	Under evaluation
FPT-64P-M09	MB91919-605	Under evaluation

- Contact information

  Minato electronics Co., Ltd.: Phone 045-591-5611

3. Memory Space

■ Memory Map of Piggyback/Evaluation Device



4. Writing data to the EPROM

(1) Set the EPROM writer for the CU50-OTP (device code: T.B.D).

(2) Load the program data to the EPROM writer.

(3) Write data using the EPROM writer.

4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

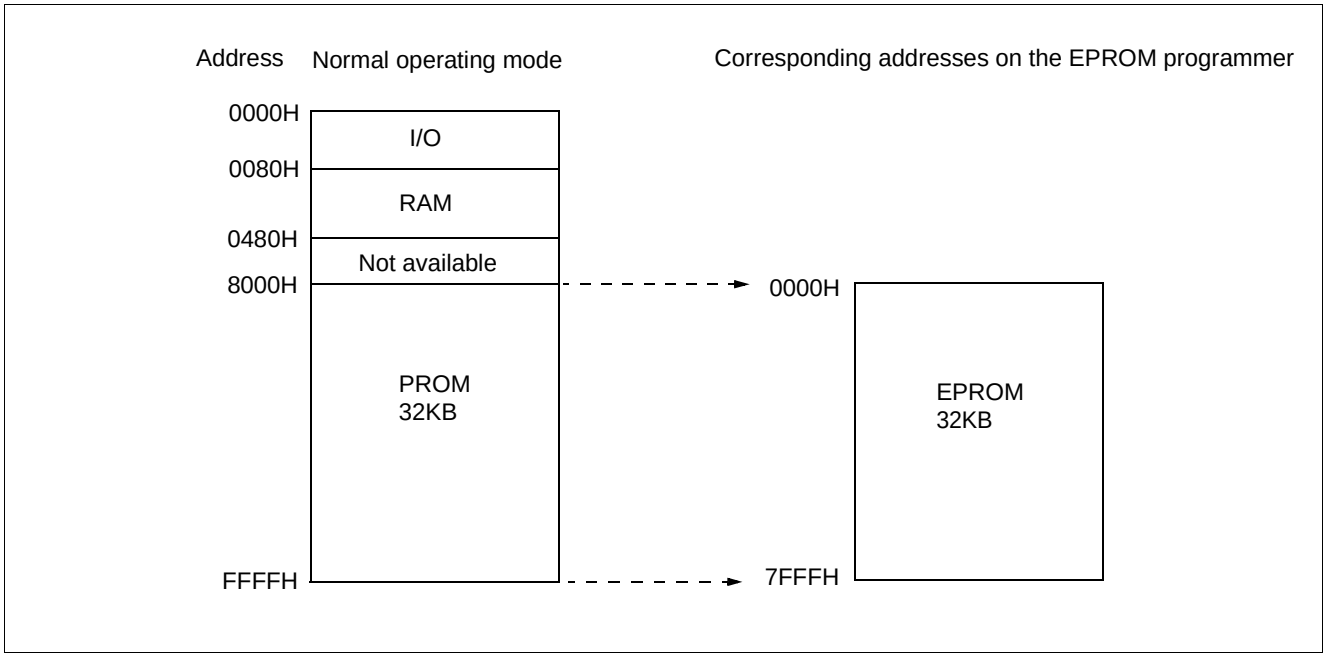
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

3. Memory Space

Memory space in each mode is diagrammed below.



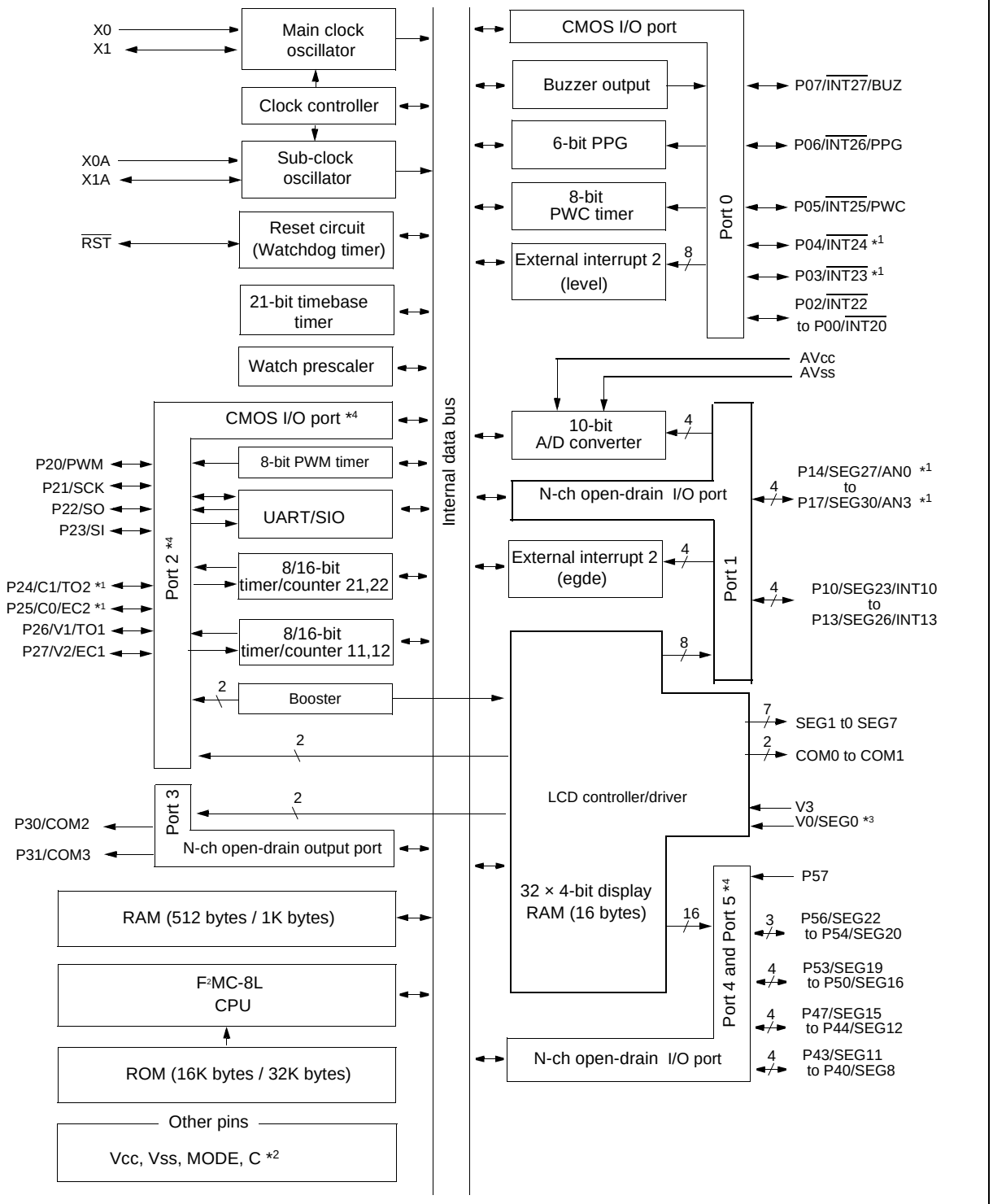
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ Block Diagram



*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P14/SEG27/AN0 to P17/SEG30/AN3 will be disabled.

*2: For product other than MB89P485, C pin is NC pin.

*3: If booster is selected, it serves as V0. If booster is not selected, it serves as SEG0.

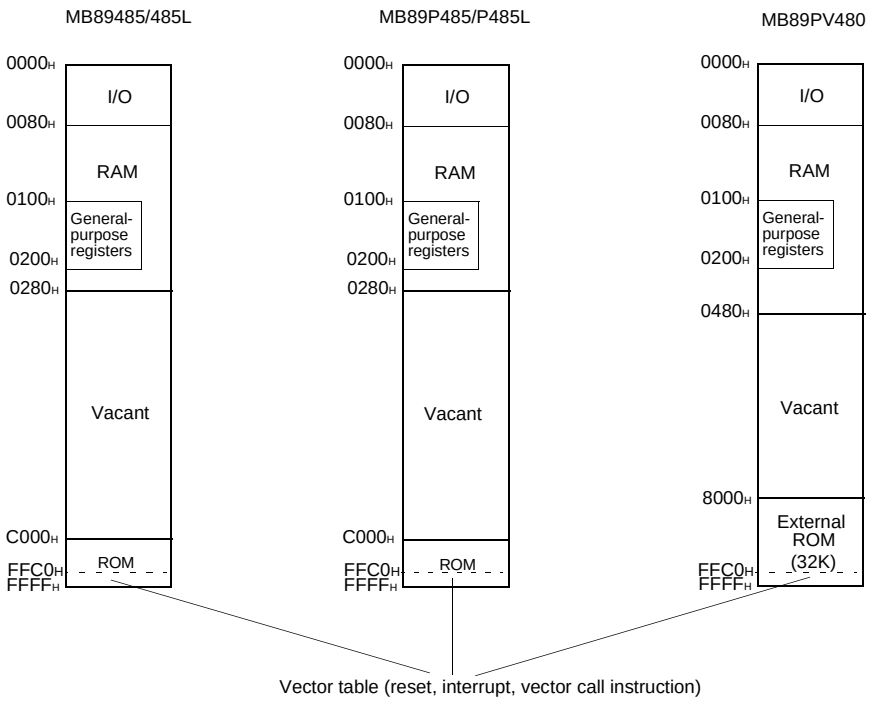
*4: P20 to P23 are CMOS I/O ports. P24 to P27 are N-ch open-drain I/O ports. P57 is input-only port.

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89480 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89480 series is structured as illustrated below.

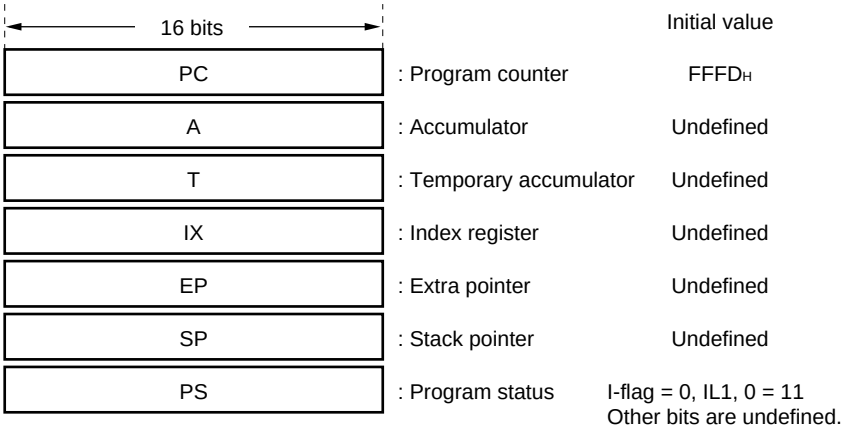
Memory Space



2. Registers

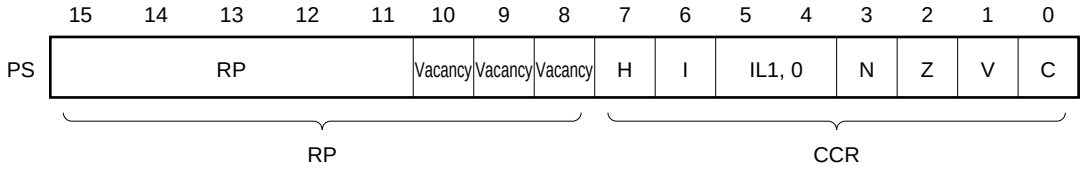
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



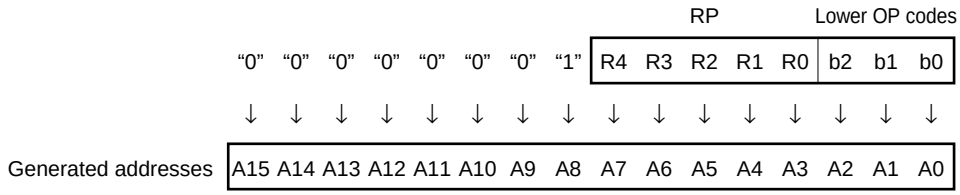
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

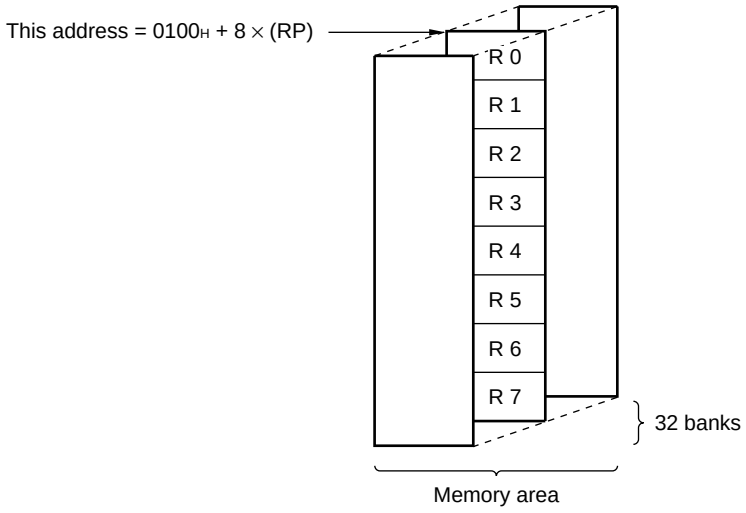
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89480 series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00_H	PDR0	Port 0 data register	R/W	$XXXXXXXX_B$
01_H	DDR0	Port 0 data direction register	W*	00000000_B
02_H	PDR1	Port 1 data register	R/W	$XXXXXXXX_B$
03_H	DDR1	Port 1 data direction register	W*	00000000_B
04_H	PDR2	Port 2 data register	R/W	00000000_B
05_H	(Reserved)			
06_H	DDR2	Port 2 data direction register	R/W	00000000_B
07_H	SYCC	System clock control register	R/W	$X\text{-}1MM100_B$
08_H	STBC	Standby control register	R/W	$00010XXX_B$
09_H	WDTC	Watchdog timer control register	W*	$0\text{---}XXXX_B$
$0A_H$	TBTC	Timebase timer control register	R/W	$00\text{---}000_B$
$0B_H$	WPCR	Watch prescaler control register	R/W	$00\text{--}0000_B$
$0C_H$	PDR3	Port 3 data register	R/W	$\text{------}11_B$
$0D_H$	(Reserved)			
$0E_H$	RSFR	Reset flag register	R	$XXXX\text{----}_B$
$0F_H$	(Reserved)			
10_H	PDR4	Port 4 data register	R/W	11111111_B
11_H	(Reserved)			
12_H	PDR5	Port 5 data register	R/W	$X1111111_B$
13_H	(Reserved)			
14_H to $1F_H$	(Reserved)			
20_H	SMC1	UART/SIO mode control register 1	R/W	00000000_B
21_H	SMC2	UART/SIO mode control register 2	R/W	00000000_B
22_H	SRC	UART/SIO rate control register	R/W	$XXXXXXXX_B$
23_H	SSD	UART/SIO status/data register	R	00001---_B
24_H	SIDR/SODR	UART/SIO data register	R/W	$XXXXXXXX_B$
25_H	EIC1	External interrupt 1 control register 1	R/W	00000000_B
26_H	EIC2	External interrupt 1 control register 2	R/W	00000000_B
27_H	EIE2	External interrupt 2 enable register	R/W	00000000_B
28_H	EIF2	External interrupt 2 flag register	R/W	$\text{-------}0_B$
29_H to $2B_H$	(Reserved)			
$2C_H$	ADC1	A/D control register 1	R/W	$\text{-}0000000_B$
$2D_H$	ADC2	A/D control register 2	R/W	$\text{-}0000001_B$
$2E_H$	ADDH	A/D data register (Upper byte)	R	$\text{------}XX_B$
$2F_H$	ADDL	A/D data register (Lower byte)	R	$XXXXXXXX_B$
30_H	ADEN	A/D input enable register	R/W	1111----_B
31_H	PCR1	PWC control register 1	R/W	$0\text{-}0\text{--}000_B$
32_H	PCR2	PWC control register 2	R/W	00000000_B
33_H	PLBR	PWC reload buffer register	R/W	$XXXXXXXX_B$

(Continued)

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
34H	CNTR	PWM timer control register	R/W	0-000000B
35H	COMR	PWM timer compare register	W*	XXXXXXXXB
36H	T4CR	Timer 22 control register	R/W	000000X0B
37H	T3CR	Timer 21 control register	R/W	000000X0B
38H	T4DR	Timer 22 data register	R/W	XXXXXXXXB
39H	T3DR	Timer 21 data register	R/W	XXXXXXXXB
3AH	T2CR	Timer 12 control register	R/W	000000X0B
3BH	T1CR	Timer 11 control register	R/W	000000X0B
3CH	T2DR	Timer 12 data register	R/W	XXXXXXXXB
3DH	T1DR	Timer 11 data register	R/W	XXXXXXXXB
3EH	PPGC1	PPG control register 1	R/W	00000000B
3FH	PPGC2	PPG control register 2	R/W	0-000000B
40H	BUZR	Buzzer control register	R/W	-----000B
41 to 5DH	(Reserved)			
5EH	LCR1	LCD controller control register 1	R/W	00010000B
5FH	LCR2	LCD controller control register 2	R/W	-0000000B
60 to 6FH	VRAM	LCD data RAM	R/W	XXXXXXXXB
70H	PURC0	Port 0 pull up resistor control register	R/W	11111111B
71H	(Reserved)			
72H	PURC2	Port 2 pull up resistor control register	R/W	----1111B
73H to 76H	(Reserved)			
77H	(Reserved)			
78H	(Reserved)			
79H	(Reserved)			
7AH	(Reserved)			
7BH	ILR1	Interrupt level setting register 1	W*	11111111B
7CH	ILR2	Interrupt level setting register 2	W*	11111111B
7DH	ILR3	Interrupt level setting register 3	W*	11111111B
7EH	ILR4	Interrupt level setting register 4	W*	11111111B
7FH	(Reserved)			

* Bit manipulation instruction cannot be used.

● **Read/write access symbols**

R/W : Readable and writable
R : Read-only
W : Write-only

● **Initial value symbols**

0: The initial value of this bit is “0”.
1: The initial value of this bit is “1”.
X: The initial value of this bit is undefined.
- : Unused bit.
M: The initial value of this bit is determined by mask option.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	MB89PV480, MB89P485, MB89485 AV_{CC} must not exceed V_{CC}
	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	MB89P485L, MB89485L AV_{CC} must not exceed V_{CC}
LCD Power supply voltage	V0 to V3	V_{SS} – 0.3	V_{SS}+ 6.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P47, P50 to P56
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min.	Max.			
Power supply voltage	V_{CC} AV_{CC}	2.2*	5.5	V	Operation assurance range	MB89485
		3.5*	5.5	V	Operation assurance range	MB89P485
		2.7*	5.5	V	Operation assurance range	MB89PV480
		1.5	5.5	V	Retains the RAM state in stop mode	MB89485, MB89P485, MB89PV480
		2.2*	3.6	V	Operation assurance range	MB89485L, MB89P485L
		1.5	3.6	V	Retains the RAM state in stop mode	
LCD power supply voltage	V0 to V3	Vss	Vcc	V		
Operating temperature	T_A	–40	+85	°C		

* : These values depend on the operating conditions and the analog assurance range. See Figure 1,2 and "5. A/D Converter Electrical Characteristics."

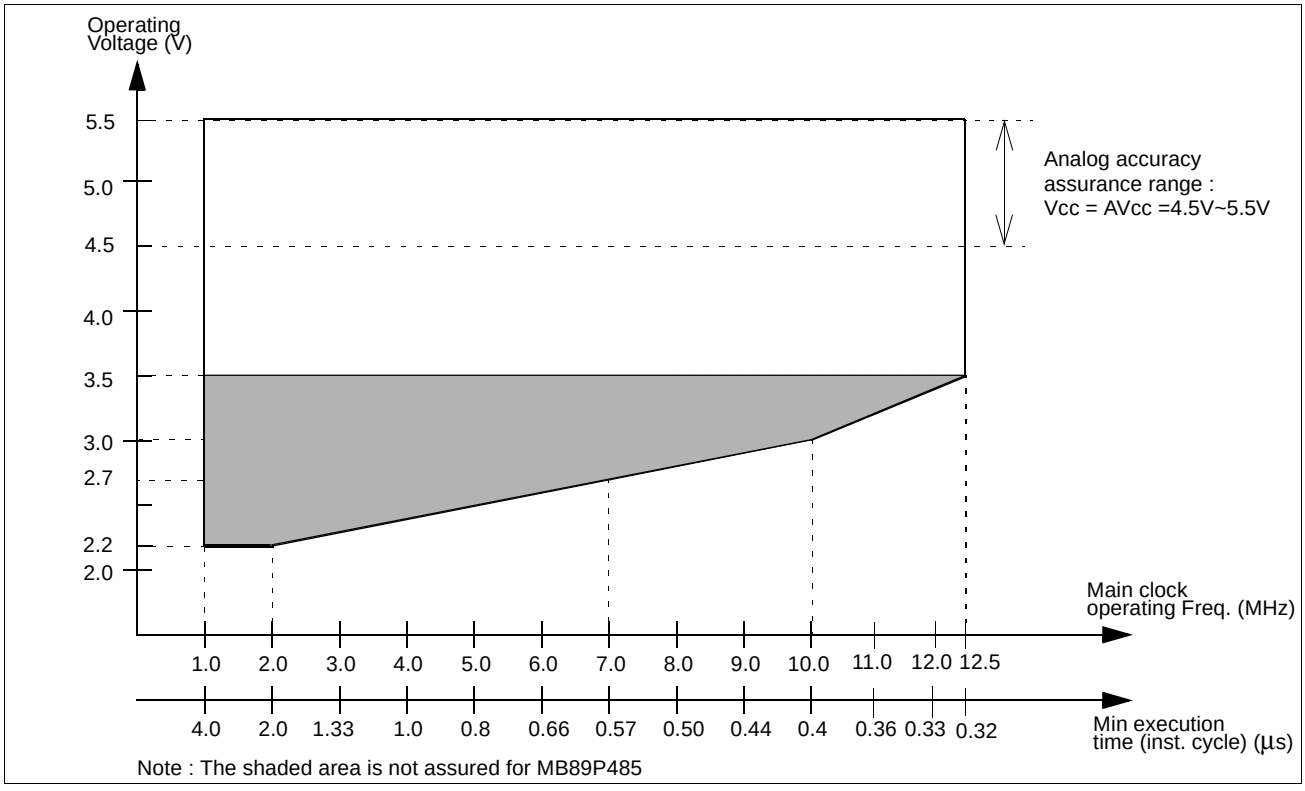


Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MB89P485/485)

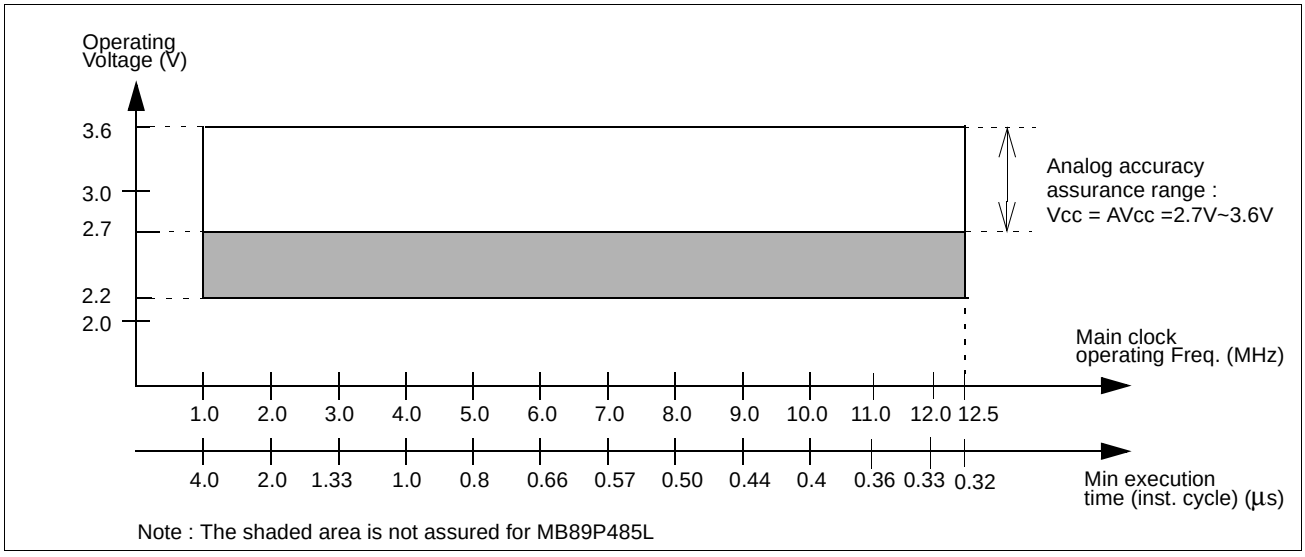


Figure 2 Operating Voltage vs. Main Clock Operating Frequency (MB89P485L/485L)

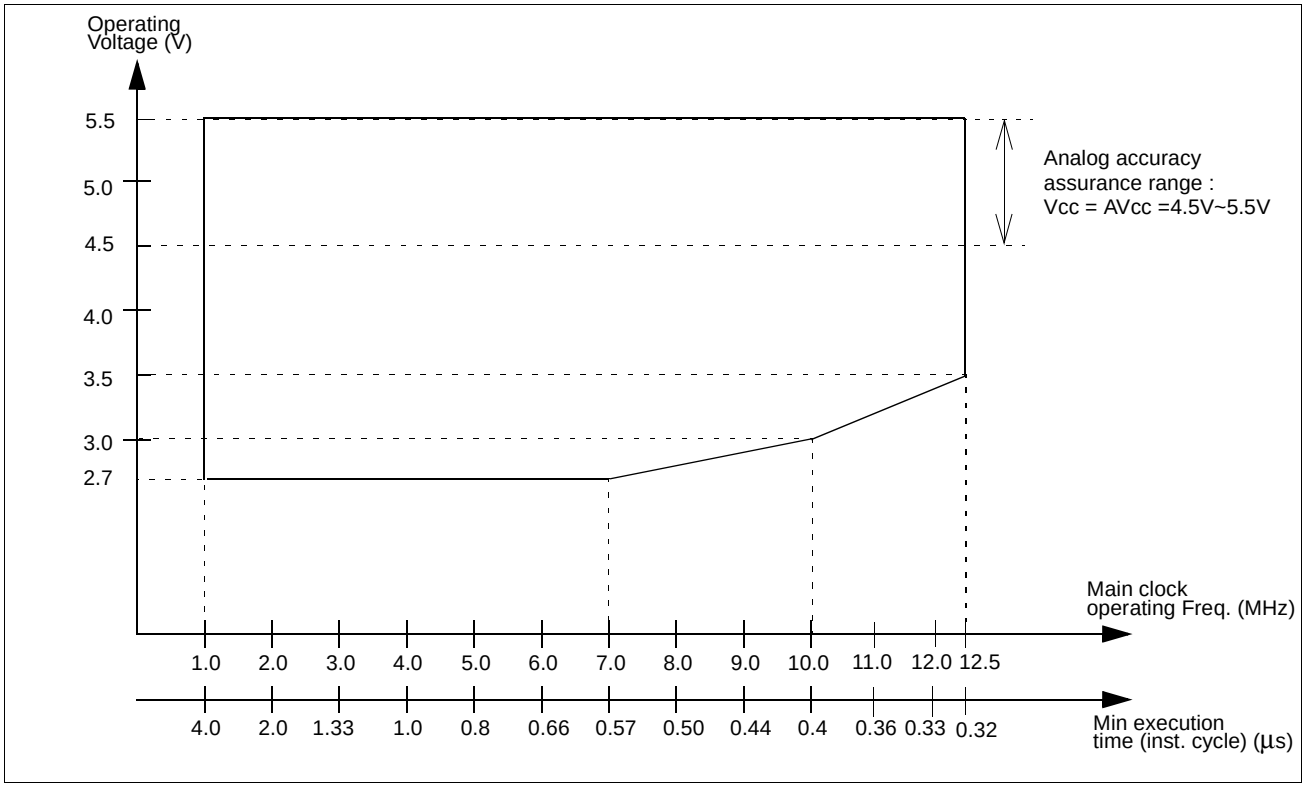


Figure 3 Operating Voltage vs. Main Clock Operating Frequency (MB89PV480)

Figure 1,2 and 3 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

$AV_{CC} = V_{CC} = 5.0$ V for MB89PV480, MB89P485, MB89485
$AV_{CC} = V_{CC} = 3.0$ V for MB89P485L, MB89485L

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P40 ~ P47, P50 ~ P57	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MODE, EC1, EC2, PWC, SCK, SI, INT10 ~ INT13, INT20 ~ INT27	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P40 ~ P47, P50 ~ P57	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MODE, EC1, EC2, PWC, SCK, SI, INT10 ~ INT13, INT20 ~ INT27	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P10 ~ P17, P24 ~ P27, P30 ~ P31, P40 ~ P47, P50 ~ P56	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	Product without booster
						V3		Product with booster
"H" level output voltage	V_{OH}	P00 ~ P07, P20 ~ P23	I_{OH} = –2.0mA	4.0	—	—	V	MB89PV480 MB89P485 MB89485
				2.2	—	—	V	MB89P485L MB89485L
"L" level output voltage	V_{OL}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P31, P40 ~ P47, P50 ~ P56, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 ~ P07, P10 ~ P17, P20 ~ P27, P40 ~ P47, P50 ~ P57	0.45 V < V_I < V_{CC}	-5	—	+5	µA	Without pull-up resister
Open-drain output leakage current	I_{LOD}	P10 ~ P17, P24 ~ P27, P30 ~ P31, P40 ~ P47, P50 ~ P56	0.45 V < V_I < V_{CC}	-5	—	+5	µA	

(Continued)

(Continued)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-down resistance	R_{DOWN}	MODE	$V_I = V_{CC}$	25	50	100	kΩ	Except MB89P485, MB89P485L
Pull-up resistance	R_{PULL}	P00 ~ P07, P20 ~ P23, RST	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor is selected (except RST)
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +3.0 V	—	—	2.5	kΩ	MB89P485L, MB89485L
			V1 to V3 = +5.0 V					MB89PV480, MB89P485, MB89485
Segment output impedance	R_{VSEG}	SEG0 to SEG30	V1 to V3 = +3.0 V	—	—	15	kΩ	MB89P485L, MB89485L
			V1 to V3 = +5.0 V					MB89PV480, MB89P485, MB89485
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V_{SS}	300	500	750	kΩ	
LCD controller/ driver leakage current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG30	—	—	—	±1	μA	
Booster for LCD driving output voltage	V_{V3}	V3	V1 = 1.5V	4.3	4.5	4.7	V	Products with booster only
	V_{V2}	V2	V1 = 1.5V	2.9	3.0	3.1	V	
Reference input voltage for LCD driving	V_{V1}	V1	I_{IN} = 0 μA	1.4	1.5	1.7	V	
Reference voltage input impedance	R_{RIN}	V1	—	8.5	9.8	11	kΩ	
Input capacitance	C_{IN}	Other than V_{CC},V_{SS},AV_{CC},AV_{SS}	f=1MHz	—	10	—	pF	

(Continued)

(Continued)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CC1}	V_{CC}	F_{CH} = 12.5MHz t_{inst} = 0.32 µs Main clock run mode	—	8	13	mA	
	I_{CC2}		F_{CH} = 12.5MHz t_{inst} = 5.12 µs Main clock run mode	—	0.7	3	mA	
	I_{CCS1}		F_{CH} = 12.5MHz t_{inst} = 0.32 µs Main clock sleep mode	—	2.5	5	mA	
	I_{CCS2}		F_{CH} = 12.5MHz t_{inst} = 5.12 µs Main clock sleep mode	—	0.4	2	mA	
	I_{CCL}		F_{CL} = 32.768kHz Subclock mode	—	50	85	µA	Except MB89P485
				—	54	91	µA	MB89P485
	I_{CCLS}		F_{CL} = 32.768kHz Subclock sleep mode	—	15	30	µA	Except MB89P485
				—	19	36	µA	MB89P485
	I_{CCT}		F_{CL} = 32.768kHz • Watch mode	—	1.6	15	µA	Except MB89P485
			• Main clock stop mode	—	5.6	21	µA	MB89P485
	I_{CCH}		Ta=+25°C Subclock stop mode	—	3	10	µA	
	I_A	AV_{cc}	Ta=+25°C	—	4	6	mA	A/D converting
	I_{AH}			—	1	5	µA	A/D stop

4. AC Characteristics

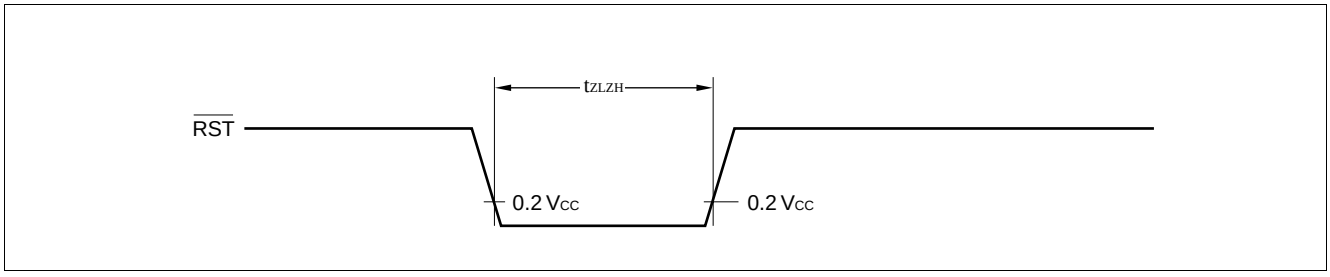
(1) Reset Timing

V_{CC} = 5.0 V for MB89PV480, MB89P485, MB89485
V_{CC} = 3.0 V for MB89P485L, MB89485L

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

Note: t_{HCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.
The MCU operation is not guaranteed when the "L" pulse width is shorter than t_{ZLZH}.

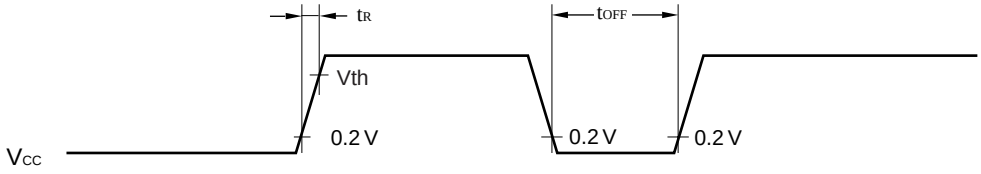


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



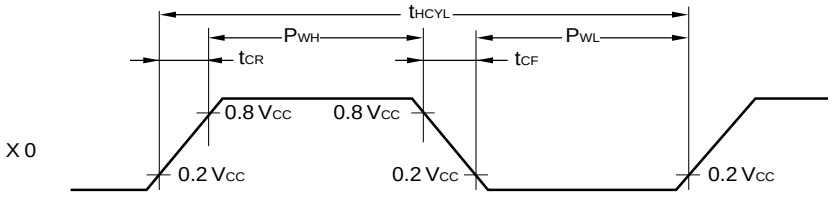
Vth = 3.5 V for MB89PV480, MB89P485 and MB89485
Vth = 1.8 V for MB89P485L and MB89485L

(3) Clock Timing

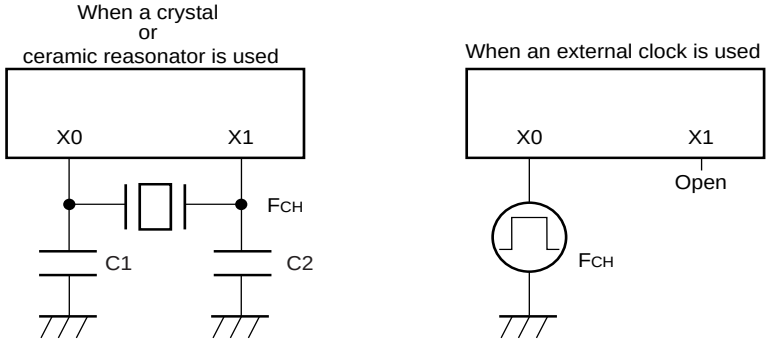
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	
	F_{CL}	X0A, X1A	—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	15.2	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	

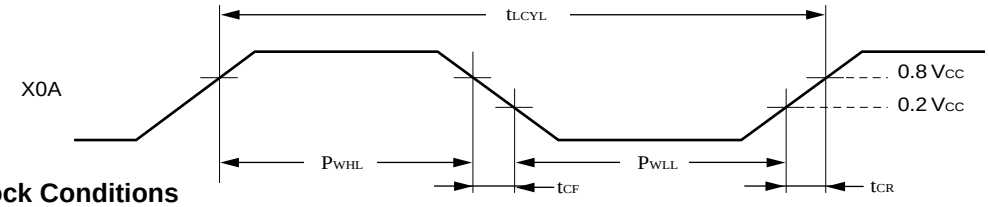
X0 and X1 Timing and Conditions



Main Clock Conditions

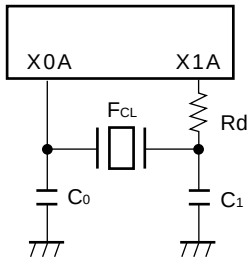


Subclock Timing and Conditions

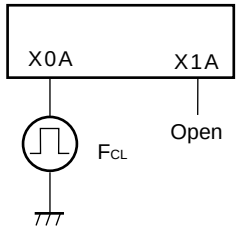


Subclock Conditions

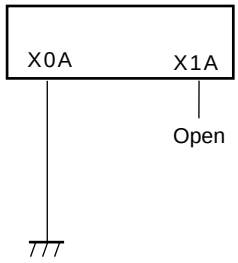
When a crystal or ceramic oscillator is used



When an external clock is used



When subclock is not used



(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})t_{inst}$ = 0.32 µs when operating at F_{CH} = 12.5 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

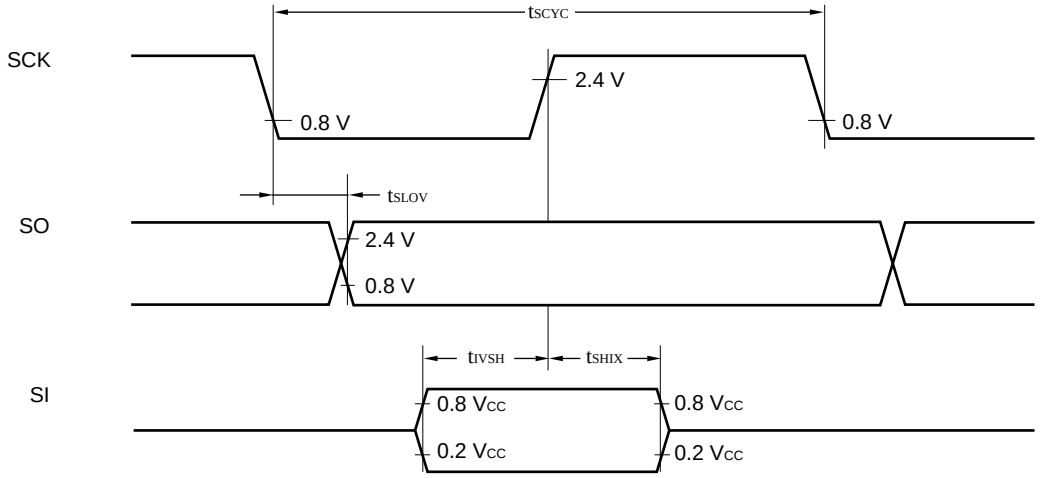
(5) Serial I/O Timing

V_{CC} = 5.0 V for MB89PV480, MB89P485, MB89485 ,V_{CC} = 3.0 V for MB89P485L, MB89485L
(AV_{SS} = V_{SS}= 0.0 V, T_A = –40°C to +85°C)

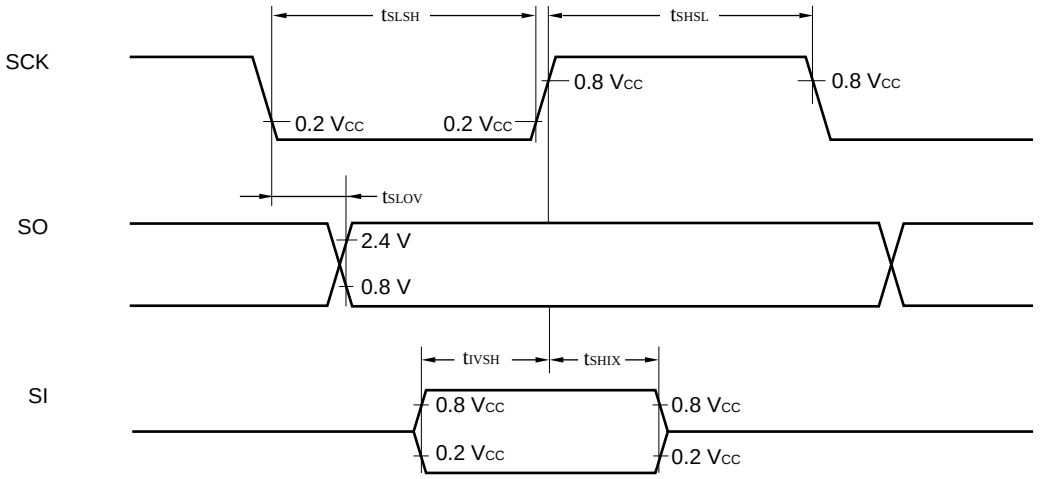
Parameter	Symbol	Pin	Condition	Value		Unit
				Min.	Max.	
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	ns

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Clock Operation



External Clock Operation

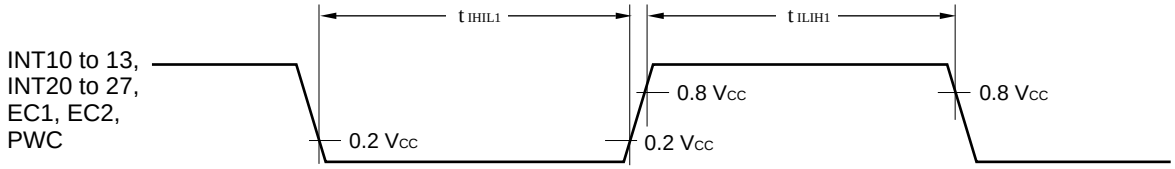


(6) Peripheral Input Timing

V_{CC} = 5.0 V for MB89PV480, MB89P485, MB89485
V_{CC} = 3.0 V for MB89P485L, MB89485L
(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	$\underline{INT10}$ ~ 13, $\overline{INT20}$ ~ $\overline{INT27}$, EC1, EC2, PWC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 4.5$ V ~ 5.5 V for MB89PV480, MB89P485, MB89485,
$AV_{CC} = V_{CC} = 2.7$ V ~ 3.6 V for MB89P485L, MB89485L,
$AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

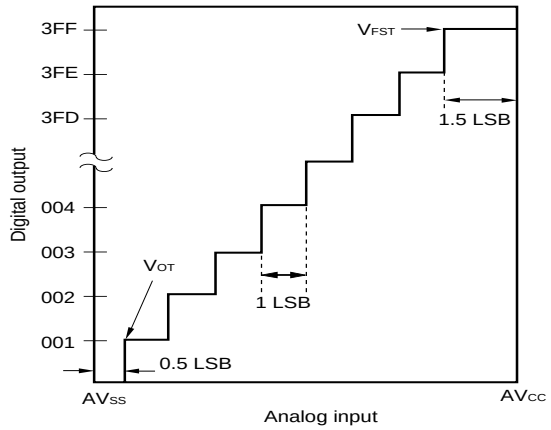
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	—	bit	
Total error			—	—	±3.0	LSB	
Linearity error			—	—	±2.5	LSB	
Differential linearity error			—	—	±1.9	LSB	
Zero transition voltage	V_{OT}		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	LSB	
Full-scale transition voltage	V_{FST}		AV_{CC} – 3.5 LSB	AV_{CC} – 1.5 LSB	AV_{CC} + 0.5 LSB	LSB	
A/D mode conversion time	—		—	—	60 tinst*	µs	
Analog port input current	I_{AIN}	AN0 to AN3	—	—	10	µA	
Analog input voltage	V_{AIN}		AV_{SS}	—	AV_{CC}	V	

* : For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics".

(2) A/D Converter Glossary

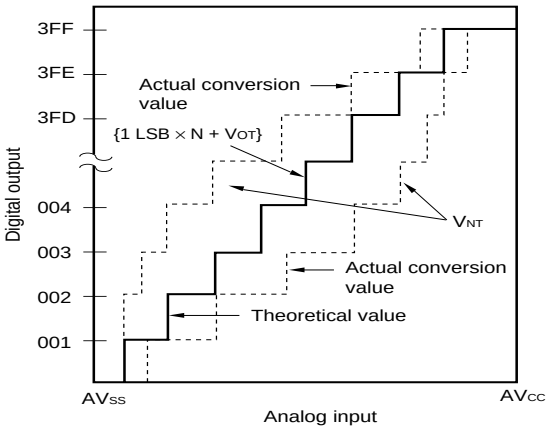
- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics.
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values.

Theoretical I/O characteristics



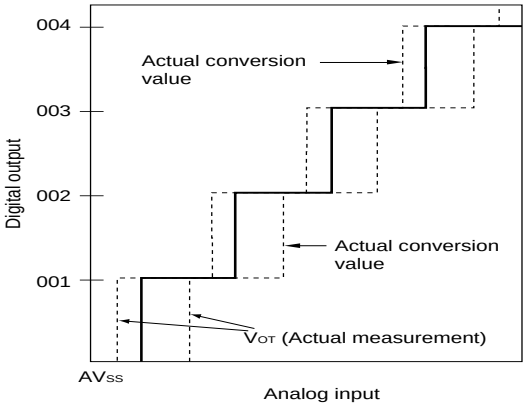
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

Total error

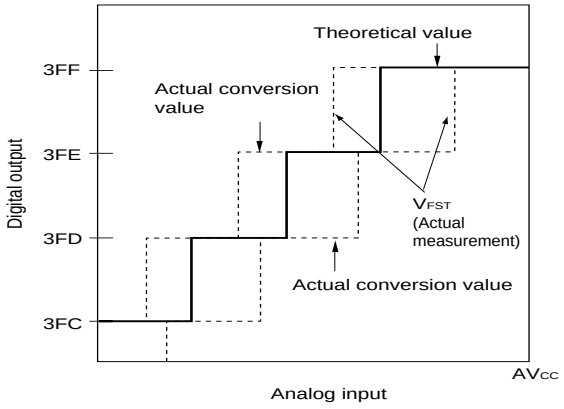


$$\text{Total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

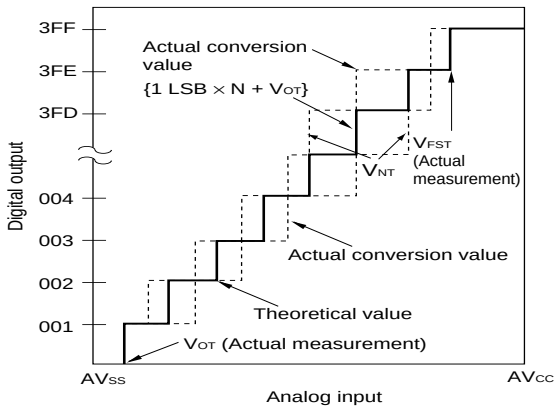
Zero transition error



Full-scale transition error

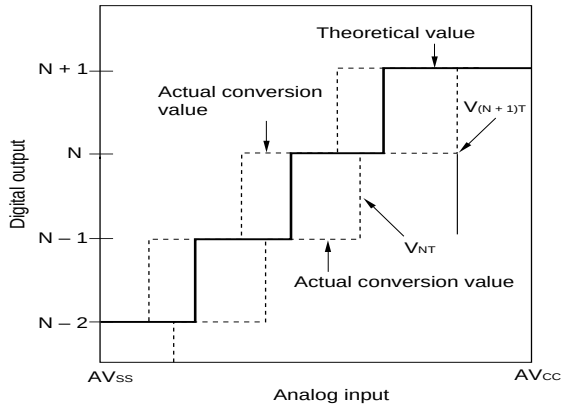


Linearity error



$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

Differential linearity error



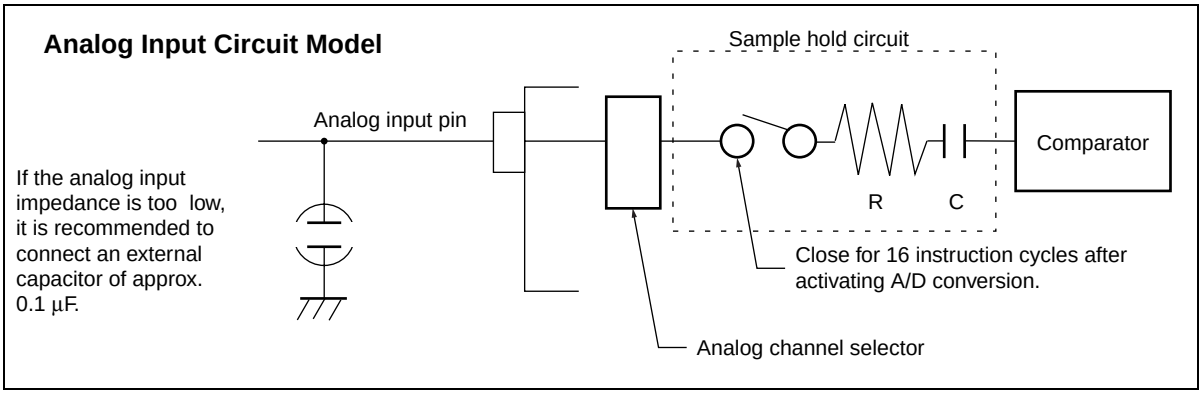
$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

(3) Notes on Using A/D Converter

- Input impedance of the analog input pins
  The A/D converter used for the MB89470 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 16 instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low.

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.



	MB89485 MB89PV480	MB89485L	MB89P485	MB89P485L
R: analog input equivalent resistance	2.2 kΩ	7.1 kΩ	2.6 kΩ	2.8 kΩ
C: analog input equivalent capacitance	45 pF	48.3 pF	28 pF	46 pF

- Error
  The smaller the |AVR - AV_{SS}|, the greater the error would become relatively.

■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

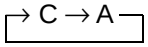
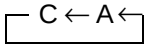
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

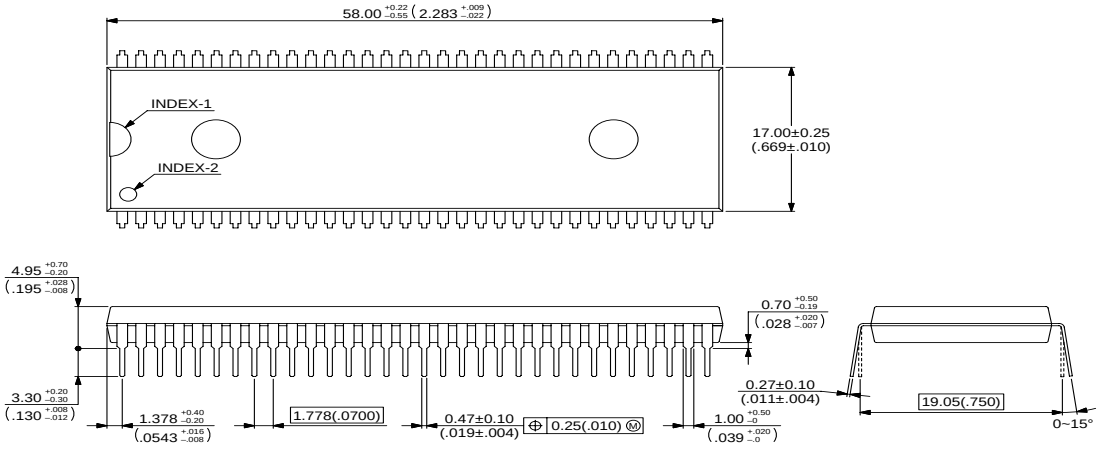
No.	Part number	MB89485	MB89485L	MB89P485	MB89P485L	MB89PV480
	Specifying procedure	**Specify when ordering masking**		**Setting not possible**		**Setting not possible**
1	Booster selection (KSV) • Internal resistor ladder • Booster	Selectable		101: Internal resistor ladder 102: Booster		101: Internal resistor ladder 102: Booster
2	Selection of OTPROM content protection feature • No protection feature • With protection feature	--		101/102: No protection 103/104: with protection		--
3	Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bits on the right.	Selectable OSC 1 : $2^{14}/F_{CH}$ 2 : $2^{17}/F_{CH}$ 3 : $2^{18}/F_{CH}$		Fixed to oscillation stabilization time of $2^{18}/F_{CH}$		Fixed to oscillation stabilization time of $2^{18}/F_{CH}$
4	Selection of power-on stabilization time • Nil • $2^{17}/F_{CH}$	Selectable	Fixed to nil	$2^{17}/F_{CH}$	Fixed to nil	Fixed to nil

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89485PFM MB89P485PFM-101 MB89P485PFM-102 MB89P485PFM-103 MB89P485PFM-104 MB89485LPFM MB89P485LPFM-101 MB89P485LPFM-102 MB89P485LPFM-103 MB89P485LPFM-104	64-pin Plastic QFP (FPT-64P-M09)	101: With internal resistor ladder, without content protection 102: With booster, without content protection 103: With internal resistor ladder, with content protection 104: With booster, with content protection
MB89485P-SH MB89P485P-SH-101 MB89P485P-SH-102 MB89P485P-SH-103 MB89P485P-SH-104 MB89485LP-SH MB89P485LP-SH-101 MB89P485LP-SH-102 MB89P485LP-SH-103 MB89P485LP-SH-104	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89PV480CF-101 MB89PV480CF-102	64-pin Ceramic MQFP (MQP-64C-P01)	

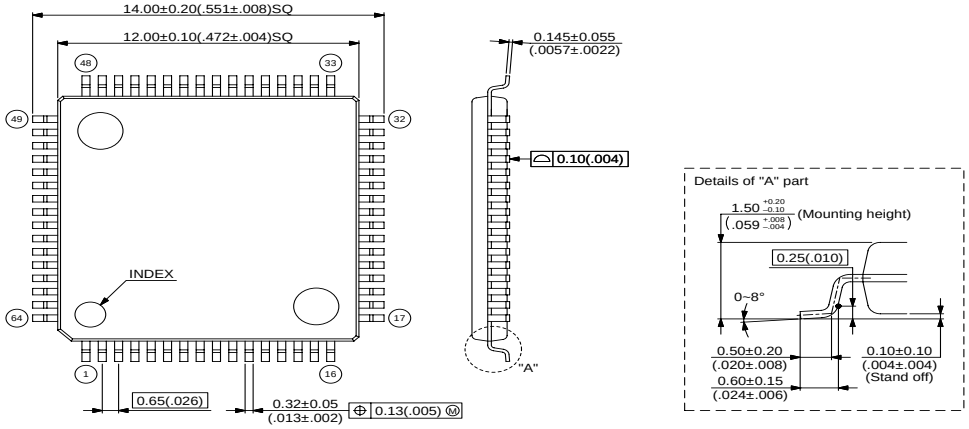
■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
DIP-64P-M01



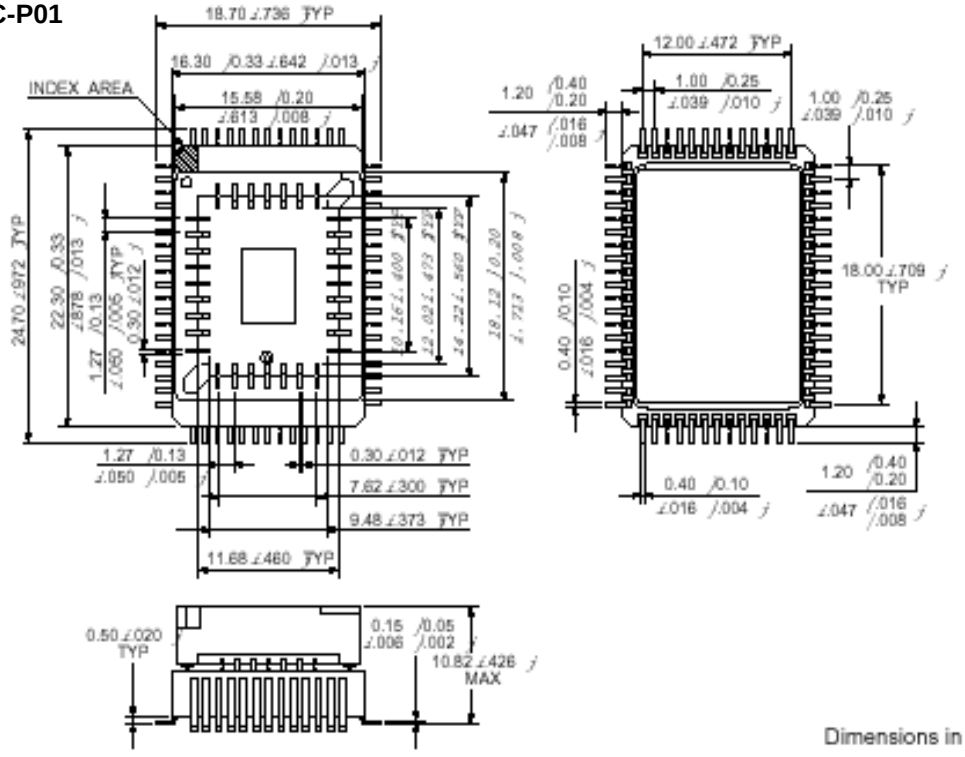
Dimensions in mm (inches)

64-pin Plastic LQFP
FPT-64P-M09



Dimensions in mm (inches)

64-pin Ceramic MQFP
MQP-64C-P01



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