DESCRIPTION

The LX1810 is a Full-Bridge thermo-electric cooler (TEC) controller specifically designed for high performance opto-electronic products where precise temperature control is required. These products tune or stabilize sensitive optical components in applications that include frequency tunable fiber optic lasers, EDFA amplifiers, waveguides, and other dense wavelength division multi-plexing (DWDM) components. Other applications include microwave transistors in new wireless base-stations.

The LX1810 uses highly efficient (>90%) pulse width modulation (PWM) technology, allowing the controller to be conveniently mounted near the TEC without adding heat to the system. The LX1810 operates on a single voltage supply, greatly simplifying supply requirements, with an operating frequency that is high enough to eliminate detrimental thermal stresses to the TEC. The output ripple factor of the system can be maintained well below 10% thus not effecting the performance of delta T control.

Utilizing a full-bridge topology, the LX1810 can be used for both heating and cooling operations. The LX1810, when used in conjunction with a temperature sense device, accurately regulates TEC current levels allowing tight control of temperature.

Fully integrated FET drivers in a 28-Pin SSOP allows the design of a fully functional TEC controller while minimizing board space.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

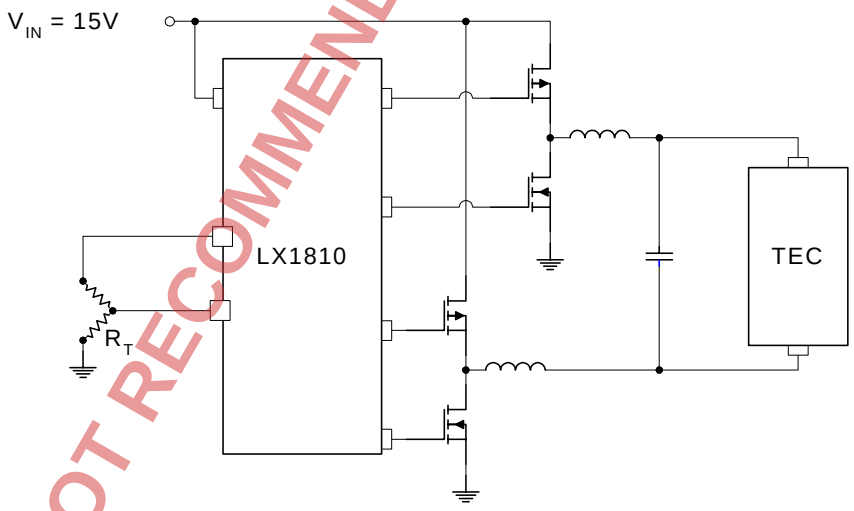
KEY FEATURES

- Integrated Switching Full-Bridge PWM Drive Architecture
- Single DC Supply Operation
- Very Low Output Noise
- Maximum Efficiency 90%
- High Output Integrated Drivers
- PSRR –70dB Typical
- Differential Input To Minimize Noise
- External Oscillator Synchronization
- 28-Pin SSOP Package

APPLICATIONS/BENEFITS

- Peltier Effect (Thermoelectric Coolers) Controllers
- High Efficiency H-Bridge Drive Circuits
- RF Power Amplifier Electronic Cooling
- CPU Electronic Cooling

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	DB Plastic SSOP 28-Pin
0 to 70	LX1810-CDB

Note: Available in Tape & Reel.
Append the letter "T" to the part number. (i.e. LX1810-CDBT)

Rev. 1.0a, 10/21/2002

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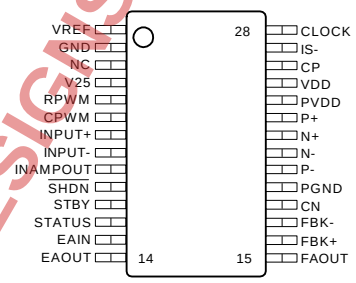
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (PVDD, VDD) ..... -0.3V to 15V
SLEEP, STATUS, FBK+, FBK- ..... -0.3V to V_{DD} +0.3V
IS- ..... PV_{DD} –2 to PV_{DD} to +0.3V
RPWM, CPWM, MUTE ..... -0.3V to V_{REF}+0.3V
INPUT +, INPUT -, INAMPOUT ..... -0.3V to V_{REF}+0.3V
EAIN, EAOUT, FAOUT ..... -0.3V to V_{REF}+0.3V
CLOCK ..... -0.3V to C_N +0.3V
Operating Junction Temperature Plastic (DB Package) ..... 125°C
Storage Temperature Range ..... -65 °C to 150 °C
Lead Temperature (Soldering, 10 seconds) ..... 300 °C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



THERMAL DATA

DB **Plastic SSOP 28-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	50°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
VREF	5V Reference	**FAOUT**	Feedback Amplifier Output
GND	Low Current Ground	**FBK+**	Feedback Amplifier Non-Inverting Input
NC	No Internal Connection	**FBK-**	Feedback Amplifier Inverting Input
V25	2.5V Reference	**CN**	Supply Decoupling for NFET Drivers
RPWM	PWM Oscillator Timing Resistor	**PGND**	Output Driver High Current Ground
CPWM	PWM Oscillator Timing Capacitor	**P-**	Drive for PFET on Negative Half of Bridge
INPUT+	Positive Differential Amplifier Input	**N-**	Drive for NFET on Negative Half of Bridge
INPUT -	Negative Differential Amplifier Input	**N+**	Drive for NFET on Positive Half of Bridge
INAMPOUT	Input Differential Amplifier Output	**P+**	Drive for PFET on Positive Half of Bridge
$\overline{\text{SHDN}}$	IC Shutdown Control Input (active low)	**PVDD**	Output Driver Supply Voltage
STBY	IC Standby Control Input (active high)	**VDD**	Analog Supply Voltage
STATUS	UVLO Indicator (Open Collector Output)	**CP**	Supply Decoupling for PFET Drivers
EAIN	Inverting Input of Error Amplifier	**IS -**	Current Limit Sense Input
EAOUT	Error Amplifier Output	**CLOCK**	Input / Output Clock for Synch Operation

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C < TA < 70°C.
Test conditions: RPWM = 49.9k, CPWM = 100pF, VDD = PVDD = 15V

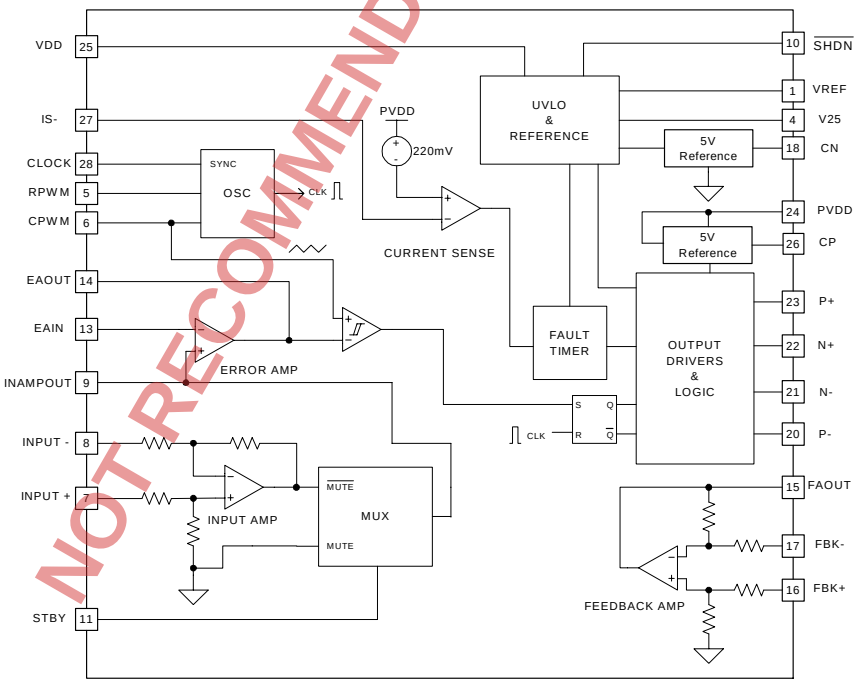
Parameter	Symbol	Test Conditions	LX1810 Min	LX1810 Typ	LX1810 Max	Units
Supply Voltage						
Supply Voltage	V_{DD}		7		15	V
Power Supply Rejection Ratio	PSRR	V_{IN} = 15V, V_{RIPPLE} = $1V_{RMS}$, 10Hz to 10kHz		-70		dB
Oscillator Section						
Oscillator Frequency	F_{OSC}			335		kHz
Charge Current	I_{CHG}	(varies with V_{DD} pin voltage)		-110		µA
Discharge Current	I_{DIS}	(varies with V_{DD} pin voltage)		110		µA
Oscillator Peak Voltage	V_{PK}	(varies with V_{DD} pin voltage)		3.4		V
Oscillator Valley Voltage	V_{VAL}	(varies with V_{DD} pin voltage)		1.6		V
Voltage Stability		V_{DD} = 8V to 15V		0.6	2	%
Temperature Stability		T_A = 0°C to 70°C		1.0	2	%
		T_A = -40°C to 125°C		1.5		%
Error Amplifier						
Input Offset Voltage	V_{IO}			5		mV
DC Open Loop Gain	A_{OL}			60		dB
Unity Gain Bandwidth	UGBW			7		mHz
High Output Voltage	V_{OH}	I_{OUT} = -100µA	V_{REF} –1			V
Low Output Voltage	V_{OL}	I_{OUT} = +100µA			50	mV
Input Common Mode Range						
Input Bias Current	I_{IN}	V_{IN} = 1V to V_{REF}			1	µA
Input Amplifier						
Stage Gain		Set by Internal Resistors	3.465	3.5	3.535	V/V
Output Voltage, High	V_{OH}	I_{OUT} = -100µA	3.85			V
Output Voltage, Low	V_{OL}	I_{OUT} = +100µA			1.3	mV
Input Impedance				42		kΩ
Feedback Amplifier						
Stage Gain		Set by Internal Resistors	89	91	93	mV/V
Input Impedance				388		kΩ
Current Limit Comparator						
Voltage Sense Threshold			190	210	230	mV
Blanking Pulse Delay				500		ns
Response Time		Excluding blanking pulse		250		ns
I_{UM} Pulses required to Current Limit Latch		(Required Number of Clock Cycles)	9	9	9	
Consecutive Clear Pulses required to reset I_{UM} counter		(Required Number of Clock Cycles)	2	2	2	
Reference Voltage Section						
Initial Accuracy				5.000		
Voltage Stability				± 25	± 50	mV
Temperature Stability		T_A = 0°C to 70°C		2	5	mV
		T_A = -40°C to 125°C		4	10	mV
Line Regulation		V_{DD} = 9V to 15V		0.5		mV
Load Regulation		I_{OUT} = 0 to 20mA		5		mV
Under voltage Lockout Section						
Start Threshold Voltage				6.5		V
UV Lockout Hysteresis			0.5	6.5		V
UVLO Delay To Output Enable		(Required Number of Clock Cycles)		62,500		

ELECTRICAL CHARACTERISTICS (CONT)

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C < TA < 70°C.
Test conditions: RPWM = 49.9k, CPWM = 100pF, VDD = PVDD = 15V

Parameter	Symbol	Test Conditions	LX1810 Min	LX1810 Typ	LX1810 Max	Units
Supply Current						
$\overline{SHDN}$ Current		$\overline{SHDN}$ Input = 0V, T_A = 25°C		25		µA
Operating Current		$\overline{SHDN}$ Input = 2V, V_{IN} = 15V, No MOSFETs connected		2.9	5.0	mV
$\overline{SHDN}$ to Output Enable		(Required Number of Clock Cycles)		62,500		
$\overline{SHDN}$ Threshold			1.2	1.45	1.6	V
Standby Section						
Standby Threshold			1.6	1.7	1.8	V
Output Drivers for N-Channel MOSFETs						
NFET Drivers, Low Level Voltage	V_{OL}	I_{SINK} = 3mA		30	100	mV
		I_{SINK} = 75mA		1.5	2.0	V
NFET Drivers, High Level Voltage	V_{OH}	I_{SOURCE} = 3mA, C_N = 5.2V applied externally		30	100	mV
		I_{SOURCE} = 75mA, C_N = 5.2V applied externally		1.5	2.0	V
Output Drives For P-Channel MOSFETs						
PFET Drivers, Low Level Voltage	V_{OL}	I_{SINK} = 3mA		30	100	mV
		I_{SINK} = 75mA		1	1.5	V
PFET Drivers, High Level Voltage	V_{OH}	I_{SOURCE} = 3mA, C_P = 5.2V (applied externally)		30	100	mV
		I_{SOURCE} = 75mA, C_P = 5.2V (applied externally)		1	1.5	V

BLOCK DIAGRAM



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NOTES

DB 28-Pin Shrink Small Outline Package SSOP

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Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.65	1.85	0.065	0.073
B	0.25	0.38	0.009	0.015
C	0.13	0.22	0.005	0.008
D	9.90	10.50	0.390	0.413
E	5.00	5.60	0.197	0.221
F	0.65 BSC		0.025 BSC	
G	0.05	0.21	0.002	0.008
H	1.73	2.00	0.068	0.078
L	0.65	0.95	0.025	0.037
M	0°	8°	0°	8°
P	7.65	7.90	0.301	0.311
*LC	–	0.10	–	0.004

*Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES