HFCT-5801

155 Mb/s Single Mode Fiber Transceiver
for ATM, SONET OC-3/SDH STM-1
Part of the Avago Technologies METRAK family

Data Sheet

Description

General

The HFCT-5801 transceiver is a high performance, cost effective module for serial optical data communications applications specified for a data rate of 155 Mb/s. It is designed to provide a SONET/SDH compliant link for intermediate reach links operating at +3.3 V input voltage.

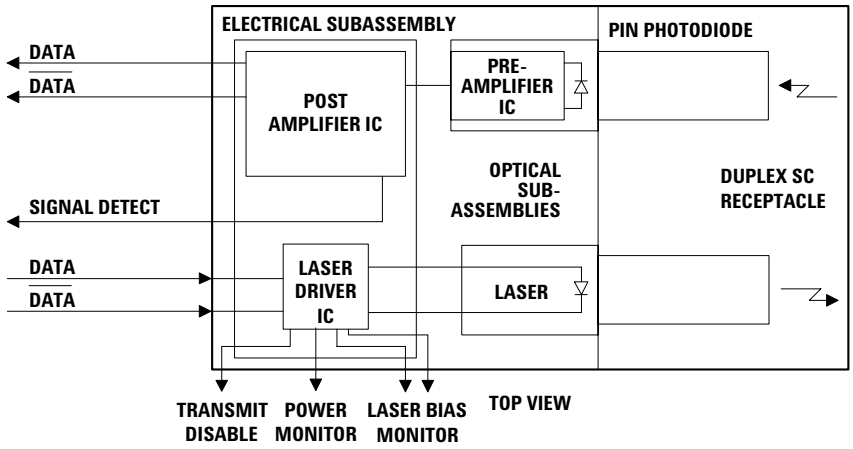
The multisourced 2 x 9 footprint package style is a variation of the standard 1 x 9 package with an integral Duplex SC connector receptacle. The extra row of 9 pins provides connections for laser bias and optical power monitoring as well as providing transmitter disable function. A block diagram is shown in Figure 1.

Applications

- ATM 155 Mb/s links for LAN backbone switches and routers
- ATM 155 Mb/s links for WAN core, edge and access switches and routers
- ATM 155 Mb/s links for add/drop multiplexers and demultiplexers
- SONET OC-3/SDH STM-1 (S-1.1) interconnections

Features

- 1300 nm Single mode transceiver for links up to 15 Km
- Compliant with T1.646-1995 Broadband ISDN and T1E1.2/98-011R1 SONET network to customer installation interface standards
- Compliant with T1.105.06 SONET physical layer specifications standard
- Multisourced 2 x 9 pin-out package style derived from 1 x 9 pin-out industry standard package style
- Unconditionally eyesafe laser IEC 825/CDRH Class 1 compliant
- Integral duplex SC connector receptacle compatible with TIA/EIA and IEC standards
- Laser bias monitor, power monitor and transmitter disable functions compliant with SONET objectives
- Two temperature ranges:
  0°C - +70°C HFCT-580IB/D
  -40°C - +85°C HFCT-5801A/C
- Single +3.3 V power supply operation and compatible LVPECL logic interfaces
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9002 certified facility
- Considerable EMI margin to FCC Class B



Transmitter Section

The transmitter section of the HFCT-5801 consists of a 1300 nm InGaAsP laser in an eyesafe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a custom IC which converts differential input LVPECL logic signals into an analog laser drive current. The laser bias monitor circuit is shown in Figure 2a, the power monitor circuit in Figure 2b.

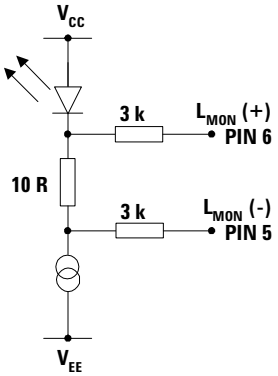


Figure 2a. Laser Bias Monitor

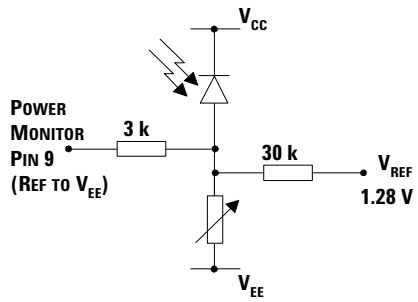


Figure 2b. Power Monitor Circuit

Receiver Section

The receiver utilizes an InGaAs PIN photodiode mounted together with a transimpedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

Receiver Signal Detect

Signal Detect is a basic fiber failure indicator. This is a single-ended LVPECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 0.5 dB higher than the deassert level.

Transceiver Specified for Wide Temperature Range Operation

The HFCT-5801 is specified for operation over normal commercial temperature range of 0° to +70°C (HFCT-5801B/D) or the extended temperature range of -40° to +85°C (HFCT-5801A/C). Characterization of the parts has been performed over the ambient operating temperature range in an airflow of 2 m/s.

Other Members of Avago SC Duplex 155 Mb/s Product Family

- HFCT-5805, 1300 nm single mode transceiver for links up to 15 km. The part is based on the 1 x 9 industry standard package and has an integral duplex SC connector receptacle

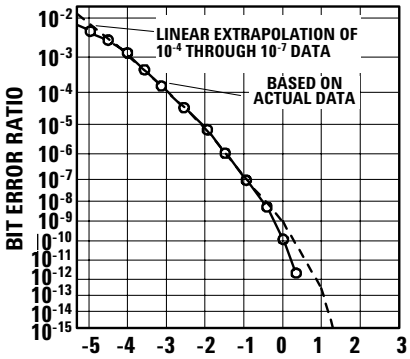


Figure 3. Relative Input Optical Power - dBm. Avg.

Applications Information

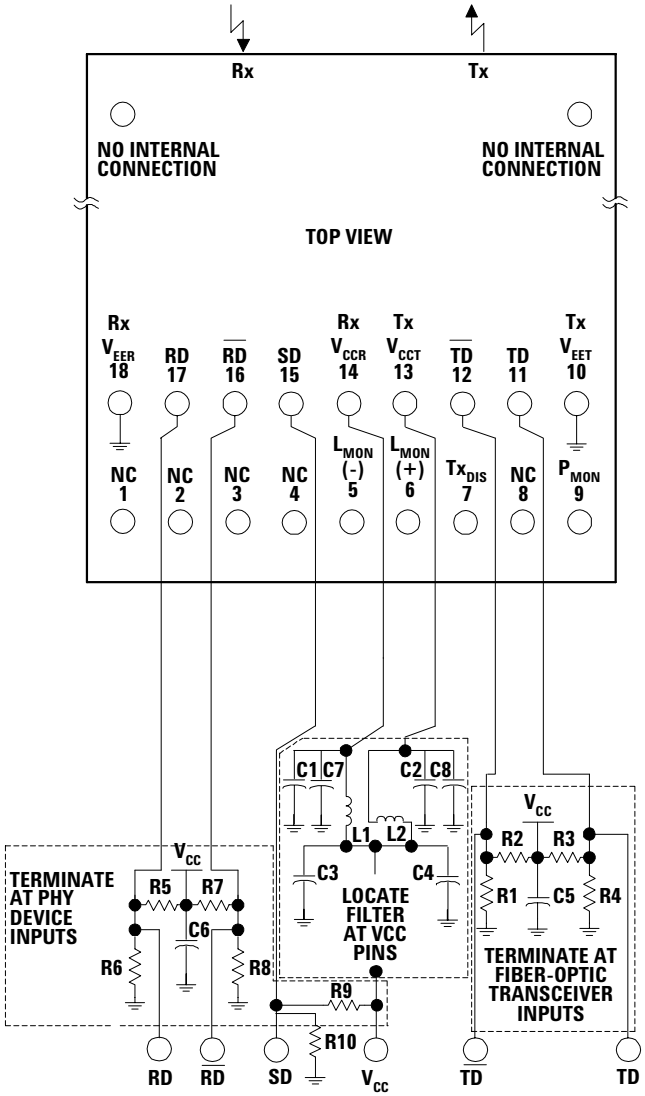
Typical BER Performance of Receiver versus Input Optical Power Level

The HFCT-5801 transceiver can be operated at Bit-Error-Rate conditions other than the required BER = 1 x 10-10 of the ATM Forum 155.52 Mb/s Physical Layer Standard. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 3. The Relative Input Optical Power in dB is referenced to the actual sensitivity of the device. For BER conditions better than 1 x 10-10, more input signal is needed (+dB).

Recommended Circuit Schematic

In order to ensure proper functionality of the HFCT-5801 a recommended circuit is provided in Figure 4. When designing the circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic figure the differential data lines should be treated as 50 ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data signals will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length. For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer plane printed circuit board is best for distribution of VCC, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit. Proper power supply filtering of VCC for this transceiver is accomplished by using the recommended, separate filter circuits shown in Figure 4 for the transmitter and receiver sections. These filter circuits suppress VCC noise over a broad frequency range, this prevents receiver sensitivity degradation due to VCC noise. It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and monolithic, ceramic bypass capacitors for the 0.1 µF capacitors. Also, it is recommended that a surface- mount



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR LVPECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE LVPECL SIGNALS. RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 W MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 82
R2 = R3 = R5 = R7 = R9 = 130
C1 = C2 = 10 µF
C3 = C4 = C7 = C8 = 100 nF
C5 = C6 = 0.1 µF.
L1 = L2 = 3.3 µH COIL OR FERRITE INDUCTOR.

Figure 4. Recommended Circuit Schematic

coil inductor of 3.3 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter VCC supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the VCC pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a lowinductance ground current return for the power supply currents.

In addition to these recommendations, Avago's Application Engineering staff is available for consulting on best layout practices with various vendors mux/demux, clock generator and clock recovery circuits. Avago has participated in several reference design studies and is prepared to share the findings of these studies with interested customers. Contact your local Avago sales representative to arrange for this service.

Evaluation Circuit Boards

Evaluation circuit boards are available from Avago's Application Engineering staff. Contact your local Avago sales representative to arrange for access to one if needed.

Recommended Solder and Wash Process

The HFCT-5801 is compatible with industry standard wave or hand solder processes. A drying cycle must be completed after wash process to remove all moisture from the module.

HFCT-5801 Process Plug

The HFCT-5801 transceiver is supplied with a process plug for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand +85°C and a rinse pressure of 110 lb/in2.

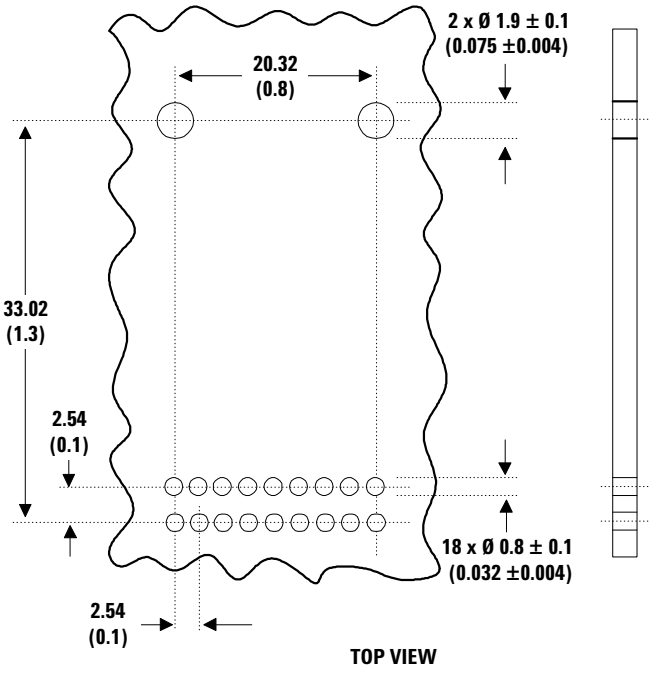
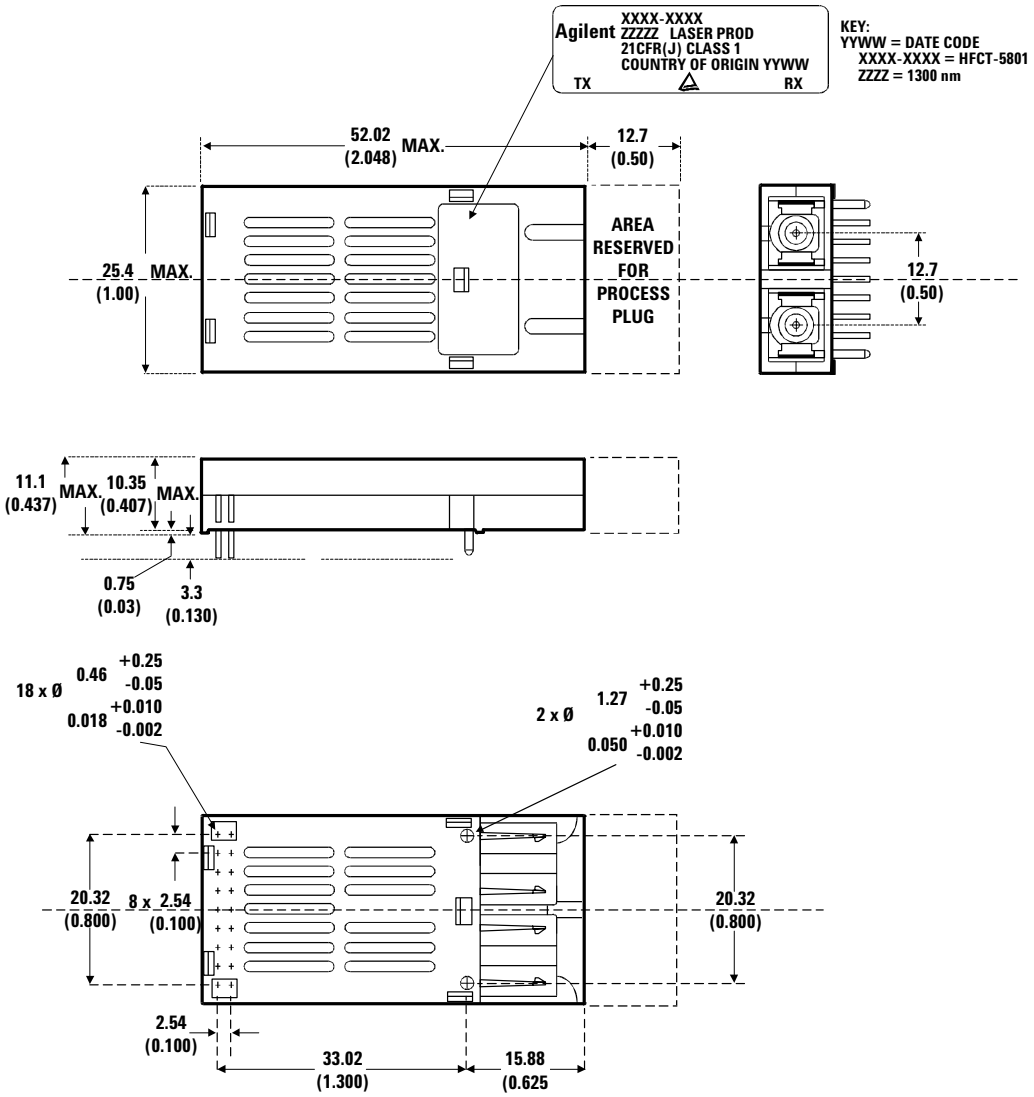


Figure 5. Recommended Board Layout Hole Pattern

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

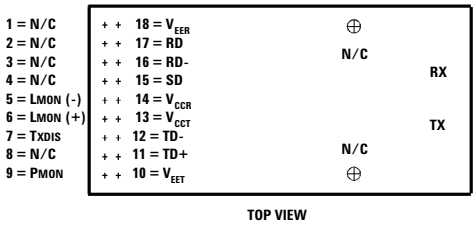
Solder fluxes used with the HFCT-5801 fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha- metals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for the HFCT-5801 are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrolldone.



Note 1: SOLDER POSTS AND ELECTRICAL PINS ARE TIN/LEAD PLATED.

DIMENSIONS ARE IN MILLIMETERS (INCHES).
TOLERANCES: X.XX ±0.025mm UNLESS OTHERWISE SPECIFIED.
X.X ±0.05 mm



TOP VIEW

Figure 6. Package Outline Drawing and Pinout

Regulatory Compliance

The HFCT-5801 is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table 1 for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important. The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas. The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFCT-5801 has been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these HFCT-5801 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Table 1. Regulatory Compliance - Typical Performance

Feature	Test Method	Performance
Electrostatic Discharge ESD) to the Electrical Pins	MII-STD-883C Method 3015.4	Class 1 (>1000 V) - Human Body Model
Electrostatic Discharge ESD) to the Duplex SC Receptacle	Variation of IEC 61000-4-2	Air discharge 15 kV
Electromagnetic Interference (EMI)	FCC Class B	Typically provide greater than 11 dB margin below 1 GHz to FCC Class B when tested in a GTEM with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz dependent on customer board and chassis designs.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 27 MHz to 1 GHz applied to the transceiver without a chassis enclosure.
Eye Safety	FDA CDRH 21-CFR 1040 Class 1	Accession Number: 9521220 - 36
	IEC 60825 - 1 Amendment 2 2001 - 01	License Number: 933/510031/03

Performance Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	+85	°C	
Lead Soldering Temperature/Time	-	-	+260/10	°C/s	
Input Voltage	-	GND	V_{CC}	V	
Power Supply Voltage	-	0	4	V	

Operating Environment

Parameter	Symbol	Minimum	Maximum	Units	Notes
Power Supply Voltage	V_{CC}	+3.1	+3.6	V	
Ambient Operating Temperature - HFCT-5801 A/C	T_{OP}	-40	+85	°C	1
Ambient Operating Temperature - HFCT-5801 B/D	T_{OP}	0	+70	°C	1

Transmitter Section

(Ambient Operating Temperature, V_{CC} = 3.1 V to 3.6 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Center Wavelength	λce	1261	-	1360		
Output Spectral Width (RMS)	$\Delta\lambda$	-	-	7.7	nm	
Average Optical Output Power	P_0	-15	-	-8	dBm	2
Extinction Ratio	E_R	8.2	-	-	dB	
Bias Monitor	-	-	0.1	-	mA/mV	
Rear Facet Monitor	-	-	V_{EE} +1.28	-	V	
Tx Disable	T_{XDIS}	2.0	-	V_{CC}	V	
Power Supply Current	I_{CC}	-	50	140	mA	3
Output Eye	Compliant with Telcordia TR-NWT-000253 and ITU recommendation G.957					
Optical Rise Time	t_R	-	1.5	-	ns	4
Optical Fall Time	t_F	-	1.7	-	ns	4
Data Input Current - Low	I_{IL}	-200	-	-	µA	
Data Input Current - High	I_{IH}	-	-	200	µA	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.81	-	-1.475	V	5
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165	-	-0.880	V	5

Notes:

1. 2 m/s air flow required.
2. Output power is power coupled into a single mode fiber.
3. The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum@ maximum temperature (not including terminations) and end of life. Typical power supply current at +25°C and 3.3 V supply.
4. 10% - 90% Values. Maximum t_R, t_F times tested against eye mask.
5. These inputs are compatible with 10 K, 10 KH and 100 K LVPECL inputs.

Receiver Section

(Ambient Operating Temperature, V_{CC} = 3.1 V to 3.6 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Receiver Sensitivity	-	-	-	-31	dBm	6
Maximum Input Power	-	-7	-	-	dBm	6
Power Supply Current	I_{CC}	-	100	160	mA	7
Signal Detect - Deasserted		-45	-	-31	dBm	
Signal Detect - Hysteresis		0.5		4	dB	
Signal Detect Assert Time (off to on)	AS_Max			100	µs	
Signal Detect Deassert Time (on to off)	ANS_Max			350	µs	
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.84	-	-1.6	V	8
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.1	-	-0.88	V	8
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.84	-	-1.6	V	8
Data Output Voltage - High	V_{OH} - V_{CC}	-1.1	-	-0.88	V	8
Data Output Rise Time	t_r	-	-	2.2	ns	9
Data Output Fall Time	t_f	-	-	2.2	ns	9

Notes

6. Sensitivity and maximum input power levels for a 2^{23}-1 PRBS with 72 ones and 72 zeros inserted. (ITU recommendation G.958).
7. The current includes 2^{23}-1 PRBS signal in LVPECL 50 Ohm loads.
8. These outputs are compatible with 10 K, 10 KH and 100 K LVPECL outputs.
9. 20 - 80% levels.

Table 2. Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the non-conductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	N/C	
2	N/C	
3	N/C	
4	N/C	
5	L_{MON}(-)	Laser Bias Monitor (-) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
6	L_{MON}(+)	Laser Bias Monitor (+) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
7	Tx_{DIS}	Transmitter Disable at 3.3 V supply Transmitter Output Disabled: 2.0 V $\leq V_7 \leq V_{CCT}$ Transmitter Output Uncertain: 1.175 V $\leq V_7 \leq$ 2.0 V. Transmitter Output Enabled: $V_{EET} \leq V_7 \leq$ 1.175 V or open circuit.
8	N/C	

Table 2. Pin Out Table (continued)

Pin	Symbol	Functional Description
9	P_{MON}	Power Monitor The analog voltage measured at this high impedance output provides an indication of whether the optical power output of the Laser Diode is operating within the normal specified power output range per the following relationships: High Light Indication: $V_9 \geq 1.78$ V. Normal Operation: $V_9 \cong 1.28$ V. Low Light Indication: $V_9 \leq 0.78$ V.
10	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.
11	TD+	Transmitter Data In Terminate this high-speed, differential Transmitter Data input with standard LVPECL techniques at the transmitter input pin.
12	TD-	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard LVPECL techniques at the transmitter input pin.
13	V_{CCT}	Transmitter Power Supply Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
14	V_{CCR}	Receiver Power Supply Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
15	SD	Signal Detect Normal input optical levels to the receiver result in a logic "1" output. Low input optical levels to the receiver result in a fault indication shown by a logic "0" output. Signal Detect is a single-ended, LVPECL output. This output will operate with a 270 Ω termination resistor to V_{EE} to achieve LVPECL output levels. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input and Loss of Signal-bar input.
16	RD-	Receiver Data Out Bar Terminate this high-speed, differential, LVPECL output with standard LVPECL techniques at the follow-on device input pin.
17	RD+	Receiver Data Out Terminate this high-speed, differential, LVPECL output with standard LVPECL techniques at the follow-on device input pin.
18	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.

Ordering Information

Temperature Range 0°C to +70°C

HFCT-5801B Black Case

HFCT-5801D Blue Case

Temperature Range -40°C to +85°C

HFCT-5801A Black Case

HFCT-5801C Blue Case

Supporting Documentation

AN 1226: HFCT-5801 Characterization Report

AN1225: HFCT-5801 Application Note

HFCT-5801 Reliability Data

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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