UM6450

Single-chip Microcontroller with 20 sec. Voice Synthesizer

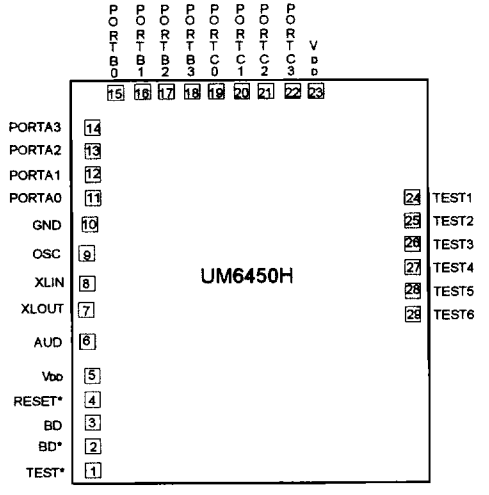
Features

- The UM6450 is a 4-bit CPU core based single chip speech synthesizer
- 4-bit parallel processing ALU compatible with UM6610
- 1.5K x 16 bits ROM
- 64 x 4 bits RAM
- Operating voltage : 2.4V~5.1V
- 12 COMS I/O port pins
- 4-level subroutine nesting including interrupts
- One 8-bit timer with predivider circuit
- Warm-up timer for power on reset
- Powerful interrupt sources :
  - Timer 0 interrupt
  - Port B, port C interrupt
- System clock : 32.768KHz crystal oscillator
- Table branch instruction and return constant instruction for table data generation function
- Data pointer function by special system register control
- Two low power operation modes-HALT and STOP
- Instruction cycle time :
  122*us* for 32.768KHz crystal oscillator
- Built-in 64 words for 20 second speech synthesizing

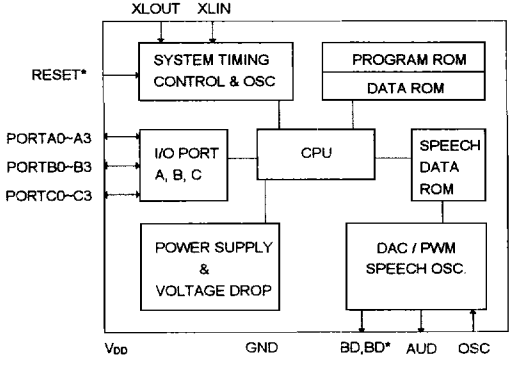
General Description

The UM6450 is a single-chip voice synthesizer with built-in 4-bit microcontroller. The built-in 4-bit microcontroller provides 1.5K x 16 program ROM and 64 x 4 RAM. There are 12 CMOS I/O ports for versatile applications. The 128K x 6 data ROM of voice synthesizer can be separated up to 64 words.The volume and sampling rate of each word is programmable. Audio voice output for the speaker and PWM piezo buzzer driver is available.

Pad Configuration



Block Diagram



Absolute Maximum Ratings*

DC Supply Voltage. . . . . -0.3V to + 7V

Input Voltage. . . . . .GND-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature. . . . . -10 ℃ to + 60 ℃

Storage Temperature. . . . . -55 ℃ to + 125 ℃

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (GND=0V, T_A=25℃, Fosc=32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.4	3	5.1	V	
Operating Current	I_{OP}			3	mA	V_{DD}=3.0V, no load
Stand-by Current	I_{SB}			5	uA	V_{DD}=3.0V,Osc. all output pins unload
Input Current	Ii		10	50	uA	V_{DD}=3.0V, Input voltage =3.0V
Input High Voltage	V_{IH}	0.7 x V_{DD}		V_{DD}	V	
Input Low Voltage	V_{IL}	-0.3		0.3 x V_{DD}	V	
Output Low Voltage	V_{OL}		0.3	0.8	V	Ports, I_{OL} =4mA sink
Output High Voltage	V_{OH}	2.2	2.4		V	Ports, I_{OH}=30uA drive
AUD Output Current	I_{AUD}		-3.0		mA	V_{OUT}=0.7V
BD, BD* Output Current	I_{OH} I_{OL}		-5.0 5.0		mA mA	V_{OUT}=3.0V V_{OUT}=0.5V
STB Bit Pulse Width	t_{STR}		83.4		uS	Typical F_S =6.0KHz
STB Key Release Time	t_{DB}		83.4		uS	Typical F_S =6.0KHz
Frequency Stability	ΔF/F			5	%	[F(3.0) - F(2.4)] / F(3.0)
Frequency Variation	ΔF/F			15	%	

Pad Description

Pad No.	Designation	I/O	Shared by	Description
1	TEST*	I/O		Test mode selection
2	BD*	O		Piezo buzzer driving pin
3	BD	O		Piezo buzzer driving pin
4	RESET*	I		Pad reset input (active low)
5,23	V_{DD}			Power supply
6	AUD	O		Audio speech output
7	XLOUT	O		Crystal oscillator output
8	XLIN	I		Crystal oscillator input
9	OSC	I		Oscillator connect pin for speech
10	GND			Ground
11~14	PORT A0~A3	I/O		Bit programmable I/O

Pad Description (continued)

Pad No.	Designation	I/O	Shared by	Description
15~18	PORT B0~B3	I/O	PBC	Bit programmable I/O, vector interrupt
19~22	PORT C0~C3	I/O	PBC	Bit programmable I/O, vector interrupt
24~29	TEST 1~6	I/O		Test pins

Functional Description

1. CPU

The CPU core contains the following function blocks: program counter, ALU, carry flag, accumulator, table branch register (TBR), data pointer (INX, DPM and DPL), and stack.

(a) PC (Program Counter)

The PC is used for addressing ROM. It consists of 11-bits :

Ripple carry counter (PC10, PC9, PC8, PC7, PC6, PC5 , PC4, PC3, PC2, PC1, PC0).

The program counter is normally incremented (+1) with each instruction execution. When executing a jump instruction (JMP, BA0, BAC, etc.), subroutine call instruction (CALL) or when in the interrupt or initial reset mode, the program counter is loaded with data corresponding to each instruction.

(b) ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction ..... (ADC, SBC, ADD, SUB, ADI, SB)
Decimal adjust for addition/subtraction .....(DAA, DAS)
Logic operations ....(AND, EOR, OR, ANDI, EORI, OR)
Decision .....(BA0, BA1, BA2, BA3, BAZ, BAC)

The carry flag (CY) holds the ALU overflow which arithmetic operation generates. During interrupt servicing or call instruction, the carry is pushed onto the stack and restored back from the stack by RTNI instruction. It is unaffected by RTNW instruction.

(c) Accumulator

The accumulator is a 4-bit register which hold the results of the arthimetic logic unit. By using the ALU, data transfer between the accumulator and the system register, or data memory can be performed.

(d) Stack

This is a group of registers which are used to save the contents of CY & PC (10 ~ 0) sequentially with every occurrence of subroutine call or interrupt and is organized with 12 bits x 4 levels. The MSB is saved for CY. The total level to be used for subroutine call and interrupt is up to 4 levels.

The contents of stack are returned sequentially to the PC with the execution of the return instruction (RTNI/ RTNW). The stack is operated on a first-in, last-out basis. Please note that this 4-level nesting includes both subroutine calls and interrupt requests and the execution of that program may enter an abnormal state. If the number of calls and interrupt requests exceed 4, the bottom of stack will be shifted out.

2. RAM

Built-in RAM consists of general purpose data memory and system registers. RAM space in the system is 128 x 4 bits.

(a) RAM Addressing

Data memory and system register can be accessed by direct addressing in one instruction. The following is the memory allocation map:

$000 - $01F: System register and I/O
$040 - $07F: Data memory

The built-in 64 x 4 bit data RAM is used by UM6450.

(b) Data Memory

The general purpose data memory is organized as 64 x 4 bits. It is used for data storage. Because of its static nature, the RAM can maintain its data after CPU enters into the STOP or HALT mode.

(c) System Registers

The configuration of system registers is listed as follows:

	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer-0 mode register (TM0)
$03	-	-	-	-	-	Reserved
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer-0 load/counter register low digit
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer-0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORT A
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORT B
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORT C
$0B	-	-	-	-	-	Reserved
$0C	-	-	-	-	-	Reserved
$0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register (TBR)
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register (INX)
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	SE4	SE3	SE2	SE1	R/W	Speech word selection low
$14	SE8	SE7	SE6	SE5	R/W	Volume, speech word selection high
$15	BUSY*	STR*	SE9	SE10	R/W	Speech status, sample rate
$16 : $1B	:	:	:	:	:	Reserved
$1C	-	TMC	TML.1	TML.0	W	Test mode register (TMR)
$1D	-	-	-	-	-	Reserved
$1E	-	-	-	-	-	Reserved
$1F	-	-	-	-	-	Reserved

(d) Data Pointer

Data memory contents can be addressed by data pointer indirectly. The pointer address is placed into register DPH (3-bits), DPM (3-bits) and DPL (4-bits) respectively. The addressing range is up to 128 locations. The pseudo index address (INX) is used to read or write data memory, then actual RAM address bit 9~bit 0 come from DPH, DPM and DPL. The DPH is set to 0 x 000 by S/W.

3. ROM

The UM6450 can address up to 1.5K words x 16 bits of program area from $000 to $5FF. ROM space in the system is 1536 x 16 bits.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed one by one. There is an area from address $000 through $004 that is reserved for special interrupt service routines as starting execution vector address.

Address	Instructions	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	-	Reserved
002H	JMP instruction	Jump to TIMER 0 service routine
003H	-	Reserved
004H	JMP instruction	Jump to PBC service routine (port B, C)

* JMP instruction can be replaced by any other instruction.

(b) Table Data Reference

Table data can be placed in the program memory. Table data can be referenced by table branch instruction (TJMP) and return constant instruction (RTNW). The table branch register (TBR) and accumulator (A) is placed by offset address of table data area in program ROM. Then, TJMP instruction branches into address [(PC10 - PC8) * (2**8) + (TBR,A)]. The address is placed by RTNW instruction to return look-up value to TBR,A. The ROM code bit 7～bit 4 are placed into TBR and bit 3 ～bit 0 into A.

4. Timer

UM6450 has one 8-bit timer, and its operation is counting up. The timer consists of an 8-bit counter and an 8-bit preload register.

The timer provides the following functions :

- Programmable interval timer function.
- Read counter value.

(a) Timer 0 Configuration and Operation

The timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Each has low order digits and high order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H). Write the low-order digit first, and then the high-order digit. The timer counter is loaded with the content of load register automaticlly. When the high order digit is written or count overflow happens, the timer overflow will generate an interrupt if the interrupt enable flag is set.

The timer can be programmed in several different system clock sources by setting timer mode register (TM0).

(b) Timer Mode Register

The 8-bit counter prescaler overflows output pulses. The timer mode registers (TM0) are 4-bit registers used for timer control as shown in table 1. The mode register selects the input pulse sources into the timer.

Table 1. Timer 0 Mode Register ($02)

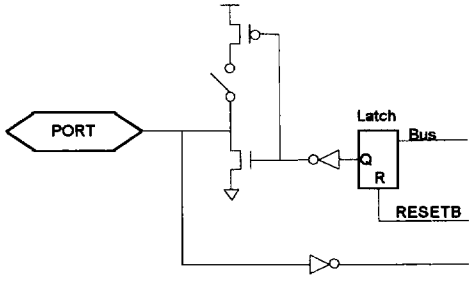
TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/ 2^{11}$	System clock
0	0	1	$/ 2^{9}$	System clock
0	1	0	$/ 2^{7}$	System clock
0	1	1	$/ 2^{5}$	System clock
1	0	0	$/ 2^{3}$	System clock
1	0	1	$/ 2^{2}$	System clock
1	1	0	$/ 2^{1}$	System clock
1	1	1	$/ 2^{0}$	System clock

5. PORT

(a) Functional Description

- CMOS type I/O port or open drain output port by mask option.
- PMOS as built-in pull-up for Input .
- Independent I/O control for every bit .
- Output high in initial state for CMOS output port .
- Operates the same as data memory for arithmetic and logic instructions.

(b) Circuit Diagram



(c) Programming

- I/O ports of UM6450 can be accessed by read/write system register.
- Memory map addresses are listed as follows:

Address	Bit3	Bit2	Bit1	Bit0	Read	Write
$08	Port A.3	Port A.2	Port A.1	Port A.0	R/W	Port A
$09	Port B.3	Port B.2	Port B.1	Port B.0	R/W	Port B
$0A	Port C.3	Port C.2	Port C.1	Port C.0	R/W	Port C

- Users can output any value to any I/O port bit at any time.
- Before reading the I/O port bit, users have to output "1" to the same bit.

6. Speech

Built-in speech is PCM coded for 20 seconds synthesizing speech. It contains an on-chip ROM for speech data storage. The stored voice is typically 20 seconds, depending on the sampling rate of synthesized speech. The built-in ROM can be separated up to 64 words of arbitrary length.

CPU accesses 64 words directly, retriggerable and the volume and sample rate are programmable by CPU except the word of power-down code. The block also contains piezo-electric buzzer drivers, and audio speech output.

(a) RAM mapping control register is shown as below:

$13	SE4	SE3	SE2	SE1	R/W	Speech word low select
$14	SE8	SE7	SE6	SE5	R/W	Speech word high select and volume
$15	BUSY*(R)	STR*(W)	SE10	SE9	R/W	Speech status and sample rate

(b) Speech word selects from SE6 ~ SE1. The format is shown below:

SE6	SE5	SE4	SE3	SE2	SE1	Word Selection
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7
0	0	1	0	0	0	8
:	:	:	:	:	:	:
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	0	1	61 (Ramp-up word)
1	1	1	1	1	0	62 (Ramp-down word)
1	1	1	1	1	1	63 (power-down)

(c) Volume control is shown below:

SE7	SE8	Volume Status
1	1	-18dB
0	1	-12dB
1	0	- 6dB
0	0	0dB

(d) Sample rate control is shown below :

SE9	SE10	Sample Rate
0	1	4.0KHz
1	1	4.8KHz
0	0	6.0KHz
1	0	8.0KHz

The control bit BUSY* can be read only by CPU to check whether the speech is playing. BUSY* writes to low when the speech starts playing and writes to high when the speech ends. BUSY* normally remains high.

The control bit STR* normally remains high. While STR* writes to low, the falling edge triggers the speech to start playing.

While the speech is playing, the audio output and piezo buzzer will be active at the same time. The start and stop address of each word is stored in control ROM.

7. Interrupt

Two interrupt sources are available for the UM6450 :

- Timer 0 interrupt (TMR0)
- Port falling edge detection interrupt (PBC*)

(a) Interrupt Control Bits and Interrupt Service:

- The interrupt request is generated when the IRQx is set to 1 and IEx is 1. At this time, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into the stack memory and the PC will jump to the interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically , then any interrupt is disabled. The IRQX, which causes the interrupt service, must be reset by software in the interrupt service routine. Once IEx is set to 1 again, UM6450 can service multi-level interrupts.
- The interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by program. Those flags are cleared to 0 at initialization by UM6450 reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	Remarks
$00	-	IET0	-	IEP	Interrupt enable flags
$01	-	IRQT0	-	IRQP	Interrupt request flags

(b) Vector Address and Interrupt Priority

Priority	Interrupt Sources
1(Most)	RESET
2	Reserved
3	TMR0
4	Reserved
5(Least)	PBC

8. System Clock and Oscillation Circuit

The system clock generator produces the basic clock pulses that provide the system clock to CPU and on-chip peripherals.

- Instruction cycle time
  122 usec. for 32.768KHz system clock

9. HALT or STOP Mode

- After the execution of HALT instruction, UM6450 will enter the halt mode. In the halt mode, CPU will stop operating but peripheral circuit (timer) will keep operating.
- After the execution of STOP instruction, UM6450 will enter the stop mode. In the stop mode, the whole chip (including the oscillator) will stop operating.
- In the halt mode, UM6450 will wake up if any interrupt occurs.
- In the stop mode, UM6450 will wake up if port interrupt occurs.

10. Warm-up Timer

The warm-up timer eliminates unstable initial oscillation when the oscillator starts in the following two situations :

(a) power on reset.

(b) wake up from stop mode.

The warm-up time interval is 0.5 second at 32.76KHz.

11. System Reset

- Hardware reset input.
- Warm-up timer for power on reset.

(a) Initial State

Hardware	After Power-on Reset
Program Counter	$000
CY	Undefined
Data Memory	Undefined
System register	Undefined
AC	Undefined
Timer Counter	Undefined
Timer Load Register	0
Interrupt Enable Flags	0
Interrupt Request Flags	0
BUSY*, STR* Output	1, 1, all lighted

12. Instruction Set

All instructions are one cycle one word . The major feature is RAM oriented operation.

(a) Accumulator Type

Mnemonic	Instruction Codes	Functions	Flag Change
ADC X(,B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM	00000 1bbb xxx xxxx	AC,Mx ← Mx + AC + CY	CY
ADD X(,B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM	00001 1bbb xxx xxxx	AC,Mx ← Mx + AC	CY
SBC X(,B)	00010 0bbb xxx xxxx	AC ← Mx + (-AC) +CY	CY
SBCM	00010 1bbb xxx xxxx	AC,Mx ← Mx + (-AC) +CY	CY
SUB X(,B)	00011 0bbb xxx xxxx	AC ← Mx + (-AC) + 1	CY
SUBM	00011 1bbb xxx xxxx	AC,Mx ← Mx + (-AC) + 1	CY
XOR X(,B)	00100 0bbb xxx xxxx	AC ← Mx XOR AC	
XORM	00100 1bbb xxx xxxx	AC,Mx ← Mx XOR AC	
OR X(,B)	00101 0bbb xxx xxxx	AC ← Mx OR AC	
ORM X(,B)	00101 1bbb xxx xxxx	AC,Mx ← Mx OR AC	
AND X(,B)	00110 0bbb xxx xxxx	AC ← Mx AND AC	
ANDM X(,B)	00110 1bbb xxx xxxx	Mx ← Mx AND AC	

(b) Immediate Type

Mnemonic	Instruction Codes	Functions	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC,Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + (-I) + 1	CY
SBIM X,I	01011 iiii xxx xxxx	AC,Mx ← Mx + (-I) + 1	CY
XORI X,I	01100 iiii xxx xxxx	AC,Mx ← Mx XOR I	
ORI X,I	01101 iiii xxx xxxx	AC,Mx ← Mx OR I	
ANDI X,I	01110 iiii xxx xxxx	AC,Mx ← Mx AND I	

(c) Decimal Adjust

Mnemonic	Instruction Codes	Functions	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust AC for Add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust AC for Sub.	CY

(d) Transfer Instruction

Mnemonic	Instruction Codes	Functions	Flag Change
LDA X(,B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(,B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC,Mx ←I	

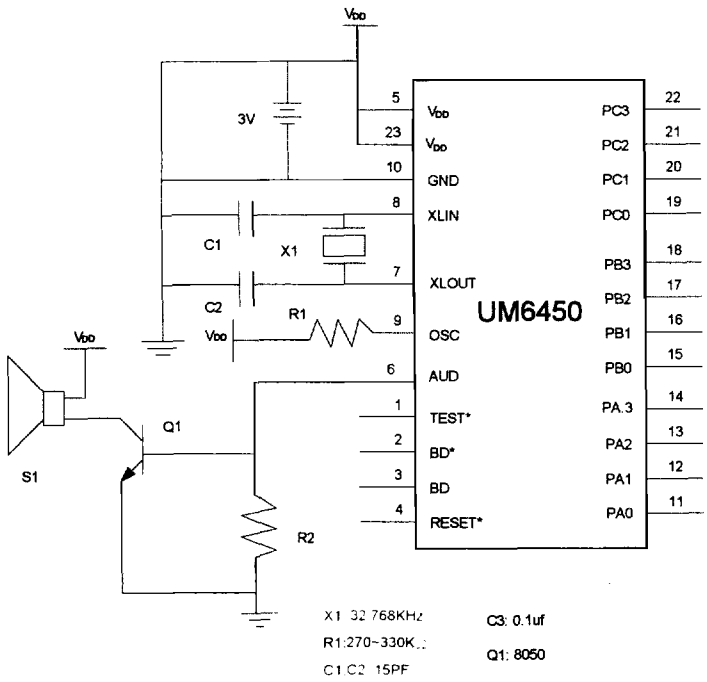
(e) Control Instruction

Mnemonic	Instruction Codes	Functions	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
A2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1, PC ← X (Not including p)	
RTNW H;L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; A ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Including p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8)(TBR)(A)	
NOP	11111 1111 111 1111	No Operation	

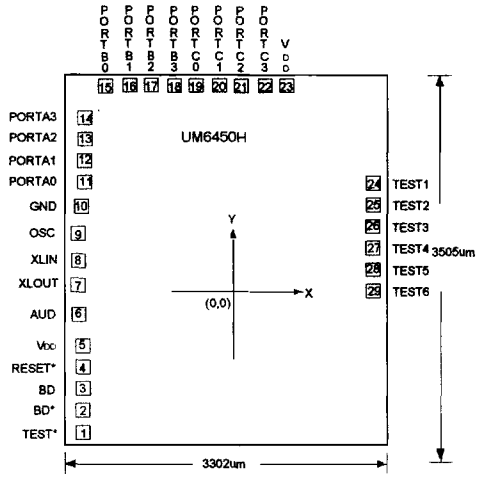
Where

PC	:	Program Counter	I,(-I)	:	Immediate data
AC	:	Accumulator	XOR	:	Logical Exclusive-Or
(-AC)	:	Complement of Accumulator	OR	:	Logical Or
CY	:	Carry Flag	AND	:	Logical And
Mx	:	Data Memory	bbb	:	RAM Bank=000
p	:	ROM Page =0	TBR	:	Table Branch Register
ST	:	Stack	AC(n),n-0~3	:	Bit n of Accumulator

Application Circuit (for reference only)



Bonding Diagram



* Connecting IC substrate to GND or keeping floating is recommended.
* Pad window ares : 100*um* x 100*um*

(unit :*um*)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	TEST*	-1310	-1538	16	PORT B1	-804	1548
2	BD*	-1310	-1257	17	PORT B2	-644	1548
3	BD	-1310	-985	18	PORT B3	-434	1548
4	RESET*	-1310	-685	19	PORT C0	-274	1548
5	V_{DD}	-1310	-505	20	PORT C1	-63	1548
6	AUD	-1340	-128	21	PORT C2	96	1548
7	XLOUT	-1349	143	22	PORT C3	306	1548
8	XLIN	-1349	361	23	V_{DD}	495	1542
9	OSC	-1349	564	24	TEST 1	1438	912
10	GND	-1309	761	25	TEST 2	1438	752
11	PORT A0	-1283	938	26	TEST 3	1438	577
12	PORT A1	-1283	1098	27	TEST 4	1438	417
13	PORT A2	-1283	1290	28	TEST 5	1438	241
14	PORT A3	-1283	1450	29	TEST 6	1438	81
15	PORT B0	-1050	1548				

Ordering Information

Part No.	Package
UM6450H-XX	CHIP FORM

XX : Code numbering assigned per customer specifications in hexadecimal format (X=0~9, A~F)