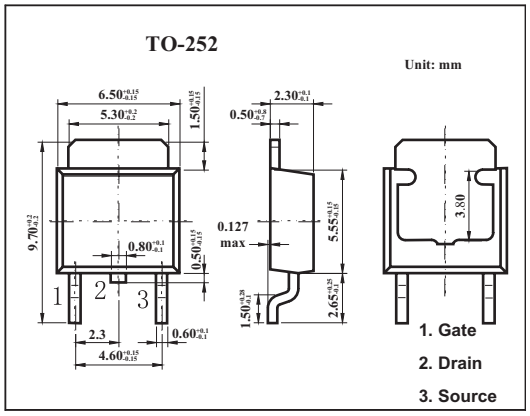
TY Semicondutor®

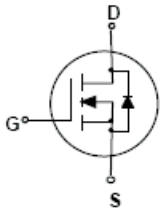
Product specification

KDD3670



■ Features

- 34 A, 100 V. $R_{DS(ON)}$ = 32mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 35mΩ @ V_{GS} = 6 V
- Low gate charge (57 nC typical)
  Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (Note 1)	I_D	34	A
Drain Current Pulsed		100	A
Power dissipation @ T_C=25℃ (Note 1)	P_D	83	W
Power dissipation @ T_a=25℃ (Note 1a)		3.8	
Power dissipation @ Ta=25℃ (Note 1b)		1.6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.8	℃/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	96	℃/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Single Pulse Drain-Source Avalanche Energy	W_{DSS}	V_{DD} = 50 V, I_D = 7.3A (Not 2)			360	mJ
Maximum Drain-Source Avalanche Current	I_{AR}	(Not 2)			7.3	A
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		92		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2	2.5	4	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		-7.2		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7.3 A		22	32	mΩ
		V_{GS} = 10 V, I_D = 7.3 A,TJ = 125℃		39	56	
		V_{GS} = 6 V, I_D =7 A,		24	35	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5 V	25			A
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 7.3 A	15	31		S
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V,f = 1.0 MHz		2490		pF
Output Capacitance	C_{oss}			265		pF
Reverse Transfer Capacitance	C_{rss}			80		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 1 A,V_{GS} = 10 V, R_{GEN} = 6 Ω		16	26	ns
Turn-On Rise Time	tr			10	18	ns
Turn-Off Delay Time	$t_{d(off)}$			56	84	ns
Turn-Off Fall Time	tf			25	40	ns
Total Gate Charge	Q_g	V_{DS} = 50 V, I_D = 7.3 A,V_{GS} = 10 V (Note 2)		57	80	nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			15		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				2.7	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.7 A (Not 2)		0.72	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in² pad of 2oz copper.

b) $R_{\theta JA}$ = 96°C/W on a minimum mounting pad.

Scale 1 : 1 on letter size paper

Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%