HD44780, HD44780A (LCD-II)

(Dot Matrix Liquid Crystal Display Controller & Driver)

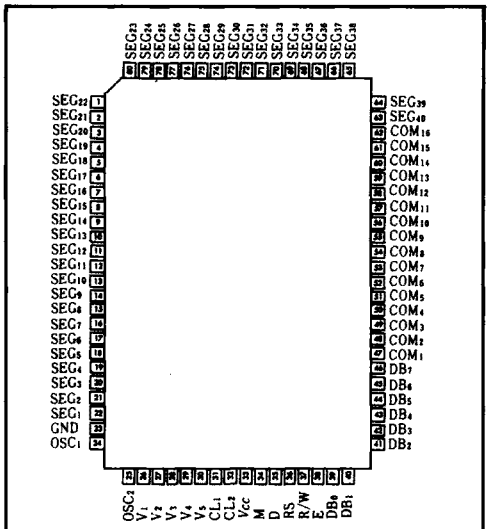
Description

The LCD-II (HD44780, HD44780A) dot matrix liquid crystal display controller & driver LSI displays alphanumerics, kana characters, and symbols. It drives a dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with low chip count by using the LCD-II (HD44780, HD44780A).
If an HD44100H driver LSI is connected to the HD44780, up to 80 characters can be displayed.
The LCD-II is produced by the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcontroller or microprocessor can complete a portable battery-driver device with low power dissipation.

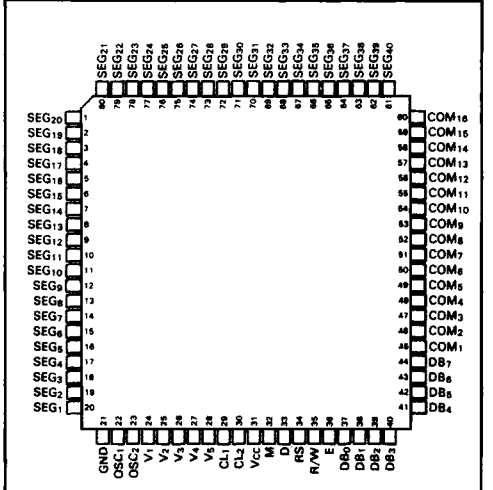
Feautures

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU
- Display data RAM: 80 × 8 bits (80 characters, max.)
- Character generator ROM:
  - —Character font 5 × 7 dots: 160 characters
  - —Character font 5 × 10 dots: 32 characters
- Character generator RAM
  - —Character font 5 × 7 dots: 8 characters
  - —Character font 5 × 10 dots: 4 characters
- Both display data and character generator RAMs can be read from the MPU
- Internal liquid crystal display driver:
  - —16 common signal drivers
  - —40 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor (selected by program):
  - —1/8 duty: 1 line of 5 × 7 dots + cursor
  - —1/11 duty: 1 line of 5 × 10 dots + cursor

Pin Arrangement



(FP-80)
(Top View)



(FP-80A)
(Top View)

—1/16 duty: 2 line of 5 × 7 dots + cursor
- Wide range of instruction functions:
  Display clear, Cursor home, Display on/off, Cursor on/off,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power on (Internal reset circuit)
- Internal oscillation circuit
  (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply:
  A single +5 V (excluding power for liquid crystal display drive)
- Operation temperature range:
  −20 to +75℃ (Device for −40 to +85℃ available upon request)
- 80-pin plastic QFP (FP-80, FP-80A)
  80-pin thin plastic QFP (TFP-80: under development)

Maximum Number of Display Characters

No. of Display Lines	Duty Factor	Extension	LCD-II	HD44100H	No. of Display Characters
1-line display	1/8 1/11 duty cycle	Not provided	1	—	8 characters × 1 line
		Porovided	1	9 (8 characters/each)	80 characters × 1 line
2-line display	1/16 duty cycle	Not provided	1	—	8 characters × 2 lines
		Provided	1	4 (8 characters × 2 lines/each)	40 characters × 2 lines

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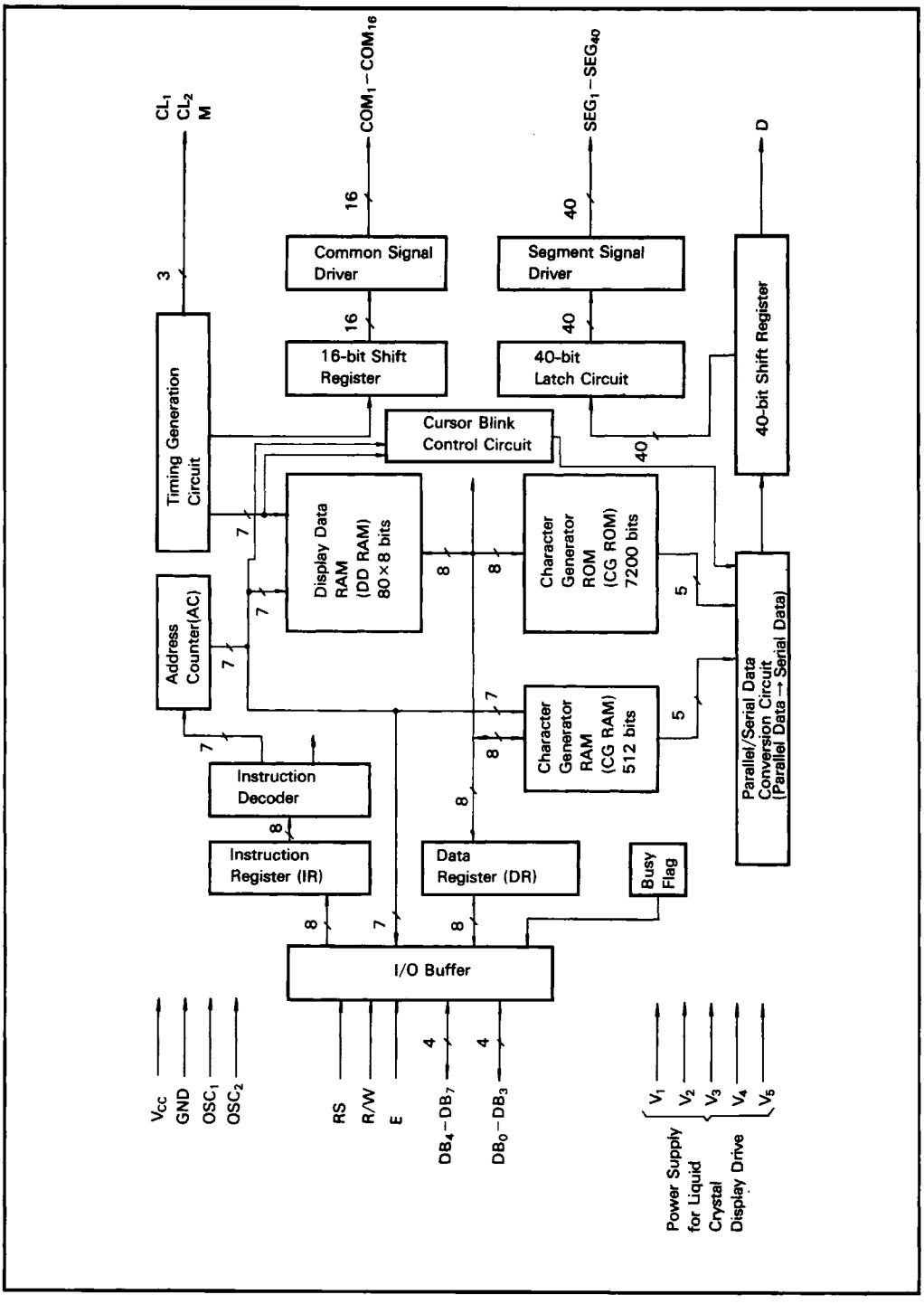
Ordering Information

Type No.	Operation Frequency	Package
HD44780SA**H	1.0 MHz	80-Pin plastic QFP (FP-80)
HD44780SA**FH		80-Pin plastic QFP (FP-80A)
HD44780SA**TF		80-pin thin plastic QFP (TFP-80: under development)
HD44780SA**FA	1.5 MHz	80-Pin plastic QFP (FP-80)

Note: ** = ROM Code No.

Block Diagram (LCD-II Interior)



Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	−0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}−13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	−0.3 to V_{CC}+0.3	V	
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND = 0 V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$
(high ← → low)

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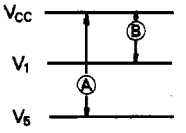
Electrical Characteristics
(V_{CC} = 5 V ± 10%, T_a = −20 to +75°C)

The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".



Ⓐ = $V_{CC} - V_5$
Ⓑ = $V_{CC} - V_1$
Ⓐ ≥ 1.5 V
Ⓑ ≤ 0.25×Ⓐ

HD44780

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.2	—	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	−0.3	—	0.6	V		(2)
Output High Voltage (1) (TTL)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1) (TTL)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	(3)
Output High Voltage (2) (CMOS)	V_{OH2}	0.9V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2) (CMOS)	V_{OL2}	—	—	0.1V_{CC}	V	L_{OL} = 0.04 mA	(4)
Driver Voltage Descending (COM)	V_{COM}	—	—	2.9	V	Id=0.05 mA	(10)
Driver Voltage Descending (SEG)	V_{SEG}	—	—	3.8	V	Id=0.05 mA	(10)
Input Leakage Current	I_{IL}	−1	—	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull-Up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	—	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	—	0.35	0.6	mA	Rf oscillation External clock operation V_{CC} = 5 V, f_{OSC} = f_{cp} = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty Cycle	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	—	—	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	—	—	0.2	μs		(7)
Input High Voltage (2)	V_{IH2}	V_{CC} − 1.0	—	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	—	—	1.0	V		(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 91 kΩ ± 2%	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	4.6	—	11	V	V_{CC} − V5 1/5 bias	(13)
	V_{LCD2}	3.0	—	11	V	1/4 bias	(13)

HD44780A

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage (1)	V_{IH1}	2.2	—	V_{CC}	V		(2)
Input Low Voltage (1)	V_{IL1}	−0.3	—	0.6	V		(2)
Output High Voltage (1) (TTL)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA	(3)
Output Low Voltage (1) (TTL)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA	(3)
Output High Voltage (2) (CMOS)	V_{OH2}	0.9V_{CC}	—	—	V	$-I_{OH}$ = 0.04 mA	(4)
Output Low Voltage (2) (CMOS)	V_{OL2}	—	—	0.1V_{CC}	V	L_{OL} = 0.04 mA	(4)
Driver Voltage Descending (COM)	V_{COM}	—	—	2.9	V	Id = 0.05 mA	(10)
Driver Voltage Descending (SEG)	V_{SEG}	—	—	3.8	V	Id = 0.05 mA	(10)
Input Leakage Current	I_{IL}	−1	—	1	μA	V_{in} = 0 to V_{CC}	(5)
Pull up MOS Current	$-I_P$	50	125	250	μA	V_{CC} = 5 V	
Power Supply Current (1)	I_{CC1}	—	0.55	0.8	mA	Ceramic filter oscillation V_{CC} = 5 V, f_{OSC} = 250 kHz	(6)
Power Supply Current (2)	I_{CC2}	—	0.35	0.6	mA	Rf oscillation External clock operation V_{CC} = 5 V, f_{OSC} = f_{cp} = 270 kHz	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}	125	250	350	kHz		(7)
External Clock Duty	Duty	45	50	55	%		(7)
External Clock Rise Time	t_{rcp}	—	—	0.2	μs		(7)
External Clock Fall Time	t_{fcp}	—	—	0.2	μs		(7)
Input High Voltage (2)	V_{IH2}	V_{CC} − 1.0	—	V_{CC}	V		(12)
Input Low Voltage (2)	V_{IL2}	—	—	1.0	V		(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{OSC}	190	270	350	kHz	Rf = 91 kΩ±2%	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{OSC}	245	250	255	kHz	Ceramic filter	(9)
LCD Voltage	V_{LCD1}	4.6	—	11	V	V_{CC} − V5 1/5 bias	(13)
	V_{LCD2}	3.0	—	11	V	1/4 bias	(13)

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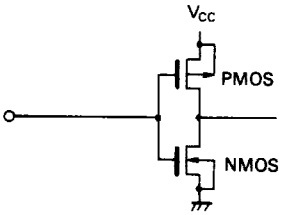
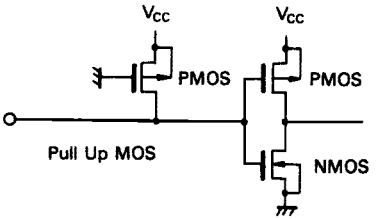
Notes: 1. The following are I/O terminal configurations except for liquid crystal display output.

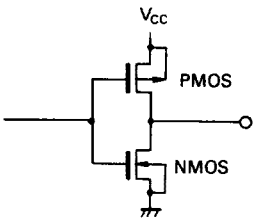
- Input Terminal
  Applicable Terminals: E
  (MOS without pull up)



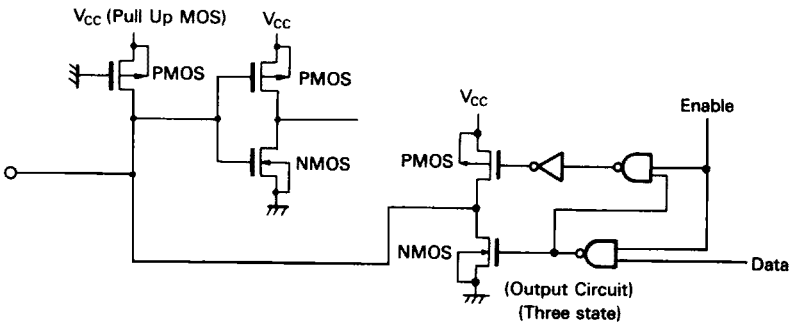
- Applicable Terminals: RS, R/W
  (MOS with pull up)



- Output Terminal
  Applicable Terminals: CL_1, CL_2, M, D

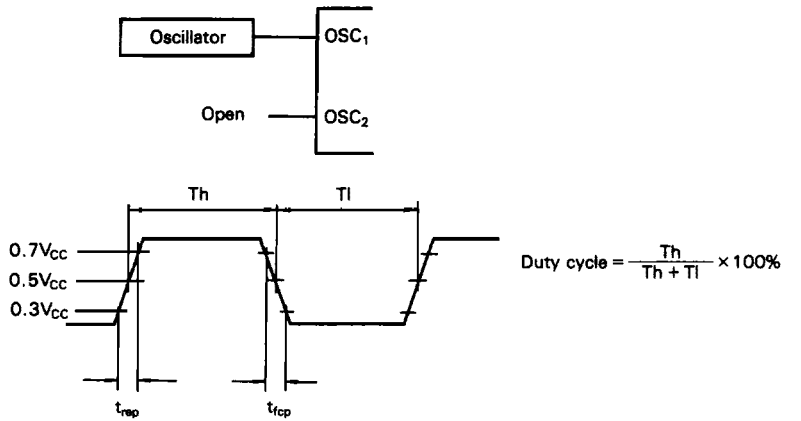


- I/O Terminal
  Applicable Terminals: DB_0 to DB_7

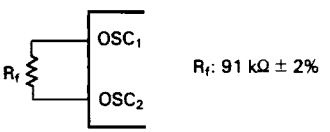


Notes: 2. Input terminals and I/O terminals. Excludes OSC_1 terminals.
Notes: 3. I/O terminals.
Notes: 4. Output terminals.
Notes: 5. Current flowing through pull-up MOSs and output drive MOSs is excluded.
Notes: 6. Input/output current is excluded. When cmos input is at an intermediate level, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Notes: 7. External clock operation.

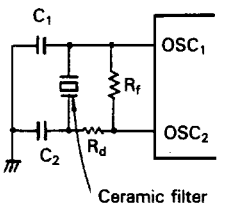


Notes: 8. Internal oscillator operation using oscillation resistor Rf.



Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacitance, wiring length for these terminals should be minimized.

Notes: 9. Internal oscillator operation using a ceramic filter.



Ceramic filter: CSB250A (Murata)
R_f: 1 MΩ ± 10%
C_1: 680 pF ± 10%
C_2: 680 pF ± 10%
R_d: 3.3 kΩ ± 5%

Notes: 10. Applies to both V_{COM} and V_{SEG} voltage drops.
V_{COM}: From power supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})
V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

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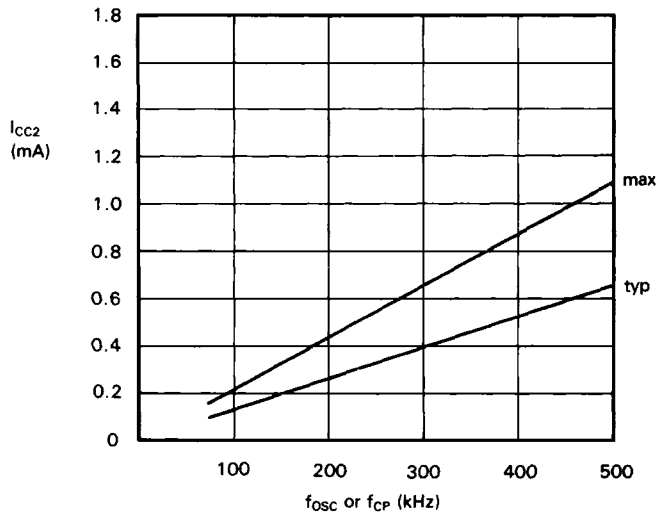
Notes: 11. Relation between operation frequency and current consumption is shown in this diagram (V_{CC} = 5 V).



Notes: 12. Applied to OSC_1 terminal.
Notes: 13. The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

Timing Characteristics

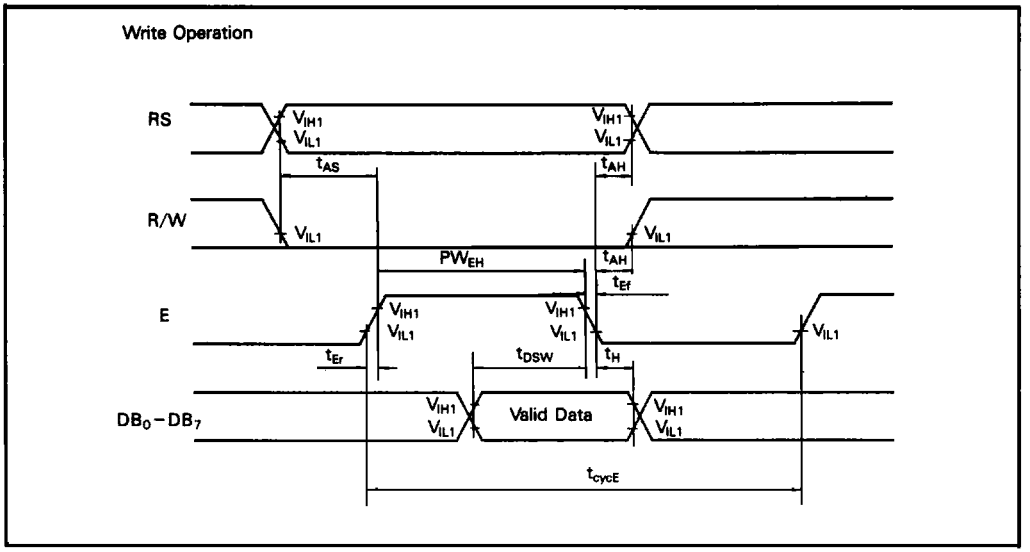


Figure 1 Bus Write Operation Sequence (Writing data from MPU to LCD-II)

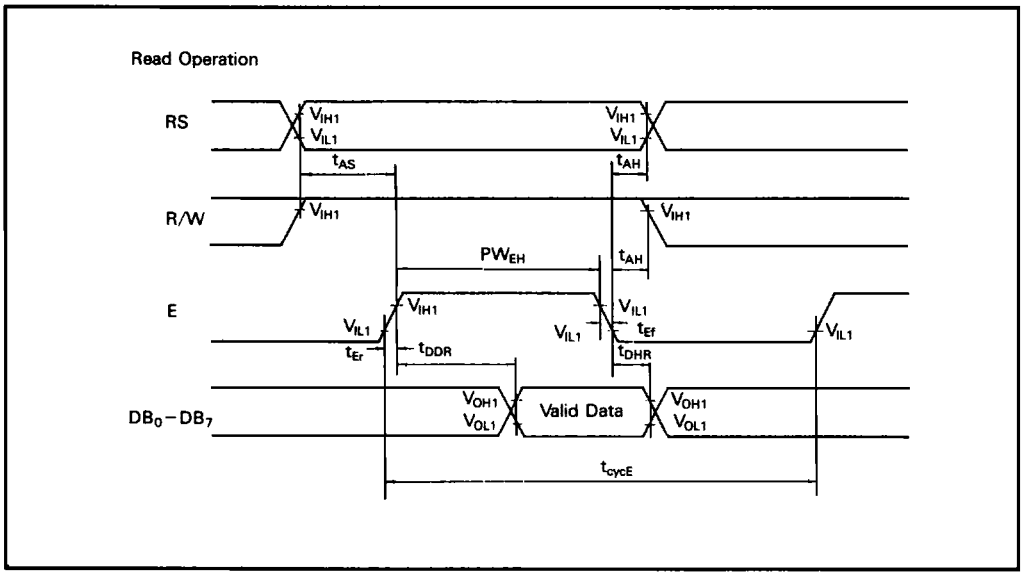


Figure 2 Bus Read Operation Sequence (Reading out data from LCD-II to MPU)

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Interface Signal with Driver LSI HD44100H

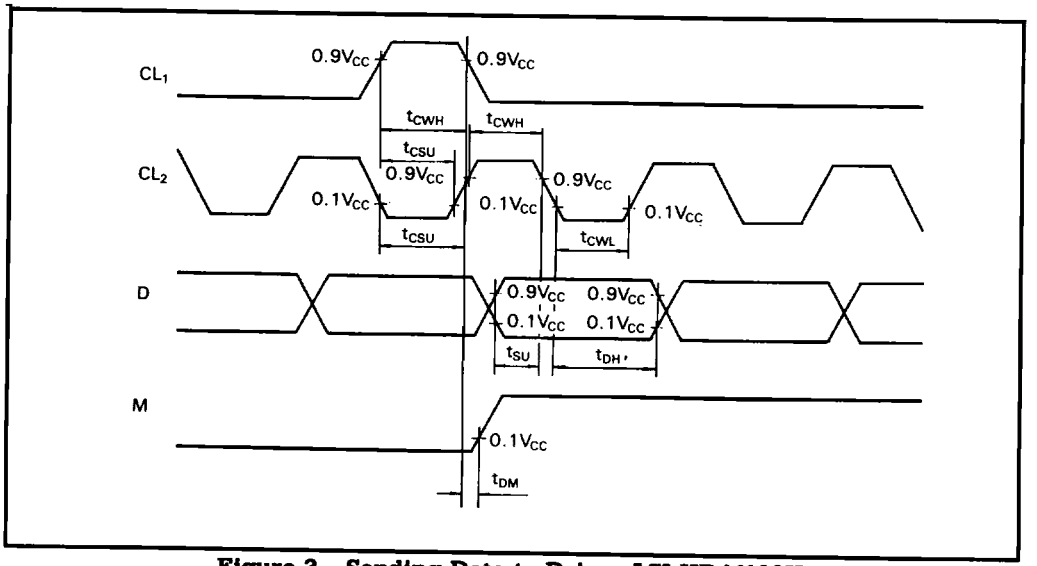

Figure 3 Sending Data to Driver LSI HD44100H

Bus Timing Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = −20 to +75°C)

HD44780

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	1000	—	ns	Fig. 1
Enable Pulse Width	High level	PW_{EH}	450	—	ns	Fig. 1
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 1
Address Set-up Time	RS, R/W E	t_{AS}	140	—	ns	Fig. 1
Address Hold Time		t_{AH}	10	—	ns	Fig. 1
Data Set-up Time		t_{DSW}	195	—	ns	Fig. 1
Data Hold Time		t_H	10	—	ns	Fig. 1

Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	1000	—	ns	Fig. 2
Enable Pulse Width	High level	PW_{EH}	450	—	ns	Fig. 2
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 2
Address Set-up Time	RS, R/W E	t_{AS}	140	—	ns	Fig. 2
Address Hold Time		t_{AH}	10	—	ns	Fig. 2
Data Delay Time		t_{DDR}	—	320	ns	Fig. 2
Data Hold Time		t_{DHR}	20	—	ns	Fig. 2

HD44780A

Write Operation (Writing data from MPU to LCD-II)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	666	—	ns	Fig. 1
Enable Pulse Width	High level	PW_{EH}	300	—	ns	Fig. 1
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 1
Address Set-up Time	RS, R/W E	t_{AS}	60*1	—	ns	Fig. 1
			100*2	—	ns	
Address Hold Time		t_{AH}	10	—	ns	Fig. 1
Data Set-up Time		t_{DSW}	100	—	ns	Fig. 1
Data Hold Time		t_H	10	—	ns	Fig. 1

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Read Operation (Reading data from LCD-II to MPU)

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Enable Cycle Time		$t_{cyc}E$	666	—	ns	Fig. 2
Enable Pulse Width	High level	PW_{EH}	300	—	ns	Fig. 2
Enable Rise/Fall Time		t_{Er}, t_{Ef}	—	25	ns	Fig. 2
Address Set-up Time	RS, R/W E	t_{AS}	60*1 100*2		ns	Fig. 2
Address Hold Time		t_{AH}	10	—	ns	Fig. 2
Data Delay Time		t_{DDR}	—	190	ns	Fig. 2
Data Hold Time		t_{DHR}	20	—	ns	Fig. 2

Notes: *1. 8-bit interface mode
*2. 4-bit interface mode

Interface Signal with HD44100H Timing Characteristics
(V_{CC} = 5.0 V ± 10%, GND = 0 V, T_a = −20 to +75°C)

HD44780

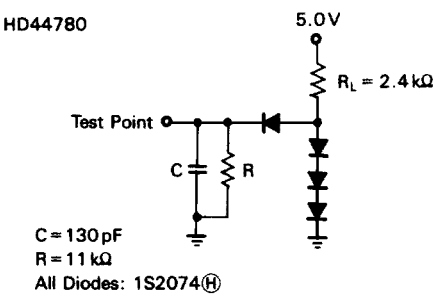
Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Clock Pulse Width	High level	t_{CWH}	800	—	ns	Fig. 3
Clock Pulse Width	Low level	t_{CWL}	800	—	ns	Fig. 3
Clock Set-up Time		t_{CSU}	500	—	ns	Fig. 3
Data Set-up Time		t_{SU}	300	—	ns	Fig. 3
Data Hold Time		t_{DH}	300	—	ns	Fig. 3
M Delay Time		t_{DM}	−1000	1000	ns	Fig. 3

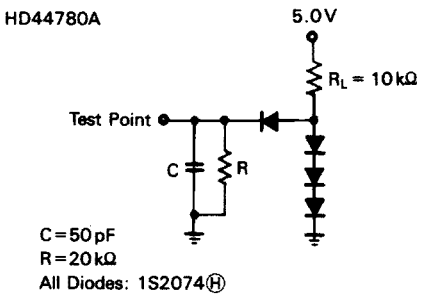
HD44780A

Item		Symbol	Limit Min	Limit Max	Unit	Test Condition
Clock Pulse Width	High level	t_{CWH}	800	—	ns	Fig. 3
Clock Pulse Width	Low level	t_{CWL}	800	—	ns	Fig. 3
Clock Set-up Time		t_{CSU}	500	—	ns	Fig. 3
Data Set-up Time		t_{SU}	300	—	ns	Fig. 3
Data Hold Time		t_{DH}	300	—	ns	Fig. 3
M Delay Time		t_{DM}	−1000	1000	ns	Fig. 3

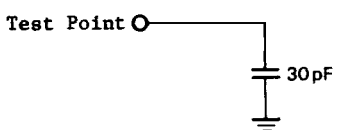
Notes:

Loading Circuit (TTL Load): DB_0 to DB_7





Loading Circuit (CMOS Load): CL_1, CL_2, D, M



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Power Supply Conditions Using Internal Reset Circuit

LCD-II

Item	Symbol	Limit		Unit	Test Condition
		Min	Max		
Power Supply Rise Time	t_{rcc}	0.1	10	ms	—
Power Supply OFF Time	t_{OFF}	1	—	ms	—

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction. (Refer to "Initializing by Instruction")

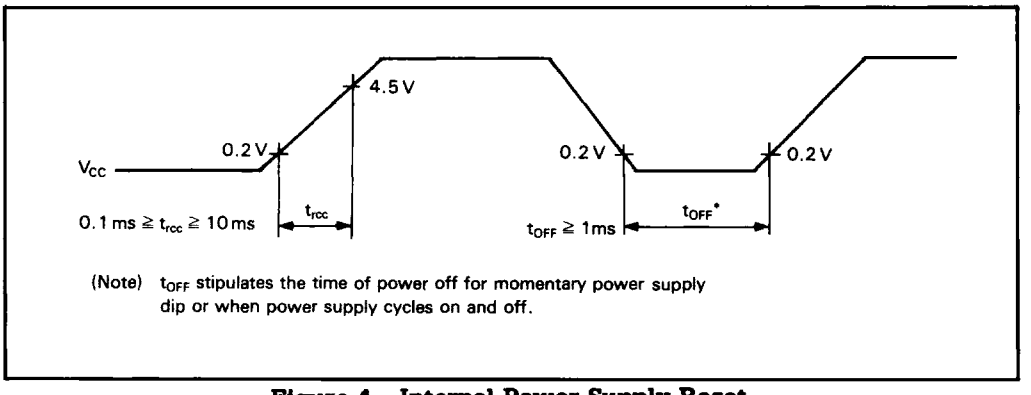


Figure 4 Internal Power Supply Reset

Terminal Function

Table 1 Functional Description of Terminals

Signal Name	No. of Lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W). 0: Write 1: Read
E	1	Input	MPU	Operation start signal for data read/write.
DB_4-DB_7	4	Input/ Output	MPU	Higher order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II. DB_7 can be used as a BUSY flag.
DB_0-DB_3	4	Input/ Output	MPU	Lower order 4 bidirectional three-state data bus lines. Used for data transfer between the MPU and the LCD-II. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Sends character pattern data corresponding to each common signal serially. 0: Non selection 1: Selection
COM_1-COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are changed to non-selection waveforms. That is, COM_9-COM_{16} are non-selection waveforms at 1/8 duty factor, and COM_{12}-COM_{16} are non-selection waveforms at 1/11 duty factor.
SEG_1-SEG_{40}	40	Output	Liquid crystal display	Segment signal.
V_1-V_5	5		Power supply	Power supply for liquid crystal display drive.
V_{CC}, GND	2		Power supply	V_{CC}: +5 V, GND: 0 V.
OSC_1, OSC_2	2			Terminals connected to resistor or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC_1.

4

Function Of Each Block

Register

The HD44780 has two 8-bit registers, an instruction register (IR), and a data register (DR).
The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.
The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data is read from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Busy flag (BF)

When the busy flag is 1, the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As table 2 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is 0.

Address counter (AC)

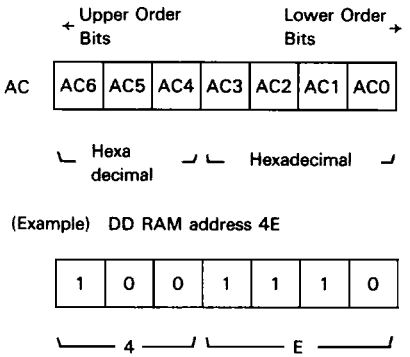
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.
After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output to DB_0 - DB_6 when RS = 0 and R/W = 1, as shown in table 2.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0-DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

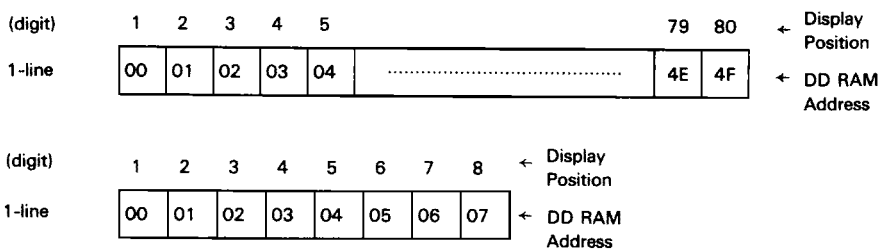
Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.
The DD RAM address (A_{DD}) is set in the address counter (AC) and is represented in hexadecimal.

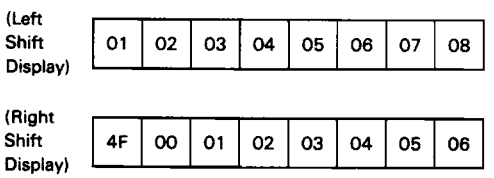


1-Line Display (N = 0)

1. When there are fower than 80 display characters, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:



When the display shift operation is performed, the DD RAM address moves as:



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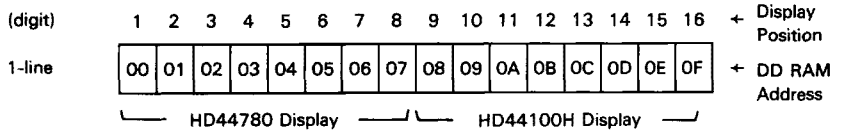
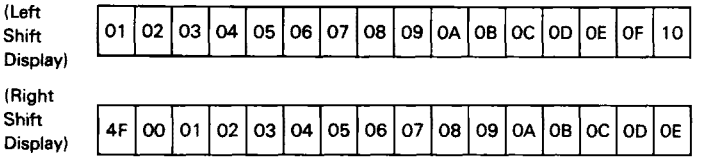
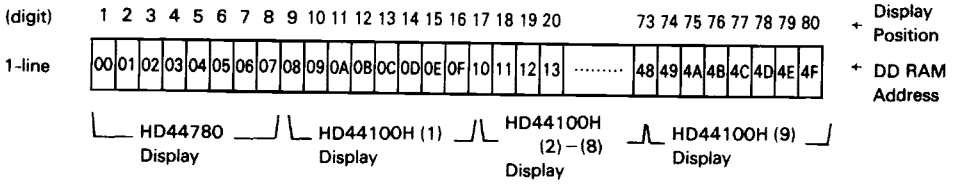
2. 16-character display using an HD44780 and an HD44100H is as shown below:



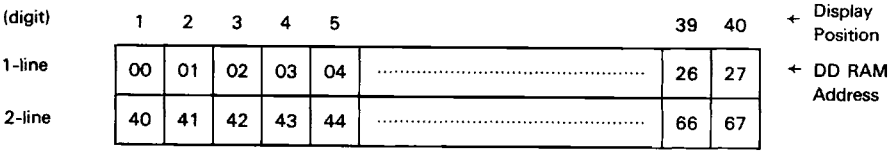
When the display shift operation is performed, the DD RAM address moves as:



3. The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of 2.
Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.



2-Line Display (N = 1)



1. When the number of display characters is less than 40 × 2 lines, the 2 lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

2. 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

HD44780 Display — HD44100H Display

When display shift is performed, the DD RAM address moves as follows:

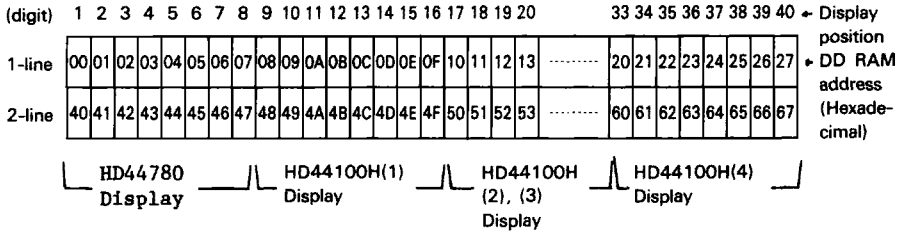
(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

4

3. The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of 2.

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.



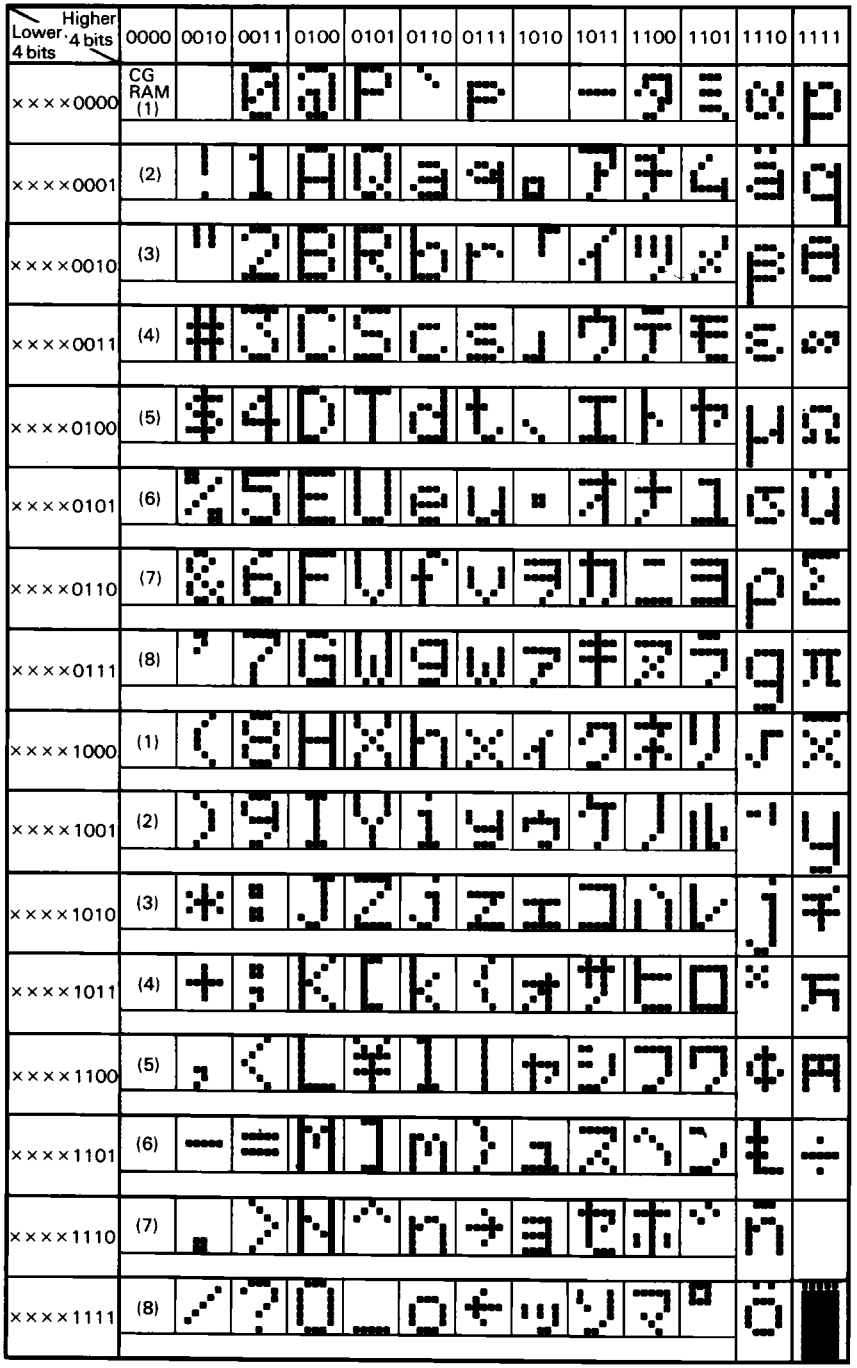
Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 5 × 7 dot character patterns and 32 5 × 10 dot character patterns. Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programmed ROM.

Character Generator RAM (CG RAM)

In the character generator RAM, the user can rewrite character patterns by program. With 5 × 7 dots, 8 character patterns can be written and with 5 × 10 dots, 4 characters can be written.
Write the character codes in the left column of table 3 to display character patterns stored in CG RAM.
Table 4 shows the relation between CG RAM addresses and data and display patterns.
As table 4 shows, an area that is not used for display can be used as a general data RAM.

Table 3 Correspondence between Character Codes and Character Pattern (Hitachi Standard HD44780A00)

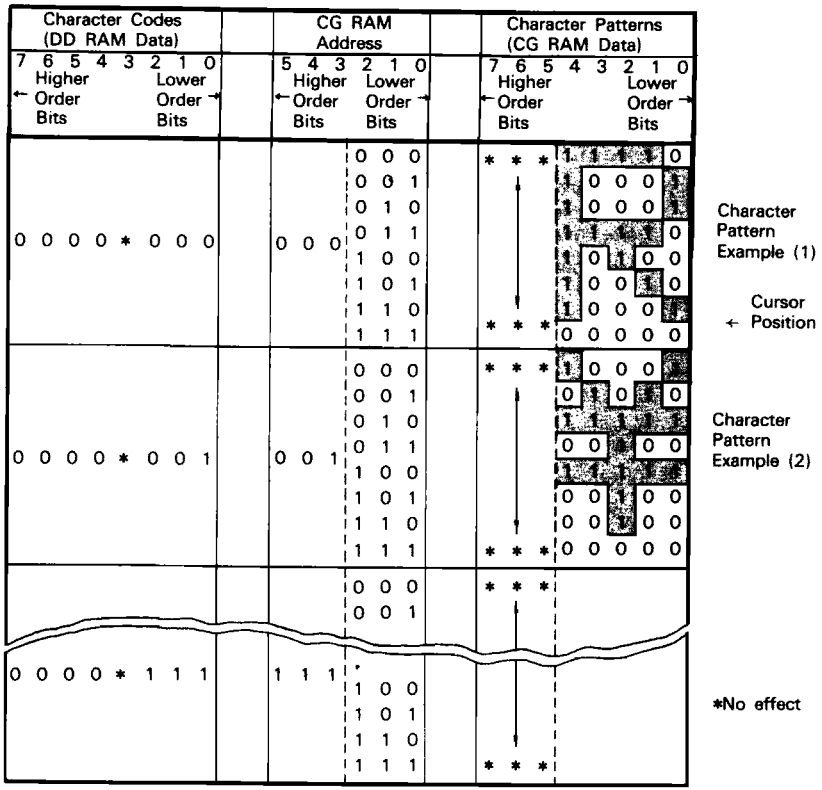


Note: The user can specify any pattern for character-generator RAM.

4

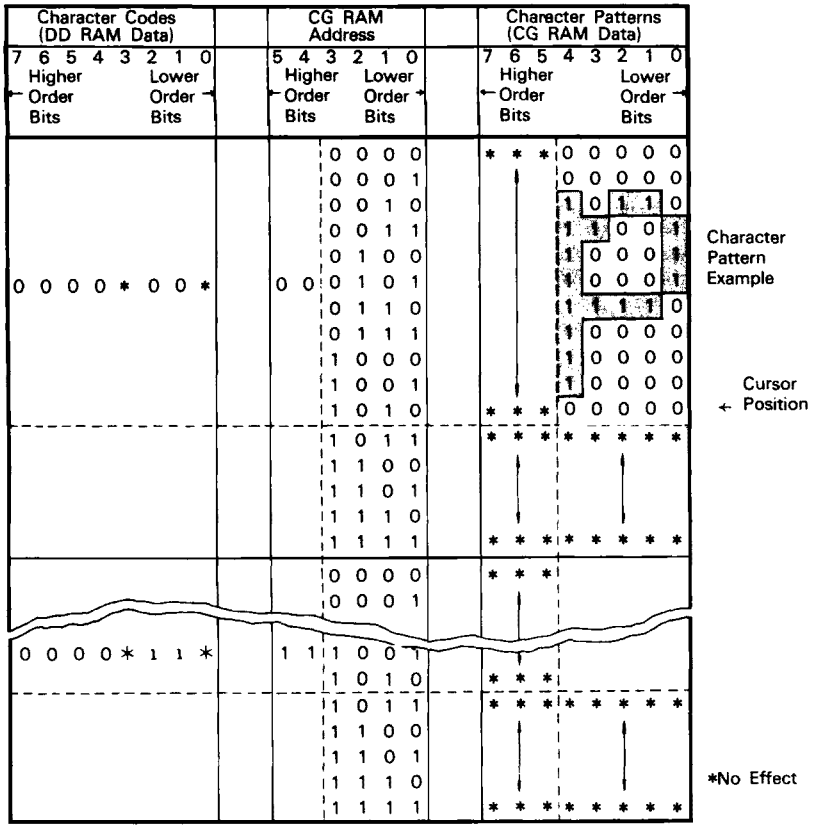
Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

For 5 × 7 dot character patterns



Notes:
1. Character code bits 0-2 correspond to CG RAM address bits 3-5 (3 bits: 8 types).
2. CG RAM address bits 0-2 designate character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.
   Maintain the 8th line data, corresponding to the cursor display position, in the 0 state for cursor display. When the 8th line data is 1, bit 1 lights up regardless of cursor presence.
3. Character pattern row positions correspond to CG RAM data bits 0-4, as shown in the figure (bit 4 being at the left end).
   Since CG RAM data bits 5-7 are not used for display, they can be used for the general data RAM.
4. As shown in table 3, CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 3 has no effect, the "R" display in the character pattern example is selected by character code "00" (hexadecimal) or "08" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

For 5 × 10 dot character patterns



Notes: 1. Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).
2. CG RAM address bits 0-3 designate character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.
Maintain the 11th line data corresponding to the cursor display position in the 0 state for cursor display. When the 11th line data is 1, bit 1 lights up regardless of cursor presence. Since the 12th-16th lines are not used for display, they can be used for general data RAM.
3. Character pattern row positions are the same as 5 × 7 dot character pattern positions.
4. CG RAM character patterns are selected when character code bits 4-7 are all 0. However, since character code bit 0 and 3 have no effect, "P" display in the character pattern example is selected by character codes "00", "01", "08" and "09" (hexadecimal).
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.

Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM, and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

Liquid Crystal Display Driver Circuit

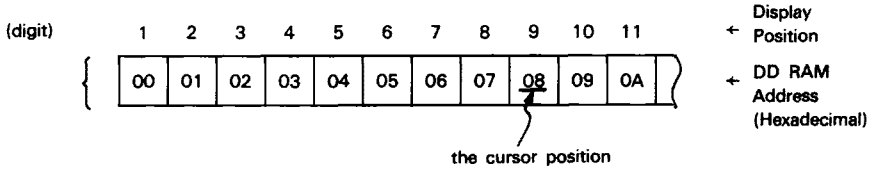
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.
The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs. The serial data can be sent to HD44100Hs, externally connected in cascade, used for display digit number extension.
Serial data send always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).
Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

Cursor/Blink Control Circuit

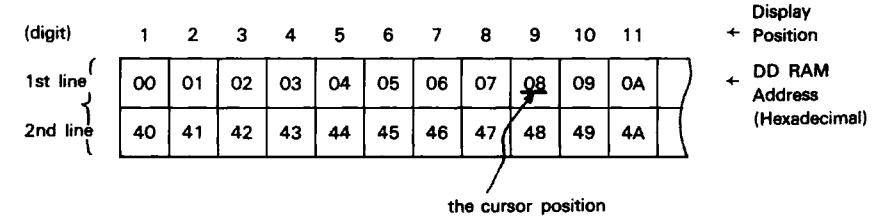
The cursor/blink control circuit generates the cursor or blink. The cursor or the blink appear in the digit at the display data RAM (DD RAM) address set in the address counter (AC).
When the address counter is $(08)_{16}$, the cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



Note: The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is a CG RAM address.

Interfacing To MPU

In the HD44780, data can be sent in either 2 4-bit operations or 1 8-bit operations so it can interface to both 4- and 8-bit MPUs.

1. When interface data is 4-bits long, data is transferred using only 4 buslines: DB_4-DB_7. DB_0-DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4-DB_7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB_0-DB_3 when interface data is 8 bits long) is transferred.
   Check the busy flag after 4-bit data has been transferred twice (one instruction). Two 4-bit operations will then transfer the busy flag and address counter data.

2. When interface data is 8 bits long, data is transferred using the 8 data buslines DB_0-DB_7.

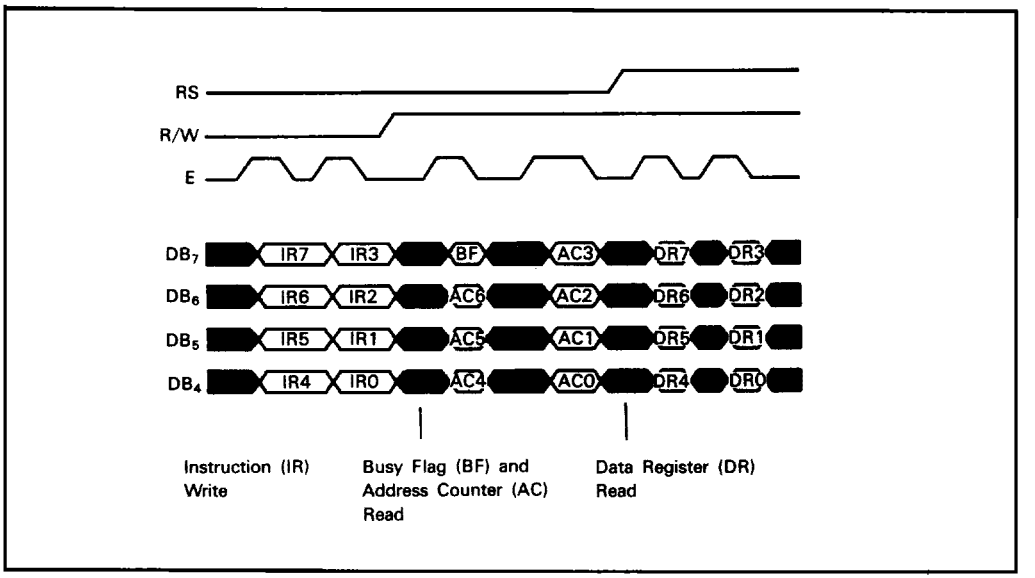


Figure 5 4-Bit Data Transfer Example

4

Reset Function

Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed during initialization. The busy flag (BF) is kept in busy state until initialization ends (BF = 1). The busy state is 10 ms after V_{CC} rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1: 8 bit long interface data
   N = 0: 1-line display
   F = 0: 5 × 7 dot character font
3. Display on/off control:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blink off
4. Entry mode set:
   I/D = 1: +1 (increment)
   S = 0: No shift

Note: When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required. Use the procedure in figures 6 and 7 for initialization.

1:

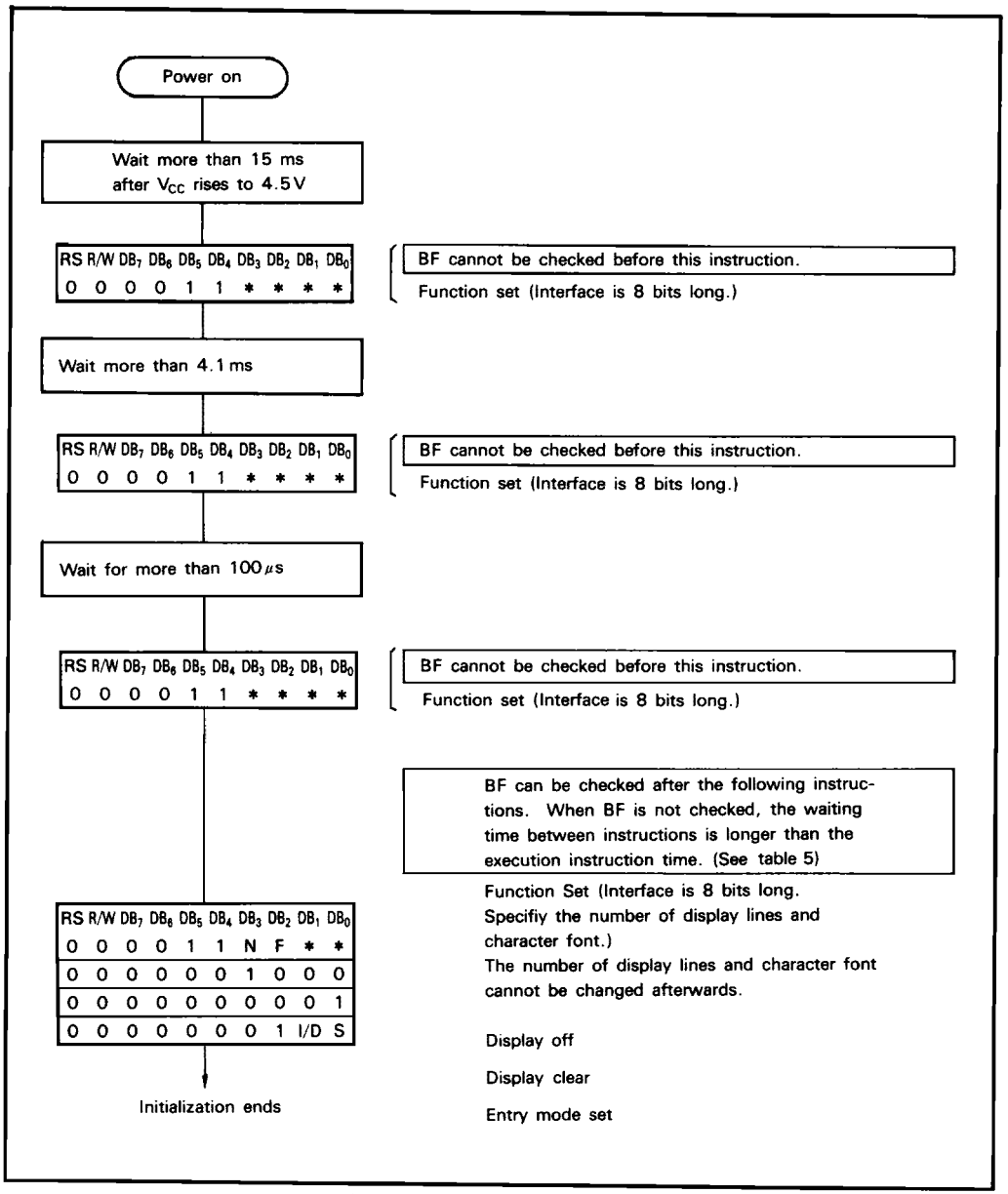


Figure 6 8-Bit Interface

2:

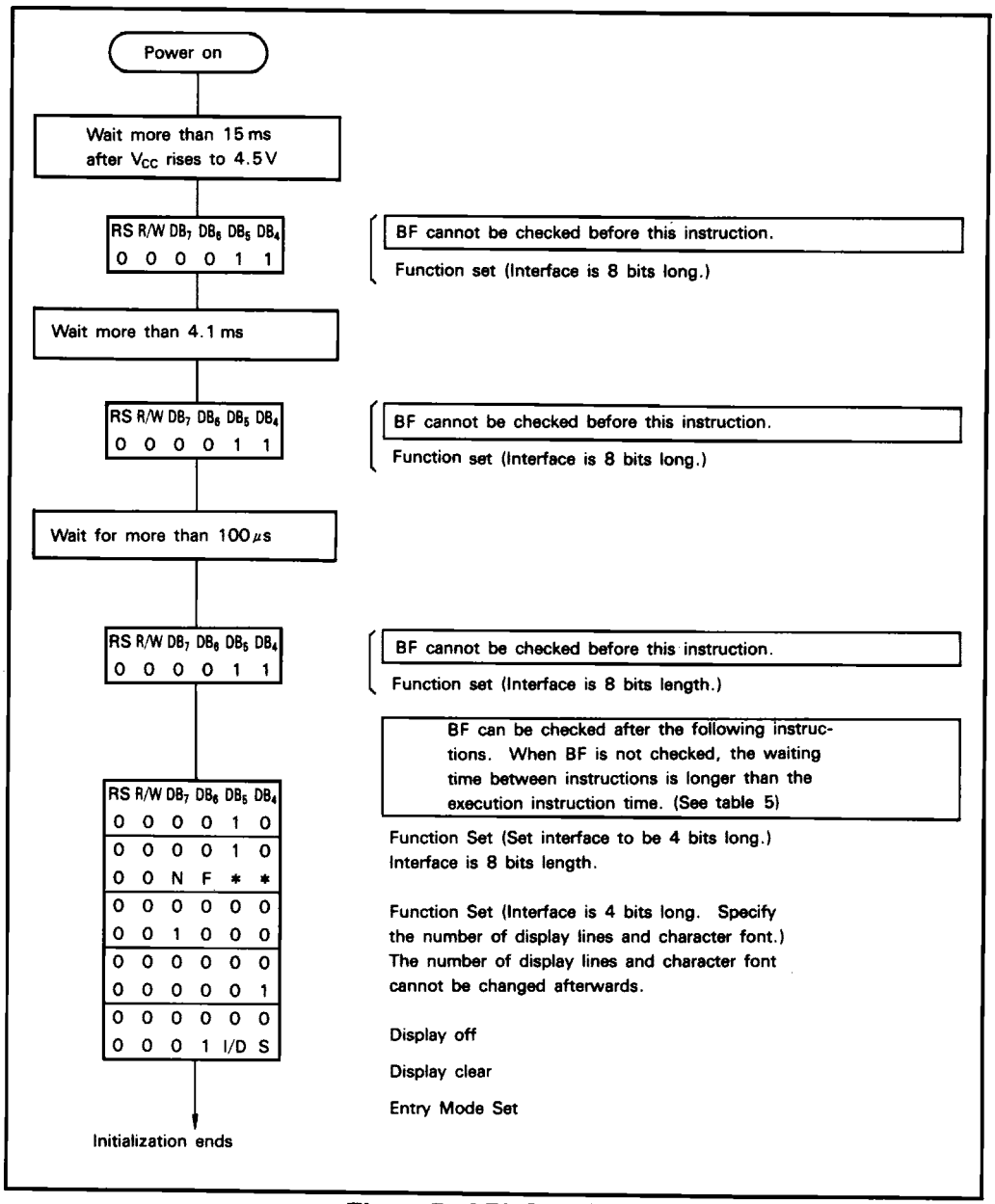


Figure 7 4-Bit Interface

Instructions

Outline

Only two HD44780 registers, the instruction register (IR) and the data register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs that operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals (OB_0-DB_7), and are here called instructions. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

1. Designate HD44780 functions such as display format, data length, etc.
2. Give internal RAM addresses
3. Perform data transfer with internal RAM
4. Others

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift especially can perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see table 7.

When an instruction is executing during internal operation, no insruction other than the busy flag/address read instruction will be executed.

Because the busy flag is set to 1 while an instruction is being executed, check to make sure it is 1 before sending an instruction from the MPU.

Notes: 1. Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See table 5 for a list of each instruction execution time.

2. After execution of a CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off. In figure 7 t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

4

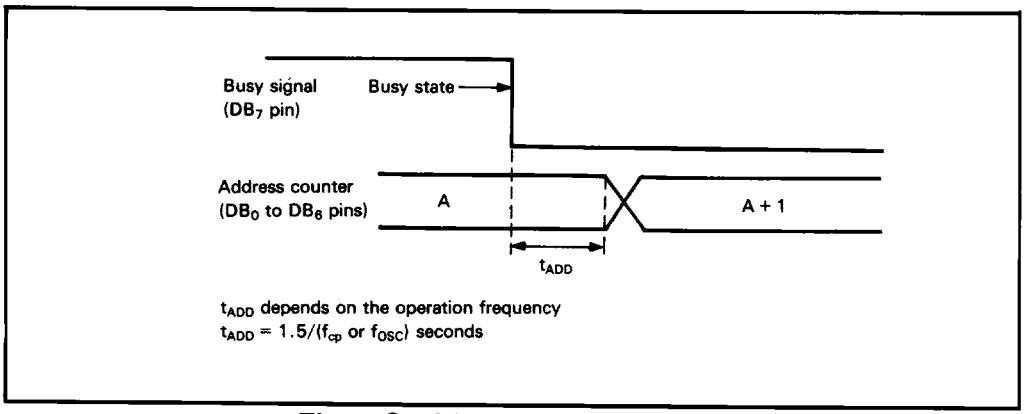


Figure 8 Address Counter Update

Table 5 Instructions

Instruction	Code										Description	Execution Time (max) (when fcp or fosc is 250 kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and recevied after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs t_{ADD} = 6 μs (Note 2)
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40μs t_{ADD} = 6 μs (Note 2)
	I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line F = 1: 5×10 dots, F = 0: 5×7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address: Corresponds to cursor address AC: Adress counter used for both DD and CG RAM address.	Execution time changes when frequency changes Example: When fcp or fosc is 270 kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No effect

Description of Details

1. Clear Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes space code 20 (hexadecimal) (character pattern for character code 20 must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (increment mode) in entry mode. S of entry mode doesn't change.

2. Return Home

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

3. Entry Mode Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

I/O: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.
The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0.
Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM causes a shift when S = 0.

4

4. Display On/Off Control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: The display is on when D = 1 and off when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed instantly by setting D = 1.

C: The cursor is displayed when C = 1 and is not displayed when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5× 10 dot character font is selected (Figure 9).

B: The character indicated by the cursor blinks when B = 1 (Figure 9). The blink is displayed by switching between all blank dots and display characters at 409.6 ms intervals when fcp or fosc = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. 406.9 × $\frac{250}{270}$ = 379.2 ms when fcp = 270 kHz.)

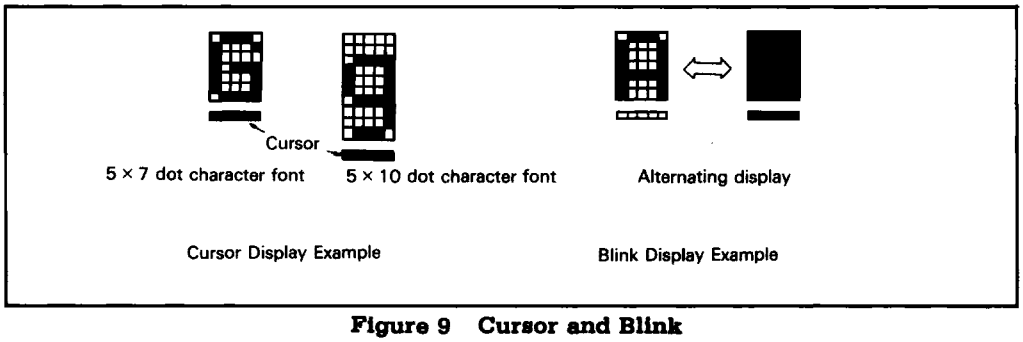


Figure 9 Cursor and Blink

5. Cursor or Display Shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data (Table 6). This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

Address counter (AC) contents do not change if the only action performed is display shift.

6. Function Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* Don't care

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB_7-DB_0) when DL = 1 and in 4 bit lengths (DB_7-DB_4) when DL = 0.

When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

Note: Perform the function at the head of the program before executing any instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

4

Table 6 Shift Function

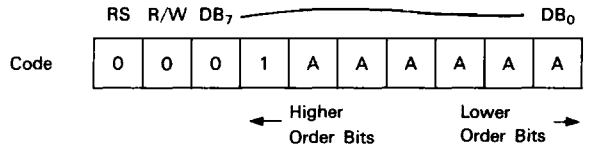
S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Table 7 Function Set

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 7 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 7 dots	1/16	Cannot display 2 lines with 5 × 10 dot character font

* Don't care

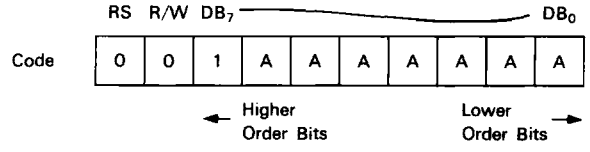
7. Set CG RAM Address



Sets the CG RAM address binary AAAAAA into the address counter.

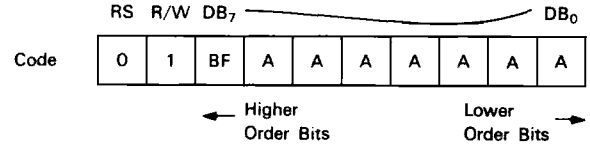
Data is then written or read from the MPU for the CG RAM.

8. Set DD RAM Address



Sets the DD RAM address binary AAAAAAA into the address counter.
Data is then written or read from the MPU for the DD RAM.
However, when N = 0 (1-line display), AAAAAAA can be 00-4F (hexadecimal). When N = 1 (2-line display), AAAAAAA can be 00-27 (hexadecimal) for the first line, and 40-67 (hexadecimal) for the second line.

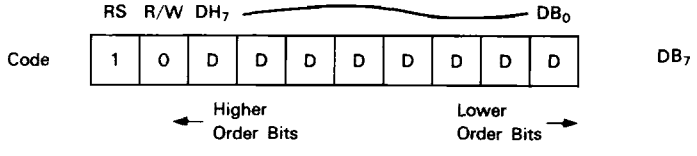
9. Read Busy Flag and Address



Reads the busy flag (BF) that indicates that the system is now internally operating on a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF isset to 0. Check the BF status before the next wire operation.

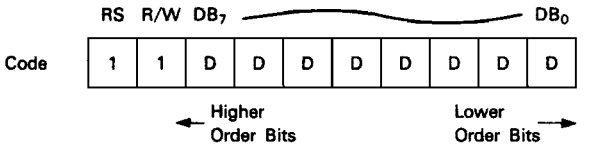
At the same time, the value of the address counter expressed in binary as AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in items 7 and 8.

10. Write Data to CG or DD RAM



Writes binary 8-bit data DDDDDDDD to the CG or the DD RAM.
Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

11. Read Data from CG or DD RAM



Reads binary 8-bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing read instructions, the next address data is normally read from the second read. The address set instruction need not be executed just before the read instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after write instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if read instructions are executed. The conditions for correct data readout are: execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading out execute the "read" instruction from the second time the "read" instruction is sent.

4

How To Use The HD44780

Interface to MPU

1. Interface to 8-Bit MPU

When connecting to 8-bit MPU through PIA
Figure 10 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.
In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively.
Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

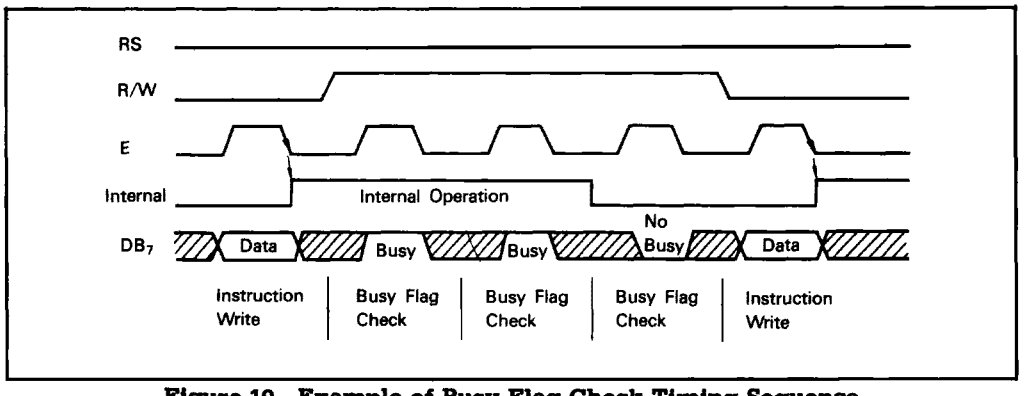


Figure 10 Example of Busy Flag Check Timing Sequence

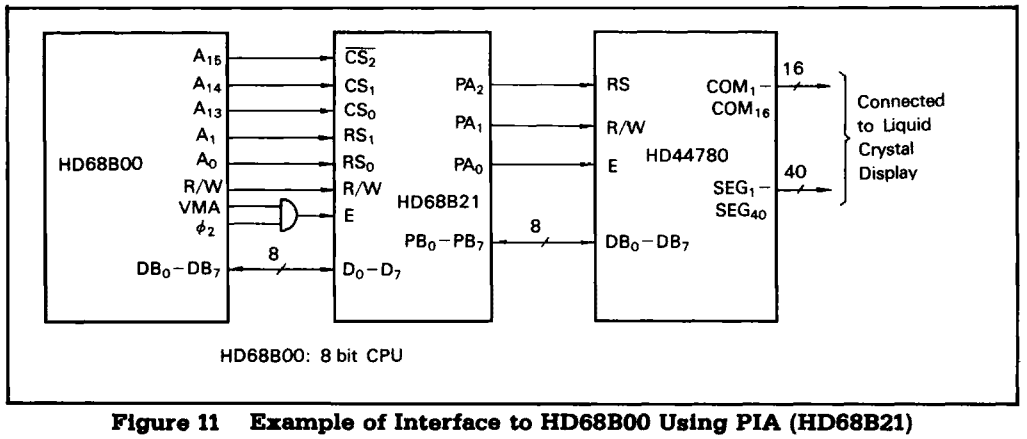


Figure 11 Example of Interface to HD68B00 Using PIA (HD68B21)

Connecting directly to the 8-bit MPU bus line

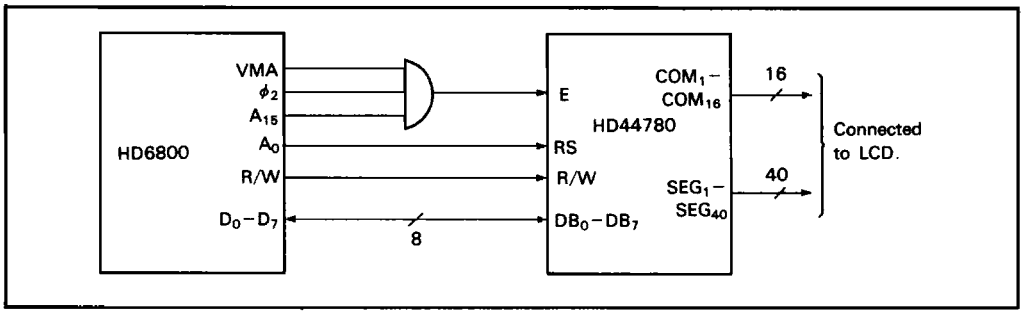


Figure 12 8-Bit MPU Interface

Example of interfacing to the HD6805

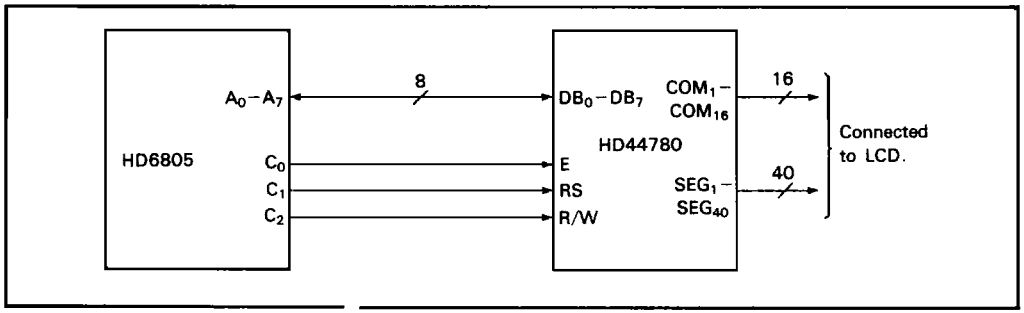


Figure 13 HD6805 Interface

Example of interfacing to the HD6301

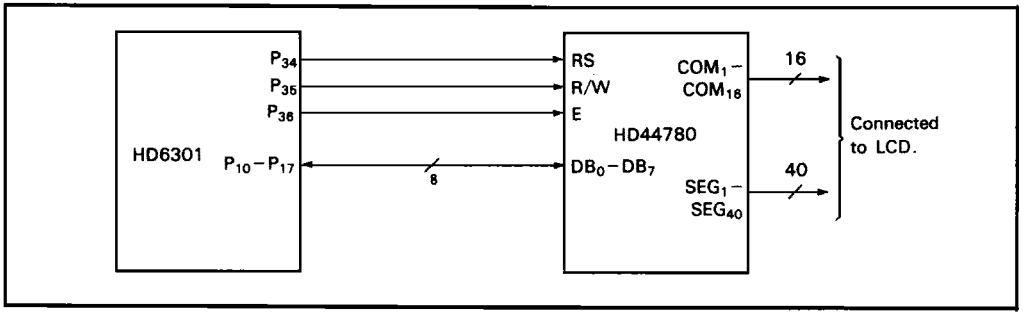


Figure 14 HD6301 Interface

4

2. Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if there are insufficient bits, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See figure 15)

Figure 15 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

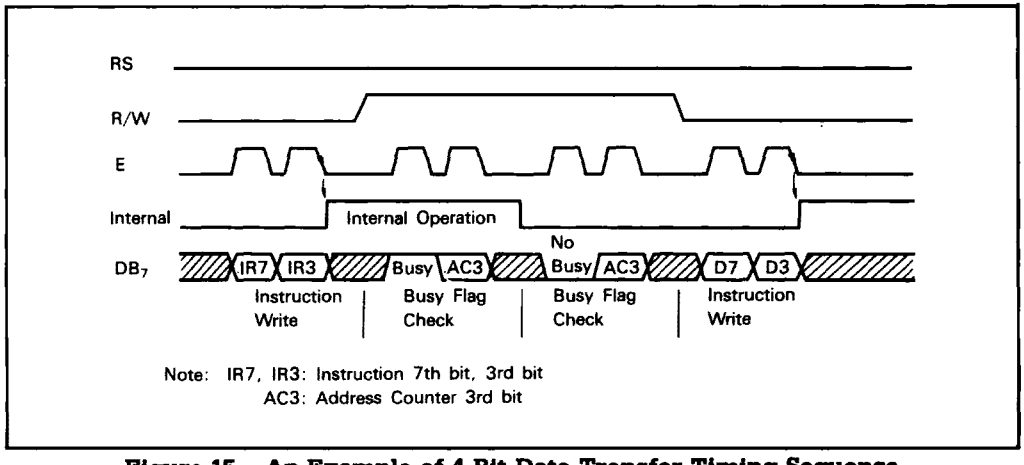


Figure 15 An Example of 4-Bit Data Transfer Timing Sequence

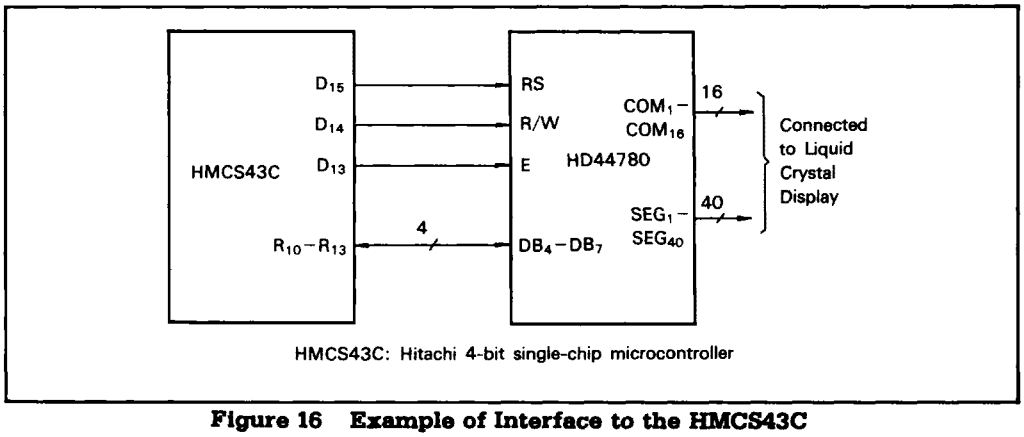


Figure 16 Example of Interface to the HMCS43C

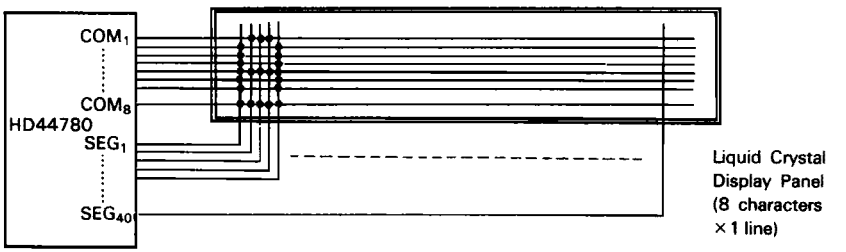
Interface to Liquid Crystal Display

1. Character Font and Number of Lines
   The HD44780 can perform 2 types of display, 5 × 7 dots and 5 × 10 dots character font, with a cursor on each.
   Up to 2 lines are displayed with 5 × 7 dots and 1 line with 5 × 10 dots. Therefore, three types of common signals are available (Table 8).
   Number of lines and font types can be selected by program.
   (See to Table 5, Instructions)

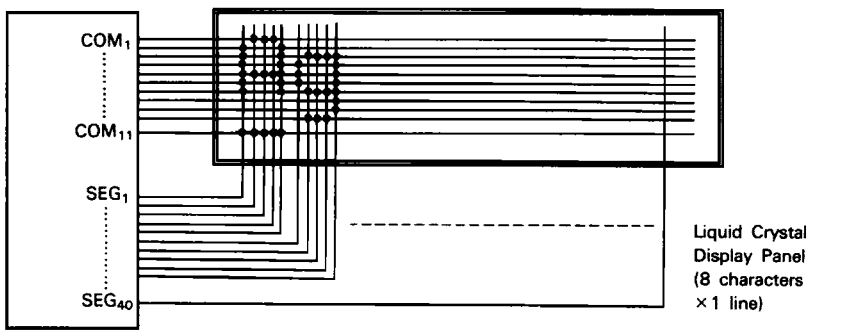
2. Connection to HD44780 and Liquid Crystal Display
   Figure 17 shows connection examples.

Table 8 Common Signals

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 × 7 dots + Cursor	8	1/8
1	5 × 10 dots + Cursor	11	1/11
2	5 × 7 dots + Cursor	16	1/16



(a) Example of a 5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

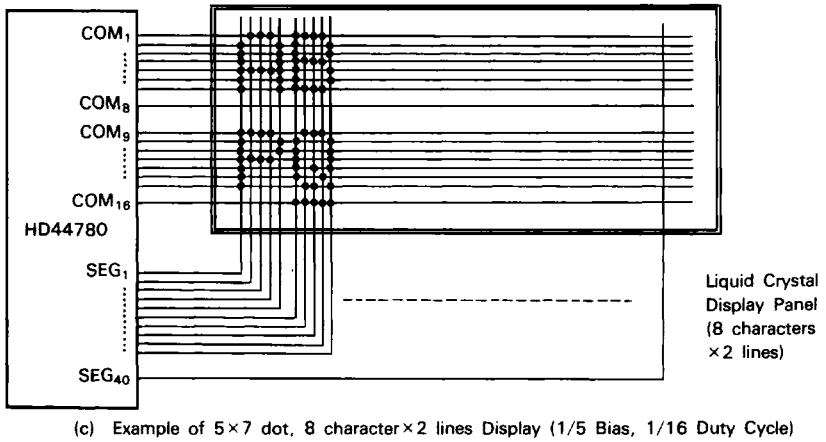


(b) Example of a 5×10 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

Figure 17 Liquid Crystal Display and Connections to HD44780

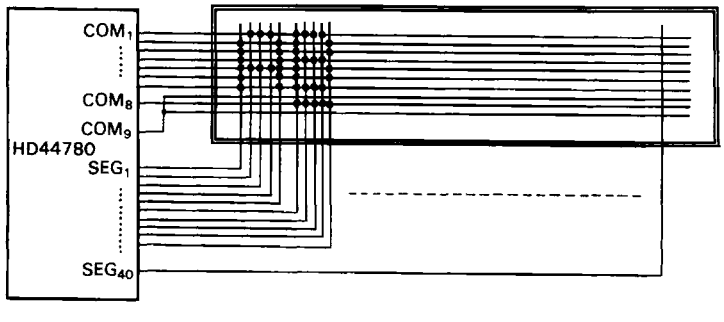
4

Since 5 SEG signal lines can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.
In Figure 15 examples (a) and (b), there are unused common signal terminals, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to crosstalk in the floating state by connecting the extra scanning lines to these common signal terminals (Figure 18).



(c) Example of 5×7 dot, 8 character×2 lines Display (1/5 Bias, 1/16 Duty Cycle)

Figure 17 Liquid Crystal Display and Connections to HD44780 (cont)

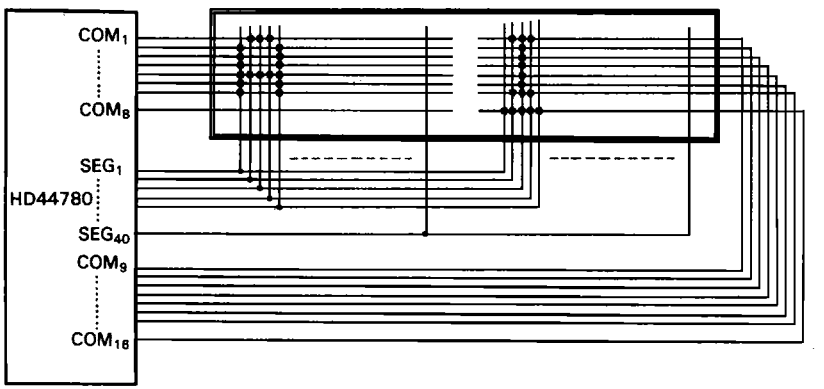


5×7 dot, 8 character×1 line Display (1/4 Bias, 1/8 Duty Cycle)

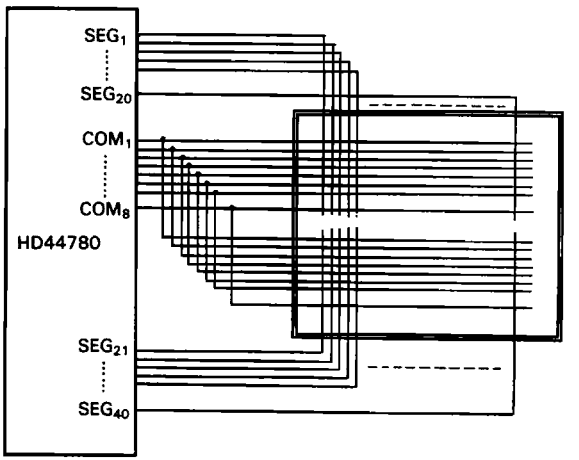
Figure 18 Using COM_9 to Avoid Crosstalk on Unneeded Scanning Line

3. Connection of Changed Matrix Layout

In the preceding examples, the number of lines matched the number of scanning lines. The display types figure 17 are made possible by changing the matrix layout in the liquid crystal display panel. In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters depend on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in figure 15.



5×7 dot, 16 character×1 line Display
(1/5 Bias, 1/16 Duty Cycle)



5×7 dot, 4 character×2 line Display
(1/4 Bias, 1/8 Duty Cycle)

Figure 19 Changed Matrix Layout Displays

4

Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 9 shows the relation.

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in figure 20.

Table 9. Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor / Power Supply Bias	1/8, 1/11 1/4	1/16 1/5
V_1	$V_{CC}-1/4\ V_{LCD}$	$V_{CC}-1/5\ V_{LCD}$
V_2	$V_{CC}-1/2\ V_{LCD}$	$V_{CC}-2/5\ V_{LCD}$
V_3	$V_{CC}-1/2\ V_{LCD}$	$V_{CC}-3/5\ V_{LCD}$
V_4	$V_{CC}-3/4\ V_{LCD}$	$V_{CC}-4/5\ V_{LCD}$
V_5	$V_{CC}-V_{LCD}$	$V_{CC}-V_{LCD}$

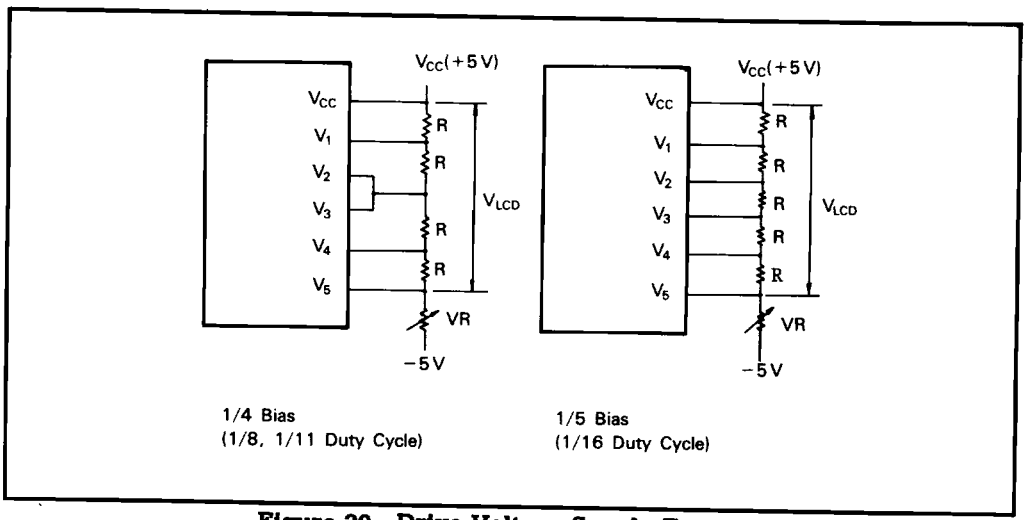
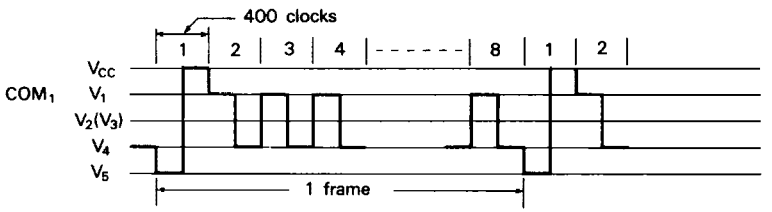


Figure 20 Drive Voltage Supply Example

Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The examples in figure 21 of liquid crystal display frame frequency apply only when oscillation frequency is 250 kHz (1 clock = 4 μs).

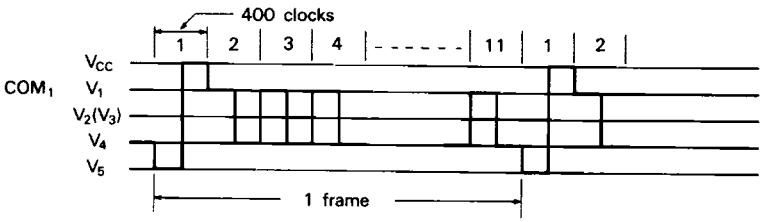
1. 1/8 Duty Cycle



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

Frame frequency = $\frac{1}{12.8\,(\text{ms})}$ = 78.1 (Hz)

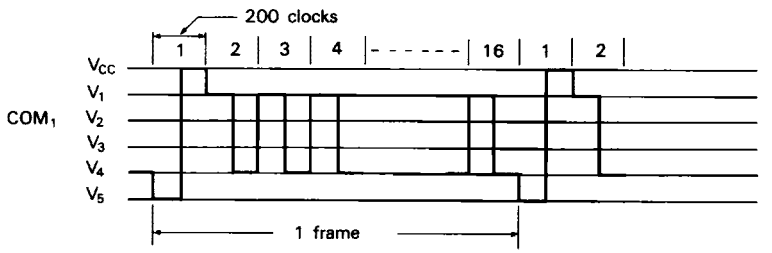
2. 1/11 Duty Cycle



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

Frame frequency = $\frac{1}{17.6\,(\text{ms})}$ = 56.8 (Hz)

3. 1/16 Duty Cycle



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

Frame frequency = $\frac{1}{12.8\,(\text{ms})}$ = 78.1 (Hz)

Figure 21 Frame Frequency

4

Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting an HD44100H liquid crystal display driver LSI to the HD44780. When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M, and D signals and power for liquid crystal display drive. Figure 22 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 HD44100H units can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in figure 22 remains unchanged for both 1-line and 2-line display or 5 × 7 and 5 × 10 dot character fonts.

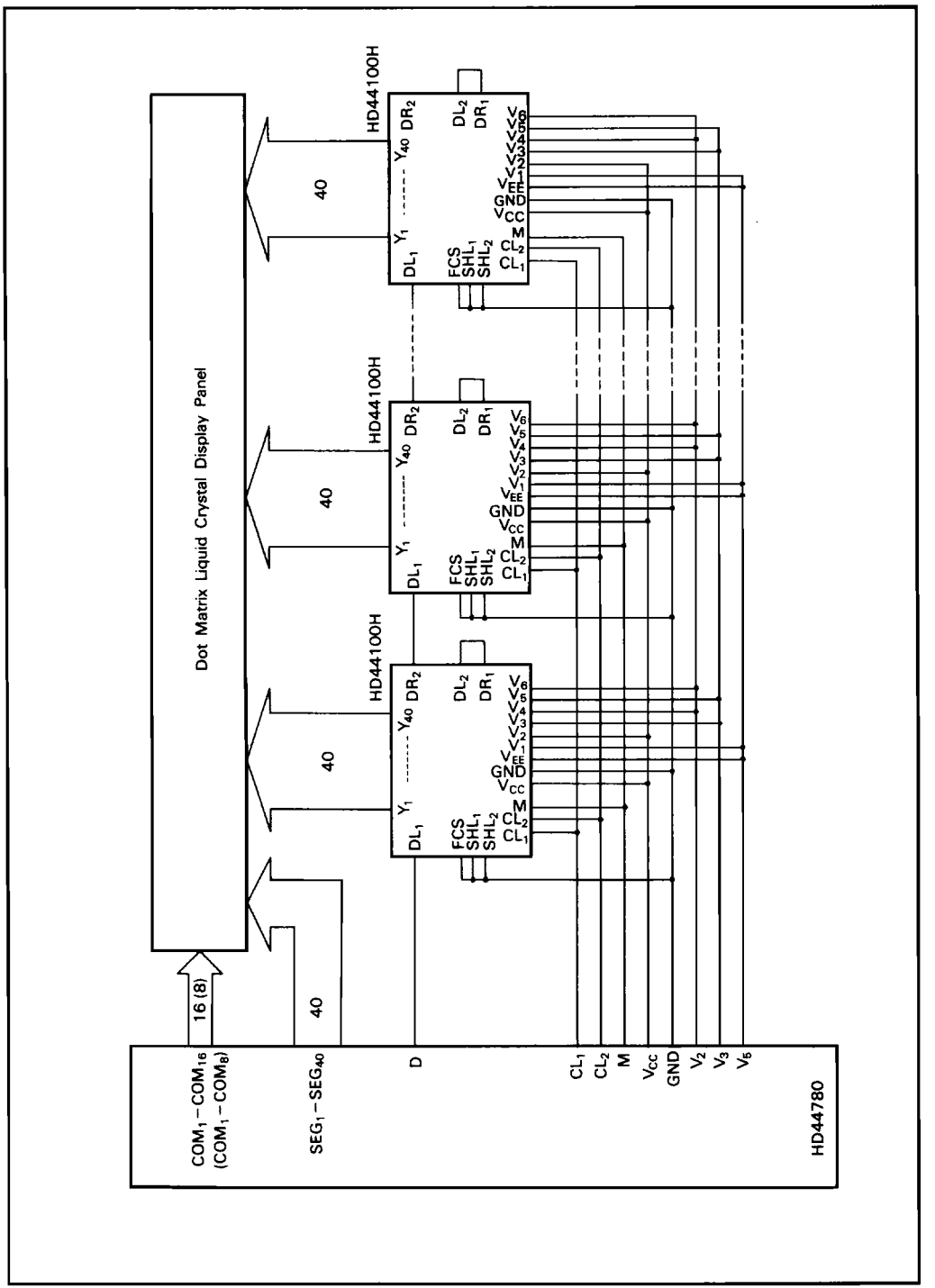


Figure 22 Example of Connecting HD44100H to HD44780

Instruction and Display Correspondence

1. 8-bit operation, 8-digit × 1-line display (using internal reset)

   Table 10 shows an example of 8-bit × 1-line display in 8-bit operation. The HD44780 functions must be set by funtion set instruction prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like a lighting board when combined with display shift operation.
   Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

2. 4-bit operation, 8-digit × 1-line display (using internal reset)

   The program must set functions prior to 4-bit operation. Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to DB_0-DB_3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see table 11). Thus, DB_4-DB_7 of the function set is written twice.

3. 8-bit operation, 8-digit × 2-line display

   For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See table 12). Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Note: When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by insruction. (See "Initializing by Instruction")

Table 10 8-Bit Operation, 8-Digit 1-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed after this.)
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	. . . . .	. . . . .	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	. . . . .	. . . . .	

4

No.	Instruction	Display	Operation
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "O".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO_	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO_	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO_	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO_	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts the display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	. . . . .	. . . . .	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 11 4-Bit Operation, 8-Digit 1-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ⁓ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display On/Off Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 12 8-Bit Operation, 8-Digit × 2-Line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply on (HD44780 is intialized by the internal reset circuit)		Initalized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.
3	Display On/Off Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	:	:	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift operate at the same time.
14	:	:	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

4

Modifying Character Patterns

1. Character Pattern Development Procedure

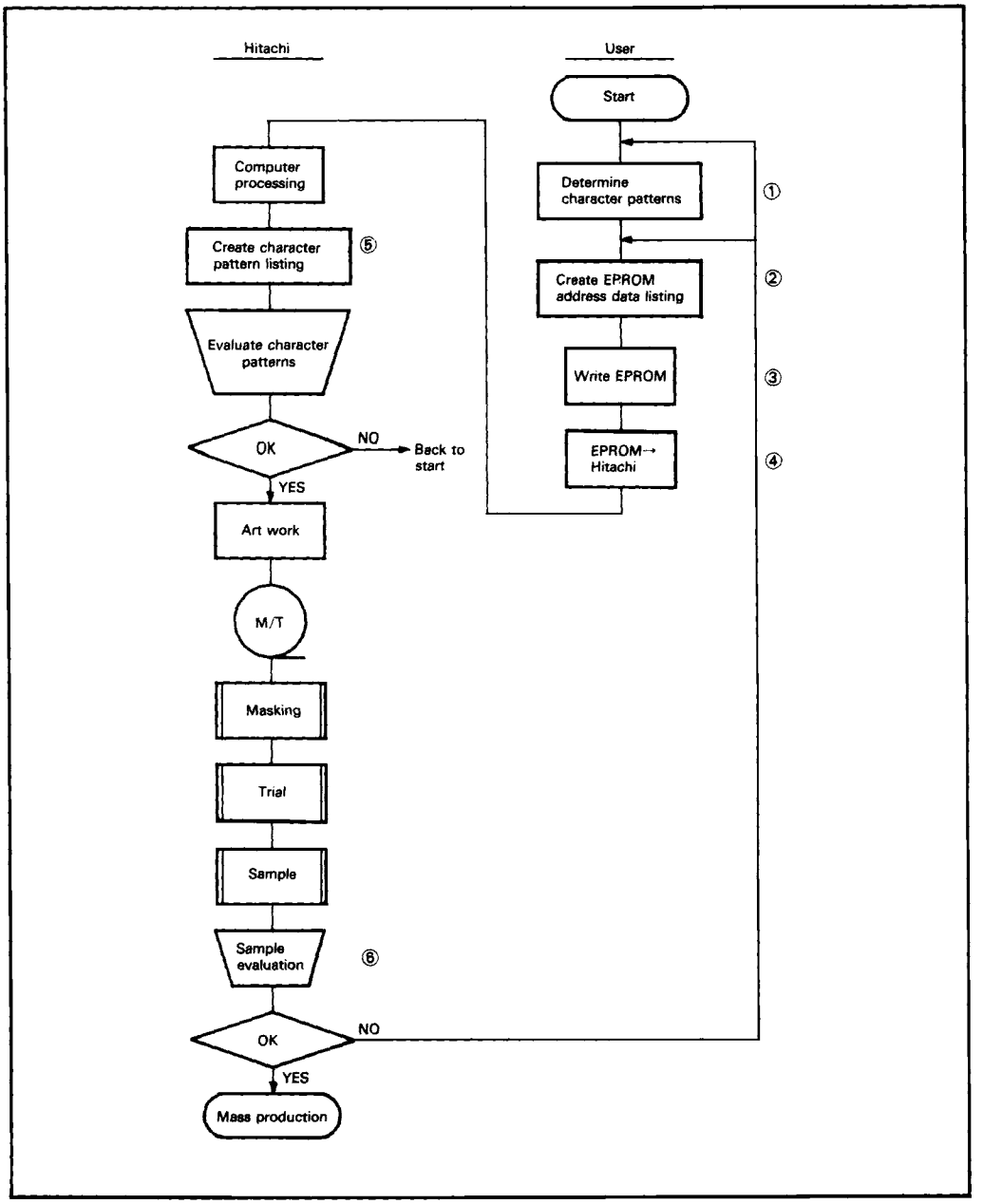


Figure 23 Character Pattern Development Procedure

The numbers in figure 17 correspond to the following operations:

a. Determine the correspondence between character codes and character patterns.

b. Create a listing indicating the correspondence between EPROM addresses and data.

c. Program character patterns in the EPROM.

d. Send the EPROM to Hitachi.

e. Hitachi performs computer processing with the EPROM to create a character pattern listing and sends it to the user.

f. If there is no problem in the character pattern listing, Hitachi creates a trial LSI and sends samples to the user. The user evaluates the samples. When it is confirmed that character patterns are correctly written, Hitachi starts mass production of the LSI.

2. Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The LCD-II character generator ROM can generate 160 5 × 7-dot character patterns and 32 5 × 10-dot character patterns for a total of 192 different character patterns.

a. 5 × 7-dot Character Pattern

For a 5×7-dot character pattern, EPROM address data and character pattern correspond with each other as shown below. Table 13 is an example of the correspondence between EPROM address data and character pattern (5 × 7 dots).

Table 13 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 7 dots)

EPROM address											Data				
															(LSB)
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	0	0	1	0	0	0	0	1	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	1	0	0	0	1
								0	1	1	1	1	1	1	0
								1	0	0	1	0	1	0	0
								1	0	1	1	0	0	1	0
								1	1	0	1	0	0	0	1
								1	1	1	0	0	0	0	0

Fill line 8 (cursor position) with 0

Character code

Line position

(1) EPROM addresses A_{10} to A_3 correspond to a character code.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 8 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

b. 5 × 10-dot Character Pattern

For a 5×10-dot character pattern, EPROM address data and character pattern correspond with each other as shown in table 14.

(1) EPROM addresses A_{10} to A_3 correspond to a character code. Set A_8 and A_9 of character pattern line 9 and later lines to 0.
(2) EPROM addresses A_2 to A_0 specify a line position of character pattern.
(3) EPROM data O_4 to O_0 correspond to character pattern data.
(4) A lit display position (black) corresponds to 1.
(5) Fill line 11 (cursor position) of character pattern with 0.
(6) EPROM data O_5 to O_7 are not used.

c. Handling Unused Character Patterns

(1) EPROM data outside the character pattern area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(2) EPROM data in CG RAM area
Ignored by the character generator ROM for display operation so it can be 0 or 1.

(3) EPROM data used when the user does not use any LCD-II character pattern
Handled in one of the two ways explained below. Select one of the two ways according to the user application.

(a) When unused character patterns are not programed
If an unused character code is written in the LCD-II DD RAM, all dots are lit. No programming for a character pattern is equivalent to all bits lit. (This is because EPROM is filled with 1 when the EPROM is erased.)

(b) Program 0 for unused character patterns
Nothing is displayed even if unused character codes are written in LCD-II DD RAM. (This is equivalent to space).

Table 14 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 dots)

EPROM address											Data				
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1 (LSB)	O_0
								0	0	0	0	0	0	0	0
								0	0	1	0	0	0	0	0
								0	1	0	0	1	1	0	1
1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1
								1	0	0	1	0	0	0	1
								1	0	1	1	0	0	0	1
								1	1	0	0	1	1	1	1
								1	1	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0

Character code

Line position

Fill line 11 (cursor position) with 0.