

CERAMIC SMD CRYSTAL CLOCK OSCILLATOR



7.0 x 5.0 x 1.8mm

ABNM SERIES

RoHS
Compliant

FEATURES:

- Low Jitter (<20pS P-P typ.)
- Low Phase Noise (<0.5pS typ, 12kHz to 20MHz)
- Low Power (2.5V to 3.3V)
- CMOS, LVPECL or LVDS output

APPLICATIONS:

- SONET, PCI Express, SERDES, Video
- Anywhere Low Jitter is required

STANDARD SPECIFICATIONS:

PARAMETERS

Frequency Range	9.5MHz to 130MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	-55°C to +125°C
Overall Frequency Stability	± 50 ppm max. (see options)
Supply Voltage (Vdd)	2.25V to 3.63V
Jitter (12KHz-20MHz)	RMS phase jitter = 0.5pS typ, <1ps max.
Period Jitter	< 30pS peak to peak typ., 40pS max.
Phase Noise (77.76MHz)	-75 dBc/Hz @ 10Hz; -95 dBc/Hz @ 100Hz; -125 dBc/Hz @ 1kHz -143 dBc/Hz @ 10kHz; -145 dBc/Hz @ 100kHz
Tri-State Function	"1" (VIH > 0.7* Vdd) or open: Oscillation; "0" (VIL < 0.3* Vdd): No oscillation/Hi Z
Optional PECL OE	"0" (Vih < 0.3* Vdd) or Open: Oscillation; "1" (VIH > 0.7* Vdd): No Oscillation/Hi Z

PECL

Supply Current (IDD)	100mA max
Symmetry (Duty Cycle)	45% min, 50% typical, 55% max.
Output Logic High	V _{DD} -1.025V min, V _{DD} -0.880V max.
Output Logic Low	V _{DD} -1.810V min, V _{DD} -1.620V max.
Rise time	850pS max, 500pS typ.

LVDS

Supply Current (IDD)	80mA max
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V _{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV _{OD})	-50mV min, 50mV max
Output High Voltage	V _{OH} = 1.6V max, 1.4V typical
Output Low Voltage	V _{OL} = 0.9V min, 1.1V typical
Offset Voltage [R _L = 100Ω]	V _{OS} = 1.125V min, 1.2V typical, 1.375V max
Offset Magnitude Voltage[R _L = 100Ω]	ΔV _{OS} = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I _{OXD}) [Vout=VDD or GND, VDD=0V]	±10μA max, ±1μA typical
Differential Clock Rise Time (t _r) [R _L =100Ω, CL=10pF]	0.2ns min, 0.7ns typical, 1.0ns max
Differential Clock Fall Time (t _f) [R _L =100Ω, CL=10pF]	0.2ns min, 0.7ns typical, 1.0ns max

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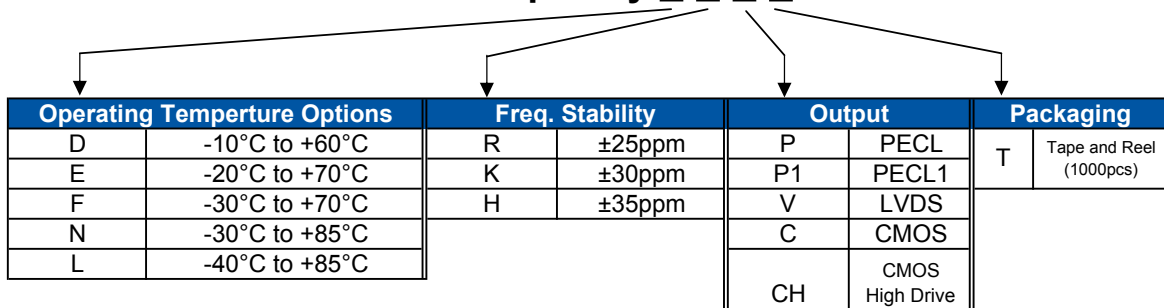
STANDARD SPECIFICATIONS (cont'd):

CMOS	
Supply Current (I _{DD})	40mA max
Output Clock Duty Cycle @ 50% V _{DD}	45% min, 50% typical, 55% max
Output High Voltage (V _{OH}) [I _{OH} =8.5mA]	2.4V max
Output Low Voltage (V _{OL}) [I _{OL} =8.5mA]	0.4V max
Output Drive Current - Standard Drive (I _{OSD}) [V _{OL} =0.4V, V _{OH} =2.4V]	10mA Min
Output Drive Current - High Drive (I _{OSD}) [V _{OL} =0.4V, V _{OH} =2.4V]	30mA Min
Output Clock Rise/Fall Time - Standard Drive [10%~90% VDD with 15pF load]	2.4nS typical
Output Clock Rise/Fall Time - High Drive [10%~90% VDD with 10pF load]	1.2nS typical
Output Clock Duty Cycle [Measured @ 50% VDD]	45% min, 50% typical, 55% max

OPTIONS AND PART IDENTIFICATION

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ABNM-Frequency-□-□-□-□



PIN ASSIGNMENTS

PIN #	Name	DESCRIPTION
1	Tri-state	Tristate
2	NC	No Connect
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output.
5	Q	Complimentary PECL, LVDS, or NC.
6	V _{DD}	VDD Connection.

TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION		PIN 1 logic level*	Output State
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1	Enabled
		0	Tri-state
V,C & CH	LVDS, CMOS, CMOS High Drive	0	Tri-state
		1(Default)	Enabled

*Connect to VDD for logic level "1", connect to ground for logic level "0".

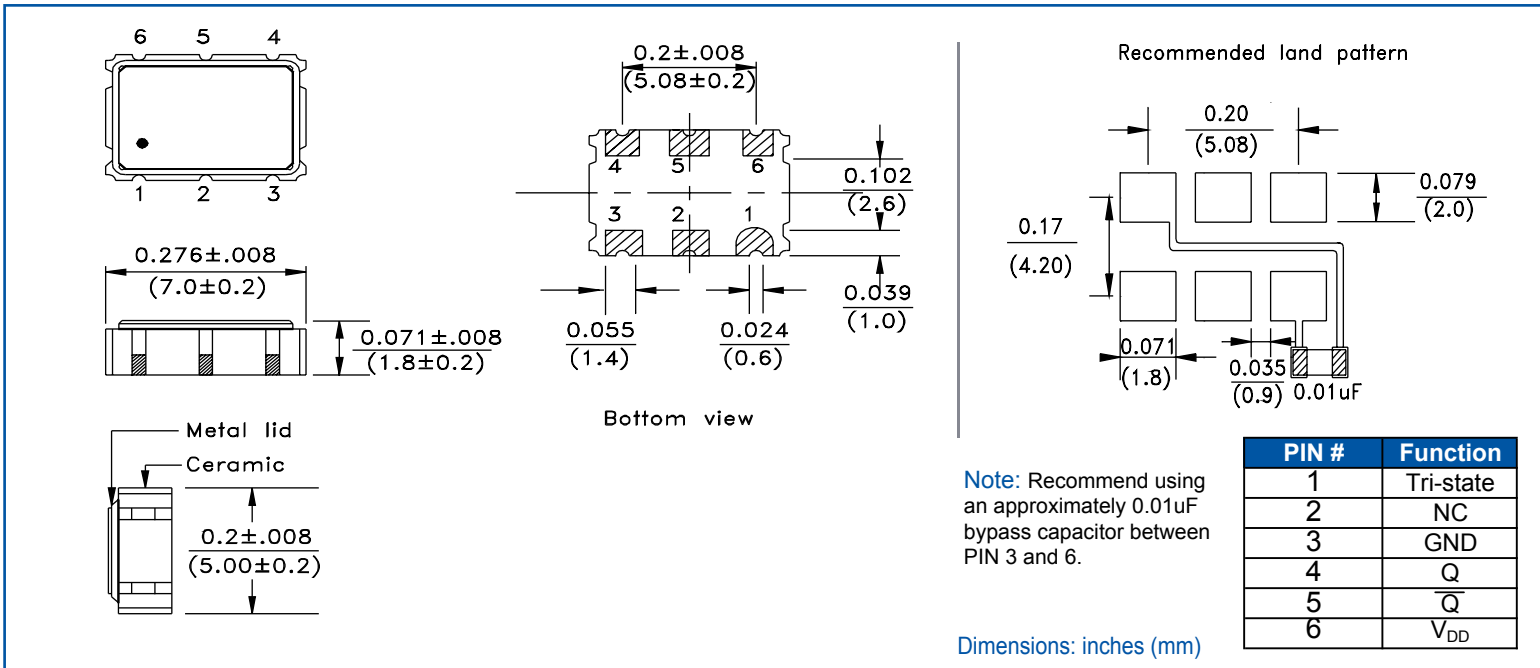
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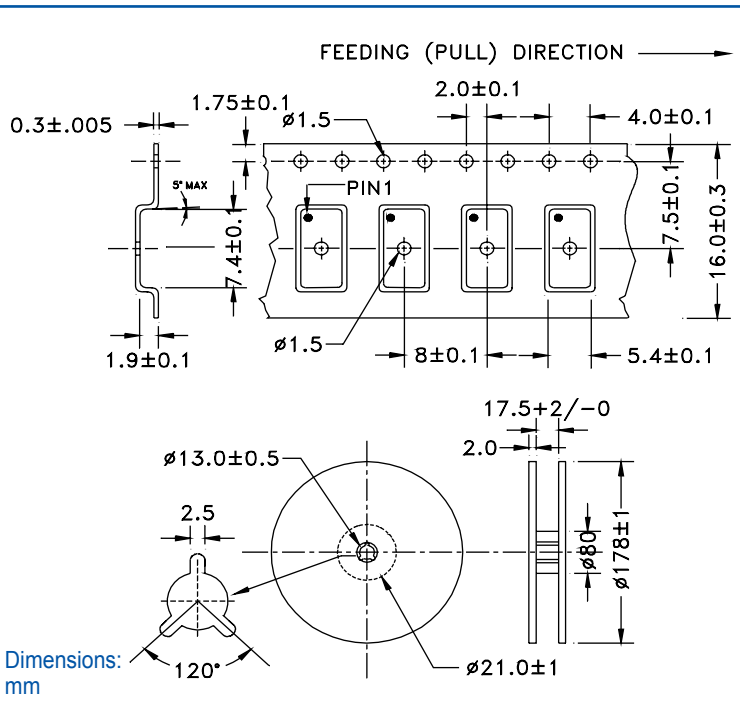
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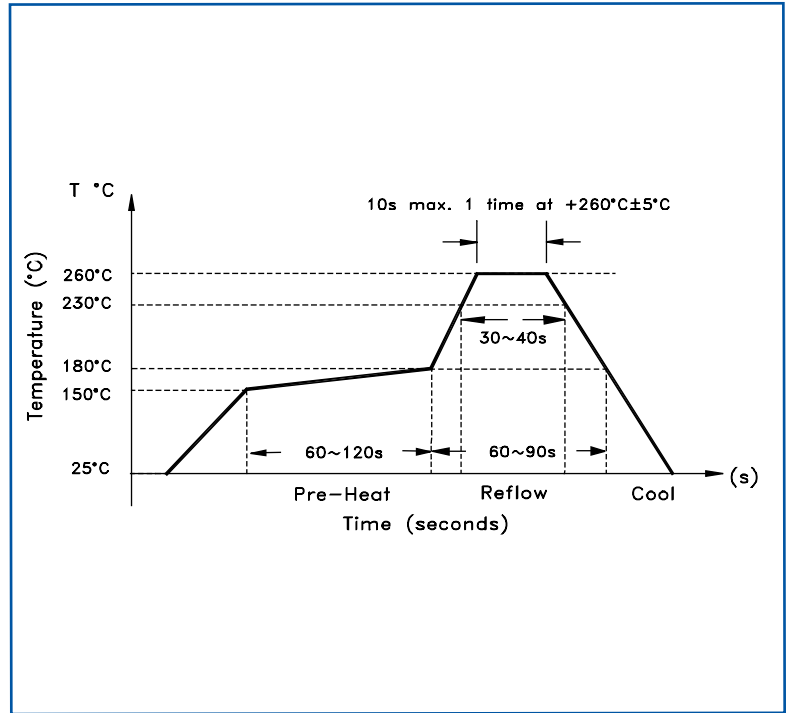
OUTLINE DRAWING:



TAPE & REEL: T = Tape and reel 1,000pcs/reel



REFLOW PROFILE:



Need a test socket for the ABNM Series? To view compatible **PRECISION TEST & BURN-IN SOCKETS** for these parts, [click here](#).

NOTE: Abracon manufactured products are intended for general commercial and industrial use. For applications requiring high reliability and/or presenting extreme operating environment, written consent & authorization from Abracon is required.

ABRACON IS
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CERTIFIED



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30332 Esperanza, Rancho Santa Margarita, California 92688
tel 949-546-8000 | fax 949-546-8001 | www.abracon.com