NEC

MOS INTEGRATED CIRCUIT

μPD16623

240-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALE)

The μPD16623 is a TFT-LCD source driver compatible with 64 gray scale displays.

Along with its digital data input consisting 6 bits by 3 dots, the driver can realize a full-color display of 260,000 colors based on γ-corrected power output of 64 values by means of an internal D/A converter and nine external power supplies.

The clock frequency is 33 $MHz_{MIN.}$, which is applicable to VGA-standard TFT-LCD panels.

FEATURES

- Capable of power output of 64 values by means of nine external power supplies and a D/A converter.
- Capable of γ-corrected power level inversion
- *Output voltage range:* 4.8 $V_{P-P\ MAX.}$ *(when the driver part supply voltage* V_{DD1} = 5.0 V)
- CMOS level input
- Input of 6 bits (gray scale data) × 3 dots
- High-speed data transfer: $f_{max.}$ = 33 MHz (Internal data transfer rate when the logic part supply voltage V_{DD1} = 3.0 V)
- 240 outputs
- Equipped with slim TCP

ORDERING INFORMATION

Part Number	Package
μPD16623N-×××	TCP (TAB package)

Remark Because the TCP's external shape is customized, please consult an NEC salesperson for further details in this regard.

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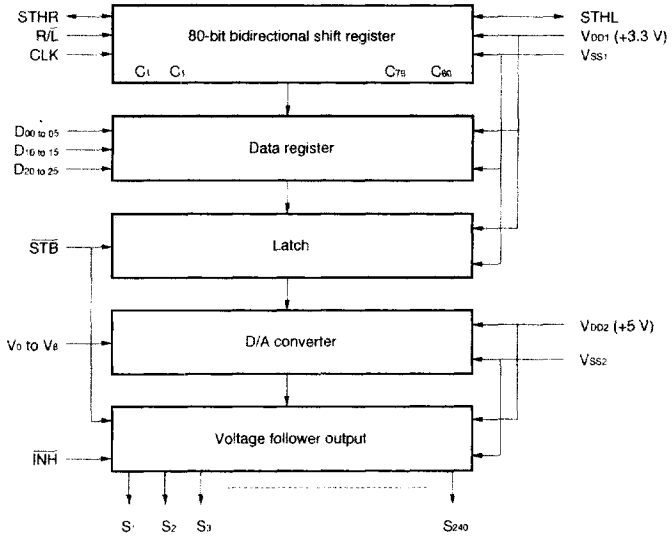
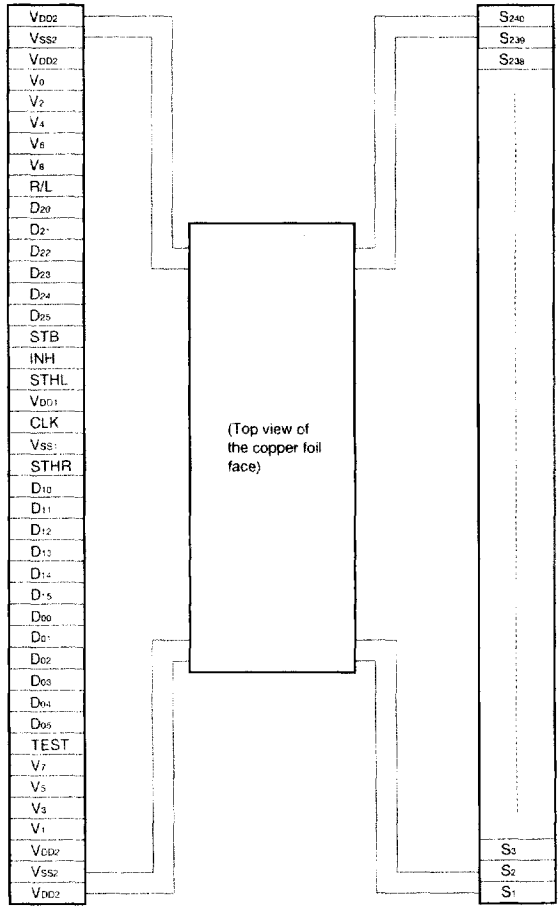
1. BLOCK DIAGRAM



2. **PIN CONFIGURATION** (Since the μPD16623's standard TCP is not available, please refer to the μPD16622N-053 for functional assessment purposes.)



Remark This figure is not an external view of the device.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{240}	Driver output	D/A-converted analog voltage of 64 gray scale is output.
D_{B0} to D_{B5} D_{G0} to D_{G5} D_{R0} to D_{R5}	Display data input	Display data is entered with the width of 18 bits of gray scale data (6 bits) × 3 dots (RGB) D_{x0}: LSB, D_{x5}: MSB
R/$\overline{L}$	Shift direction switching input	Refers to the start pulse input/output pin in cascading. The shift directions of the shift registers are as follows: R/$\overline{L}$ = H: STHR input; $S_1 \rightarrow S_{240}$; STHL output R/$\overline{L}$ = L: STHL input; $S_{240} \rightarrow S_1$; STHR output
STHR	Right shift start pulse input/output	R/$\overline{L}$ = H: Becomes the start pulse input pin. R/$\overline{L}$ = H: Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R/$\overline{L}$ = H: Becomes the start pulse output pin. R/$\overline{L}$ = L: Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift clock input of the shift register. At the rising edge, this pin reads the display data into the data register. At the 80th clock since input of the start pulse, the start pulse output is driven high to become the start pulse of the next-level driver. The 80th clock of the first-level driver becomes the start pulse input of the next-level driver.
$\overline{STB}$	Latch input	At the rising edge, this pin latches the contents of the data register, transfers them to the D/A converter, and then precharges the driver output. After $\overline{STB}$ input, the contents of the internal shift register are cleared. When started up, it operates normally after input of 1 pulse. For details of the $\overline{STB}$'s input timing, please refer to **Relationship Between $\overline{STB}$, Start Pulse (STHR, STHL) and Blanking Period**, which describes switching characteristic waveforms.
$\overline{INH}$	Inhibit input	The driver which is placed in the precharge state by the $\overline{STB}$ outputs the analog value corresponding to the display data at the rising edge of $\overline{INH}$. For details of the $\overline{INH}$ input timing, please refer to the switching characteristic waveforms.
V_0 to V_8	γ-corrected power supply	Inputs the γ-corrected power from outside. $V_{SS2} \leq V_0 \leq V_1 \leq V_2 \leq V_3 \leq V_4 \leq V_5 \leq V_6 \leq V_7 \leq V_8 \leq V_{DD2}$ or $V_{SS2} \leq V_8 \leq V_7 \leq V_6 \leq V_5 \leq V_4 \leq V_3 \leq V_2 \leq V_1 \leq V_0 \leq V_{DD2}$ During gray scale voltage output, make sure to retain the gray scale level power. When shifting the γ-corrected power during the precharged period, ensure that this power is stable before securing the precharge period t_{PCH}.
TEST	Test pin	Place the pin at "H".
V_{DD1}	Logic part power	3.3 V ±0.3 V
V_{DD2}	Driver part power	5.0 V ±0.5 V
V_{SS1}	Logic ground	Ground
V_{SS2}	Driver ground	Ground

Caution For prevention of latch-up breakdown, the power must be applied in order of V_{DD1}, logic input, V_{DD2}, and then gray scale power (V_0 to V_8). Powering-OFF is carried out in the reverse order. Be sire to observe this sequence even during the period of transition.

4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The major 9 points on the curve of γ characteristics on the LCD panel are arbitrarily assigned to external power supplies V_8 to V_0. The upper 3 bits of the display data select external power supplies V_{n+1} to V_n; and the lower 3 bits split V_{n+1} to V_n into eight uniform partitions by means of D/A conversion to output the 64 gray scale voltage.

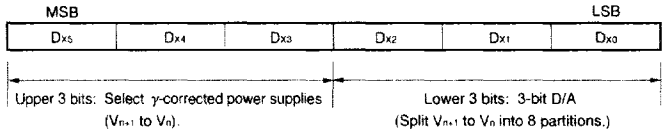
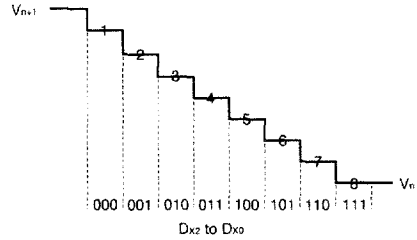


Table 1

D_{X5}	D_{X4}	D_{X3}	V_{n+1} to V_n
0	0	0	V_8 to V_7
0	0	1	V_7 to V_6
0	1	0	V_6 to V_5
0	1	1	V_5 to V_4
1	0	0	V_4 to V_3
1	0	1	V_3 to V_2
1	1	0	V_2 to V_1
1	1	1	V_1 to V_0

Figure 1



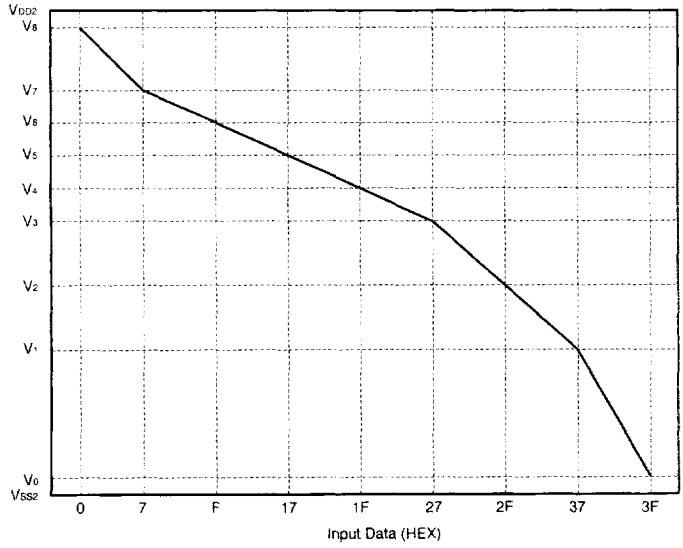
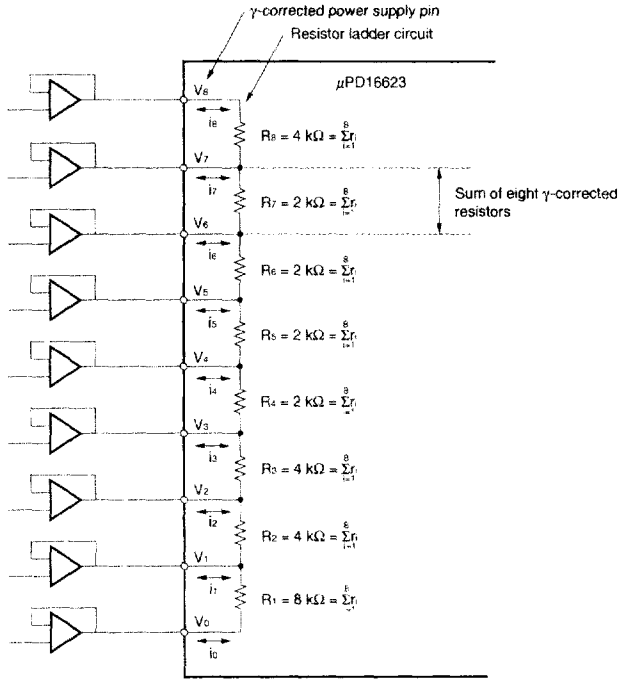


Table 2 Relationship Between Input Data and Output Voltage

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
00H	0	0	0	0	0	0	$V_7 + (V_8 - V_7) \times 7/8$
01H	0	0	0	0	0	1	$V_7 + (V_8 - V_7) \times 6/8$
02H	0	0	0	0	1	0	$V_7 + (V_8 - V_7) \times 5/8$
03H	0	0	0	0	1	1	$V_7 + (V_8 - V_7) \times 4/8$
04H	0	0	0	1	0	0	$V_7 + (V_8 - V_7) \times 3/8$
05H	0	0	0	1	0	1	$V_7 + (V_8 - V_7) \times 2/8$
06H	0	0	0	1	1	0	$V_7 + (V_8 - V_7) \times 1/8$
07H	0	0	0	1	1	1	V_7
08H	0	0	1	0	0	0	$V_6 + (V_7 - V_6) \times 7/8$
09H	0	0	1	0	0	1	$V_6 + (V_7 - V_6) \times 6/8$
0AH	0	0	1	0	1	0	$V_6 + (V_7 - V_6) \times 5/8$
0BH	0	0	1	0	1	1	$V_6 + (V_7 - V_6) \times 4/8$
0CH	0	0	1	1	0	0	$V_6 + (V_7 - V_6) \times 3/8$
0DH	0	0	1	1	0	1	$V_6 + (V_7 - V_6) \times 2/8$
0EH	0	0	1	1	1	0	$V_6 + (V_7 - V_6) \times 1/8$
0FH	0	0	1	1	1	1	V_6
10H	0	1	0	0	0	0	$V_5 + (V_6 - V_5) \times 7/8$
11H	0	1	0	0	0	1	$V_5 + (V_6 - V_5) \times 6/8$
12H	0	1	0	0	1	0	$V_5 + (V_6 - V_5) \times 5/8$
13H	0	1	0	0	1	1	$V_5 + (V_6 - V_5) \times 4/8$
14H	0	1	0	1	0	0	$V_5 + (V_6 - V_5) \times 3/8$
15H	0	1	0	1	0	1	$V_5 + (V_6 - V_5) \times 2/8$
16H	0	1	0	1	1	0	$V_5 + (V_6 - V_5) \times 1/8$
17H	0	1	0	1	1	1	V_5
18H	0	1	1	0	0	0	$V_4 + (V_5 - V_4) \times 7/8$
19H	0	1	1	0	0	1	$V_4 + (V_5 - V_4) \times 6/8$
1AH	0	1	1	0	1	0	$V_4 + (V_5 - V_4) \times 5/8$
1BH	0	1	1	0	1	1	$V_4 + (V_5 - V_4) \times 4/8$
1CH	0	1	1	1	0	0	$V_4 + (V_5 - V_4) \times 3/8$
1DH	0	1	1	1	0	1	$V_4 + (V_5 - V_4) \times 2/8$
1EH	0	1	1	1	1	0	$V_4 + (V_5 - V_4) \times 1/8$
1FH	0	1	1	1	1	1	V_4
20H	1	0	0	0	0	0	$V_3 + (V_4 - V_3) \times 7/8$
21H	1	0	0	0	0	1	$V_3 + (V_4 - V_3) \times 6/8$
22H	1	0	0	0	1	0	$V_3 + (V_4 - V_3) \times 5/8$
23H	1	0	0	0	1	1	$V_3 + (V_4 - V_3) \times 4/8$
24H	1	0	0	1	0	0	$V_3 + (V_4 - V_3) \times 3/8$
25H	1	0	0	1	0	1	$V_3 + (V_4 - V_3) \times 2/8$
26H	1	0	0	1	1	0	$V_3 + (V_4 - V_3) \times 1/8$
27H	1	0	0	1	1	1	V_3
28H	1	0	1	0	0	0	$V_2 + (V_3 - V_2) \times 7/8$
29H	1	0	1	0	0	1	$V_2 + (V_3 - V_2) \times 6/8$
2AH	1	0	1	0	1	0	$V_2 + (V_3 - V_2) \times 5/8$
2BH	1	0	1	0	1	1	$V_2 + (V_3 - V_2) \times 4/8$
2CH	1	0	1	1	0	0	$V_2 + (V_3 - V_2) \times 3/8$
2DH	1	0	1	1	0	1	$V_2 + (V_3 - V_2) \times 2/8$
2EH	1	0	1	1	1	0	$V_2 + (V_3 - V_2) \times 1/8$
2FH	1	0	1	1	1	1	V_2
30H	1	1	0	0	0	0	$V_1 + (V_2 - V_1) \times 7/8$
31H	1	1	0	0	0	1	$V_1 + (V_2 - V_1) \times 6/8$
32H	1	1	0	0	1	0	$V_1 + (V_2 - V_1) \times 5/8$
33H	1	1	0	0	1	1	$V_1 + (V_2 - V_1) \times 4/8$
34H	1	1	0	1	0	0	$V_1 + (V_2 - V_1) \times 3/8$
35H	1	1	0	1	0	1	$V_1 + (V_2 - V_1) \times 2/8$
36H	1	1	0	1	1	0	$V_1 + (V_2 - V_1) \times 1/8$
37H	1	1	0	1	1	1	V_1
38H	1	1	1	0	0	0	$V_0 + (V_1 - V_0) \times 7/8$
39H	1	1	1	0	0	1	$V_0 + (V_1 - V_0) \times 6/8$
3AH	1	1	1	0	1	0	$V_0 + (V_1 - V_0) \times 5/8$
3BH	1	1	1	0	1	1	$V_0 + (V_1 - V_0) \times 4/8$
3CH	1	1	1	1	0	0	$V_0 + (V_1 - V_0) \times 3/8$
3DH	1	1	1	1	0	1	$V_0 + (V_1 - V_0) \times 2/8$
3EH	1	1	1	1	1	0	$V_0 + (V_1 - V_0) \times 1/8$
3FH	1	1	1	1	1	1	V_0

Regarding γ-Corrected Power Circuits

The reference power supply of the D/A converter is composed of 64 resistor ladder circuits in total; and the resistance value Σr viewed from between γ-corrected power supply terminals varies depending on between which γ-corrected power supply terminals it is viewed from. Between two γ-corrected power supply terminals, there are eight identical serial resistors. The resistance value Σr in the diagram below is represented by the sum of eight values. The resistance ratio (Σr ratio) between γ-corrected power supply terminals is designed with a value comparatively close to the ratio of γ-corrected voltages V_8 to V_0 (gray scale voltages of the 8-step portion) used on the actual LCD panel. Therefore, under an ideal condition where there is no difference between these two ratios, the potential difference between the voltage of the γ-corrected power supply and the gray scale voltage of the 8-step portion in the μPD16623's resistor ladder circuits disappears. Also, because no more currents flow into the γ-corrected power supply terminals V_1 to V_7, the voltage follower circuit is rendered unnecessary.



Relationship Between Input Data and Output

Data format: 1-pixel data (6 bits) × RGB (3 dots)

Input width: 18 bits

$R/\overline{L}$ = H (Right shift)

Output	S_1	S_2	S_3	···	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	···	D_{10} to D_{15}	D_{20} to D_{25}

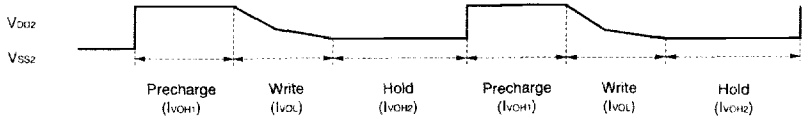
$R/\overline{L}$ = L (Left shift)

Output	S_1	S_2	S_3	···	S_{239}	S_{240}
Data	D_{03} to D_{05}	D_{13} to D_{15}	D_{23} to D_{25}	···	D_{13} to D_{15}	D_{23} to D_{25}

5. OUTPUT BUFFER OPERATION

During the blanking period, precharging is performed by the inhibit current I_{VOH1} until the V_{DD2} level is reached. Then, if writing by the LCD is completed up to a specified voltage by the sink current I_{VOL}, the machine is switched automatically to Power Save mode and the Write voltage is placed in hold by I_{VOH2}.

The timing and pulse width of the inhibit signal are determined by the load capacity of the LCD panel. Therefore, this is an item specified by the customer when designing the LCD panel. If the common electric potential is unstable during writing, it may lead to failures. (When in hold, the output impedance is as high as 1 MΩ. Thus, the load may be affected by the common inversion, causing the output to become abnormal. Be careful about this. Make sure to perform the common inversion during the low precharge period when the output impedance is low.



1 Horizontal period

Absolute Maximum Ratings (V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD1}, V_{DD2}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to $V_{DD1, 2}$+0.3	V
Output Voltage	V_O	−0.3 to $V_{DD1, 2}$+0.3	V
Permissible Dissipation	P_D	150	mW
Operating Temperature	T_A	−10 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Recommended Operating Range (T_A = −10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Power Voltage	V_{DD2}	4.5	5.0	5.5	V
γ-corrected Power	V_9 to V_8	V_{SS2}+0.1		V_{DD2}−0.1	V
Driver Part Output Voltage	V_O	V_{SS2}+0.1		V_{DD2}−0.1	V
Maximum Clock Frequency	f_{max}	33			MHz
Output Load Capacity	C_L			150	pF

Electrical Specifications (T_A = −10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 5.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH}	R/$\overline{L}$, TEST, CLK, $\overline{STB}$, $\overline{INH}$, STHR (STHL),	D_{00-05}, D_{10-15}, D_{20-25}	0.8V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}			0		0.2V_{DD1}	V
Input Leakage Current	I_{IL}	D_{00-05}, R/$\overline{L}$, D_{10-15}, D_{20-25}				±1.0	μA
Pull-up Resistor	R_{PU}	V_{DD1} = 3.3 V, TEST		100	250	750	kΩ
High-Level Output Voltage	V_{OH}	STHR (STHL), I_O = −1.0 mA		V_{DD1}−0.5			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_O = +1.0 mA				0.5	V
γ-Corrected Power Static Current Consumption	I_{V9}	V_{DD1} = 3.3 ±0.3 V, V_9 = 0.50 V, V_5 = 3.35 V, V_1 = 1.64 V, V_8 = 3.64 V, V_2 = 2.21 V, V_7 = 3.93 V, V_3 = 2.27 V, V_6 = 4.50 V, V_4 = 3.07 V, Note	V_8		+160	+300	μA
			V_7 to V_1		±10		μA
			V_0	−300	−160		μA
Driver Output Current	I_{VOH1}	$\overline{STB}$ = 0 V, V_{OUT} = 4.0 V, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V			−2.0	−0.6	mA
	I_{VOH2}	$\overline{STB}$ = $\overline{INH}$ = 3.3 V, V_{OUT} = 3.9 V, V_X = 4.9 V, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V			−5.0		μA
	I_{VOL}	$\overline{STB}$ = 3.3 V, V_{OUT} = 1.1 V, V_X = 0.1 V, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V		0.4	1.0		mA

(V_X refers to output voltages of analog output terminals S_1 to S_{240}.)
(V_{OUT} refers to voltages applied to analog output terminals S_1 to S_{240}.)
Note V_1 to V_7 are applied with the ideal voltages determined by internal resistors.

Electrical Specifications (T_A = −10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 5.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 5.0 V V_O = 1.0 V/2.5 V/4.0 V		±10	±30	mV
Output Voltage Range	V_O	Input data: 00H to 3FH	V_{SS2}+0.1		V_{DD2}−0.1	V
Dynamic Current Consumption	I_{DD1}	V_{DD1}, Note 1, Note 2, when unloaded		1.13	2.2	mA
Dynamic Current Consumption	I_{DD2}	V_{DD2}, Note 1, Note 2, when unloaded		4.04	6.0	mA

Notes 1. The $\overline{STB}$ cycle is specified with 30 μs and f_{CLK} = 25 MHz. Display data pattern: 010101 ··· (Checkered pattern)

2. Assuming a VGA's single-sided arrangement (8 items), this refers to the current consumption of one driver portion when cascaded.

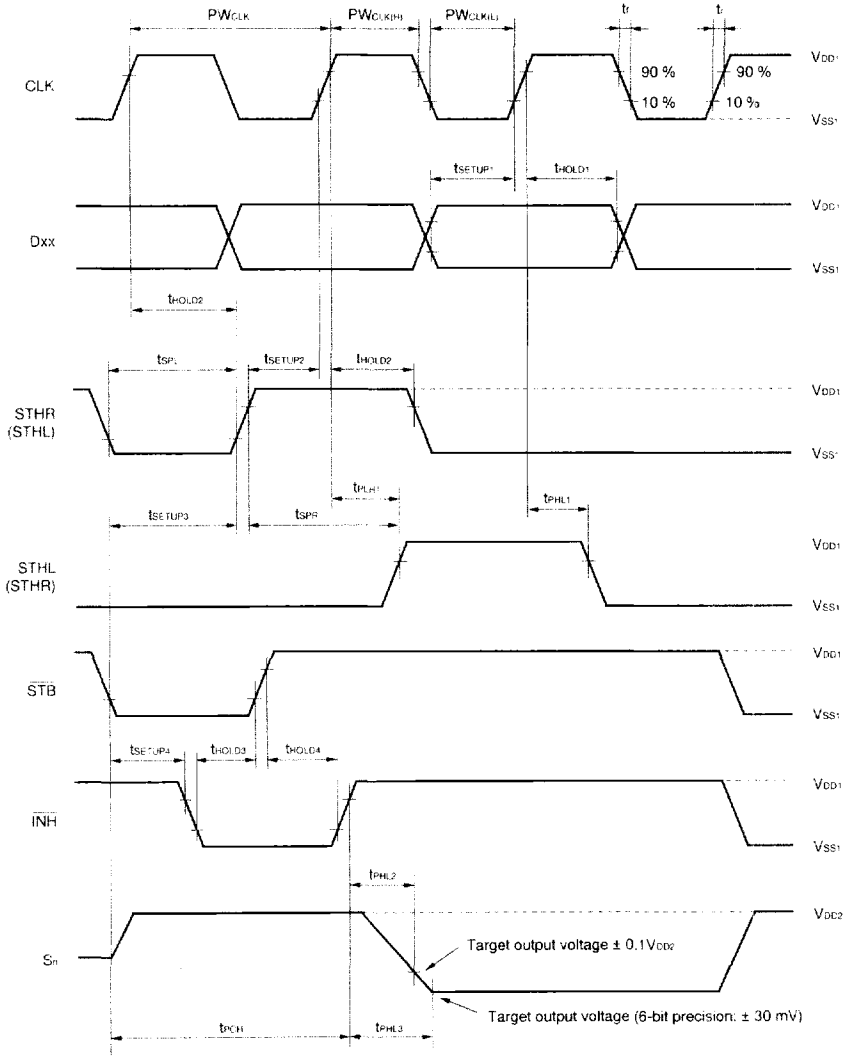
Switching Characteristics (T_A = −10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 5.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 3.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Low Period	$PW_{CLK(L)}$		4			ns
Clock High Period	$PW_{CLK(H)}$		4			ns
Data Setup Period	t_{SETUP1}		2			ns
Data Hold Period	t_{HOLD1}		2			ns
Start Pulse Setup Period	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
Start Pulse Low Period	t_{SPL}		2			CLK
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF	2		17	ns
Start Pulse Delay Time	t_{PHL1}	C_L = 15 pF	2		17	ns
Start Pulse Rise Time	t_{SPR}			80		CLK
Precharge Time	t_{PCH}		3			μs
$\overline{STB}$ Setup Time	t_{SETUP3}		1			CLK
$\overline{STB}$ Hold Time	t_{HOLD3}		1			μs
$\overline{INH}$ Setup Time	t_{SETUP4}		1			μs
$\overline{INH}$ Hold Time	t_{HOLD4}		0.5			μs
Driver Output Delay Time 1	t_{PHL2}	2 kΩ + 75 pF ×2 (π type)			3	μs
Driver Output Delay Time 2	t_{PHL3}	2 kΩ + 75 pF ×2 (π type)			10	μs
Data Invalid Period	t_{INV}			3		CLK
Final Data Timing	t_{LDT}				1	CLK
Inter-CLK-$\overline{STB}$ Time	$t_{CLK\text{-}\overline{STB}}$	CLK↑ → $\overline{STB}$ ↑ or ↓	7			ns
Inter-$\overline{STB}$-CLK Time	$t_{\overline{STB}\text{-}CLK}$	$\overline{STB}$ ↑ or ↓ → CLK ↑	7			ns
Input Capacitance 1	C_{I1}	V_0 to V_9, T_A = 25 °C		(100)		pF
Input Capacitance 2	C_{I2}	STHR (STHL), T_A = 25 °C		10	15	pF
Input Capacitance 3	C_{I3}	Other than V_0 to V_9 and STHR (STHL), T_A = 25 °C		7	10	pF

Switching Characteristics (R/$\overline{L}$ = H)

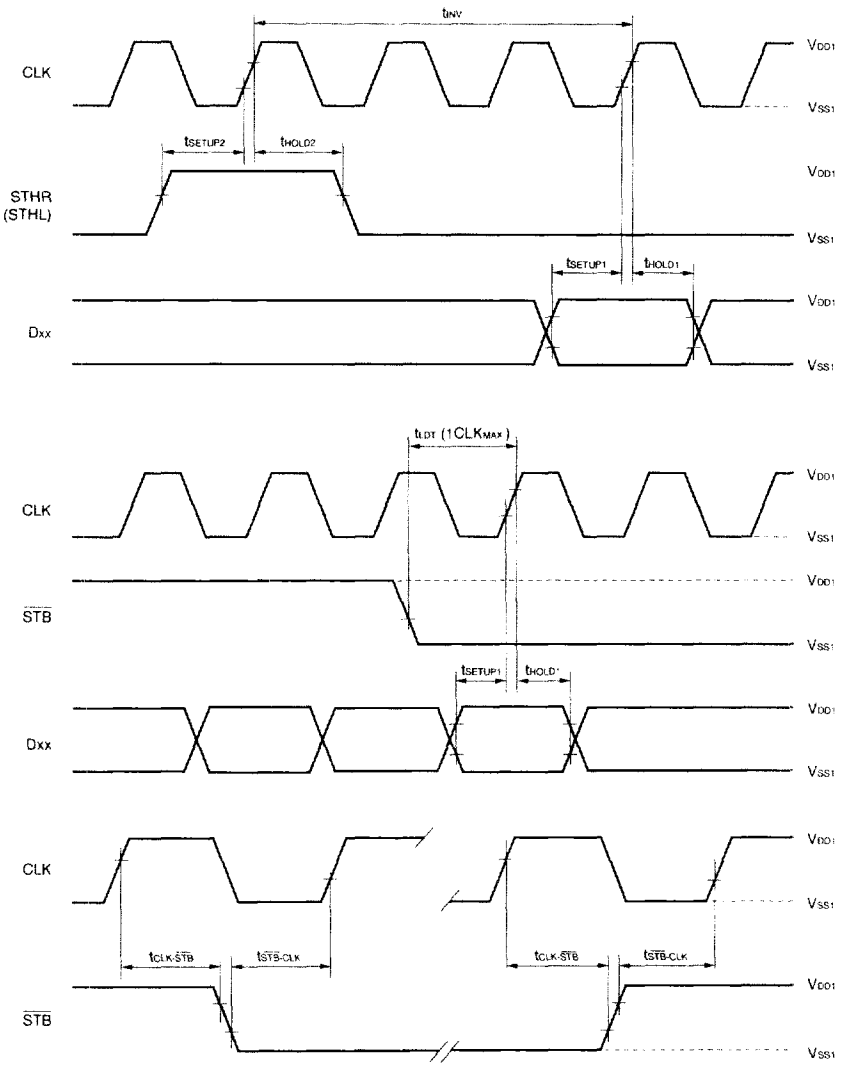
Unless otherwise specified, the input levels shall be V_{IH} = 0.8V_{DD1} and V_{IL} = 0.2V_{DD1}.

The value in brackets refers to R/$\overline{L}$ = L.

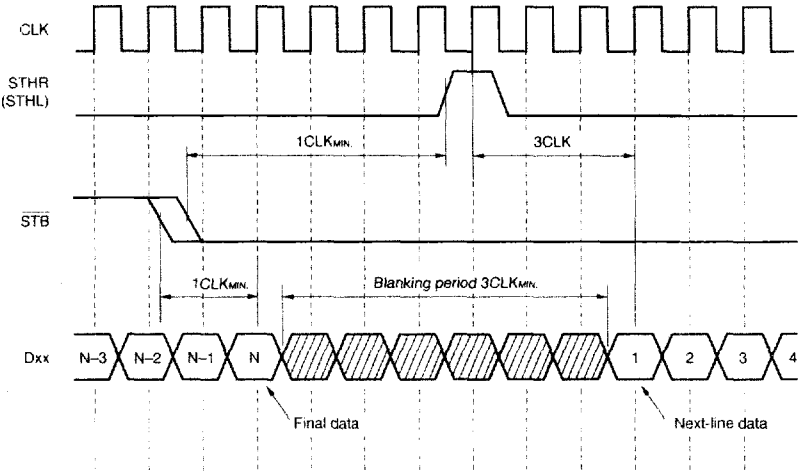


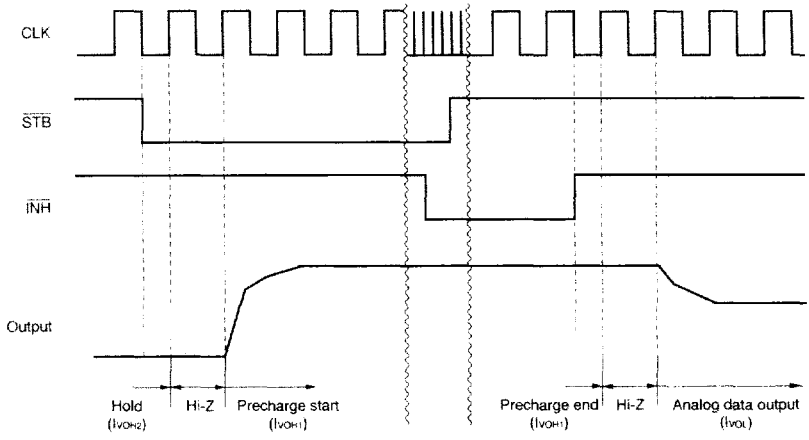
Caution When shifting the γ-corrected power during the precharge period, be sure to secure the precharge timing above after the gamma-corrected power is stabilized.

AC Timing


tINV
CLK
VDD1
VSS1
tSETUP2
tHOLD2
STHR
(STHL)
VDD1
VSS1
tSETUP1
tHOLD1
Dxx
VDD1
VSS1
tLDT (1CLKMAX)
CLK
VDD1
VSS1
STB
VDD1
VSS1
tSETUP1
tHOLD1
Dxx
VDD1
VSS1
CLK
VDD1
VSS1
tCLK-STB
tSTB-CLK
tCLK-STB
tSTB-CLK
STB
VDD1
VSS1

Relationship Between $\overline{STB}$ Start Pulse (STHR, STHL) and Blanking Period





RECOMMENDED SOLDERING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Soldering Condition	Soldering Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Sheet-shape bonding agent)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm²; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm²; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grades to NEC's Semiconductor Devices (IEI-1209)