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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD160903

384/402-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD160903 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 262,144 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a clock frequency of 45 MHz when driving at 2.7 V.

FEATURES

- CMOS level input
- 384/402 outputs
- Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 2.7 to 3.6 V
- Driver power supply voltage (V_{DD2}): 5.5 V ± 0.275 V
- High-speed data transfer: f_{CLK} = 45 MHz (internal data transfer speed when operating at V_{DD1} = 2.7 V)
- Output dynamic range: V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (POL21, POL22)
- Single-side mounting is possible (incorporation of slim TCP)

ORDERING INFORMATION

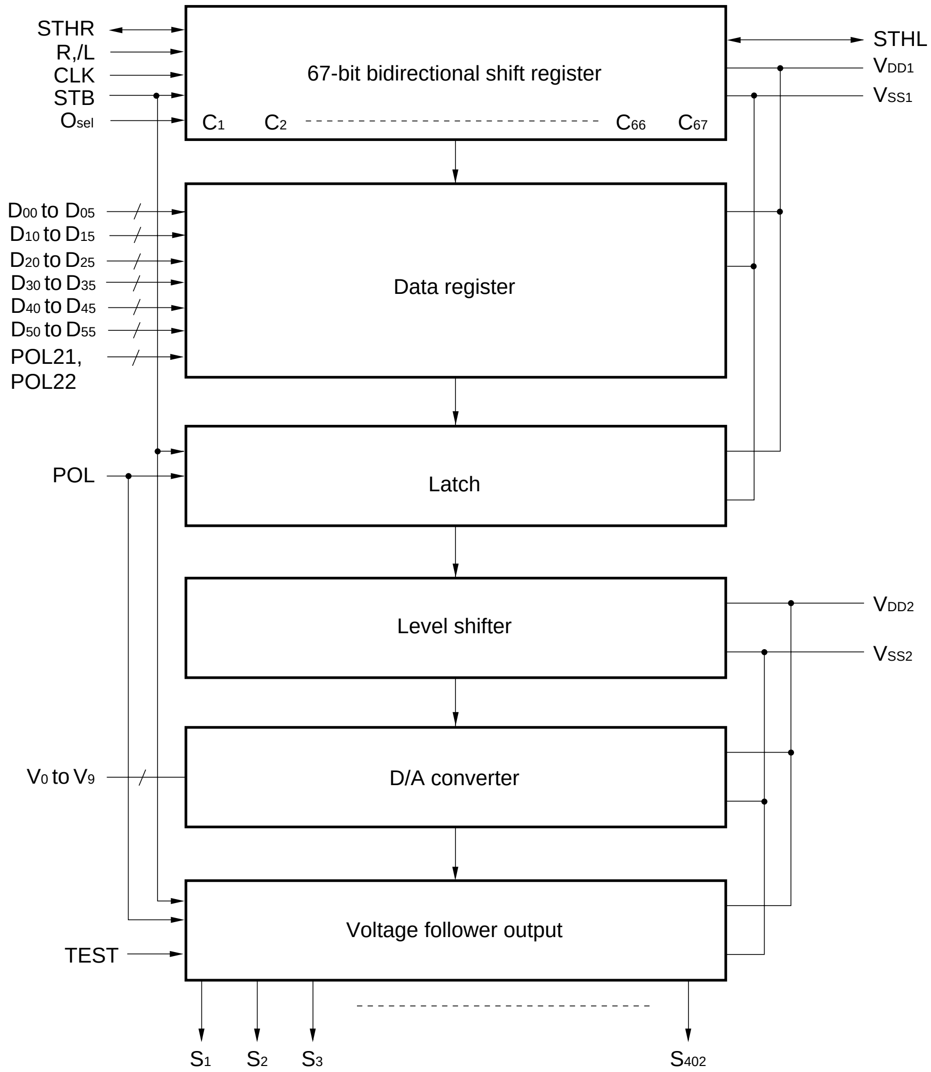
Part Number	Package
μPD160903N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

Document No. S14578EJ1V1DS00 (1st edition)
Date Published June 2001 NS CP (K)
Printed in Japan

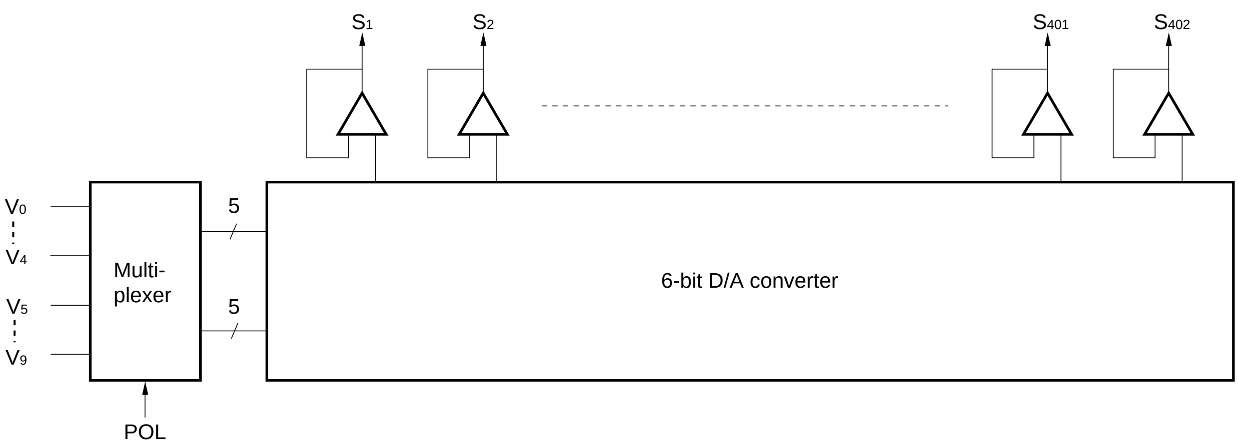
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

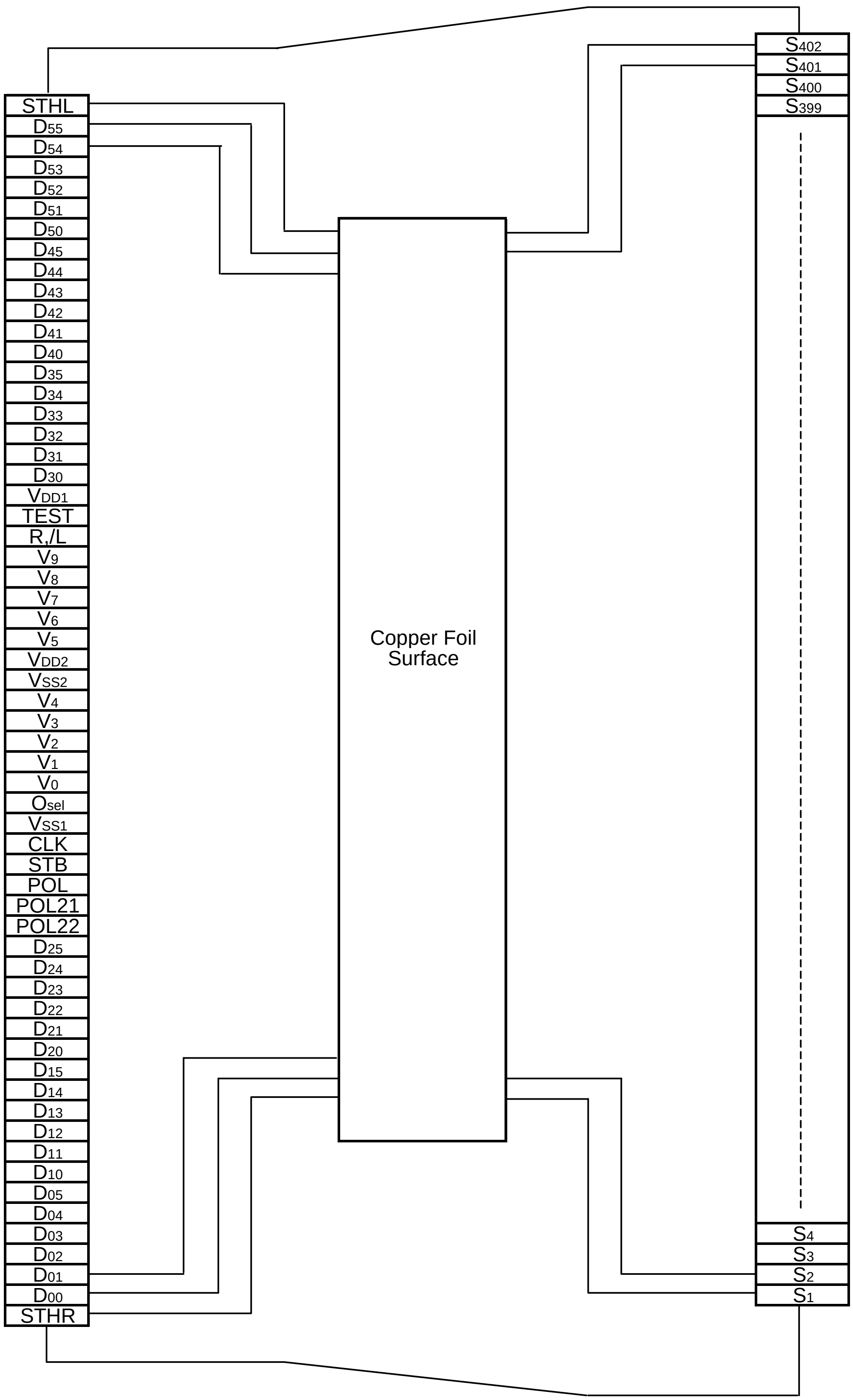


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD160903N-xxx) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{402}	Driver output	O	The D/A converted 64-gray-scale analog voltage is output.
O_{sel}	Selection number of outputs switching	I	O_{sel}:= H or open: 384 outputs (Output pinsS_{193} through S_{210} are invalid) O_{sel}: = L: 402 outputs Pulled up internally in the LSI.
D_{00} to D_{05}	Display data	I	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}			
D_{20} to D_{25}			
D_{30} to D_{35}			
D_{40} to D_{45}			
D_{50} to D_{55}			
R,/L	Shift direction control	I	Refers to the shift direction control. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR (input), $S_1 \rightarrow S_{402}$, STHL (output) R,/L = L (left shift) : STHL (input), $S_{402} \rightarrow S_1$, STHR (output)
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is valid.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	I	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 67th clock (64th clock in 384 outputs mode) after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 69th clock (66th clock in 384 mode) pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver after 4CLK . It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	I	POL = L: The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
★ POL21, POL22	Data inversion	I	Data inversion can invert when display data is loaded. POL21: Invert/not invert of display data D_{00} to D_{05}, D_{10} to D_{15}, D_{20} to D_{25}. POL22: Invert/not invert of display data D_{30} to D_{35}, D_{40} to D_{45}, D_{50} to D_{55}. POL21, POL22 = H : Display data is inverted. POL21, POL22 = L : Display data is not inverted.
TEST	Test	I	Normally, TEST = H or open. This pin is pulled up to the V_{DD1} power supply inside the IC
V_0 to V_9	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > 0.5\ V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$

(2/2)

Pin Symbol	Pin Name	I/O	Description
V_{DD1}	Logic power supply	–	2.7 to 3.6 V
V_{DD2}	Driver power supply	–	5.5 V ± 0.275 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut.

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD160903 incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships as follows:

$V_{DD2} - 0.1\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > 0.5\ V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\text{ V}$

Figures 5–2 and 5–3 indicates the relationship between the input data and output voltage and the resistance values of the resistor strings.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

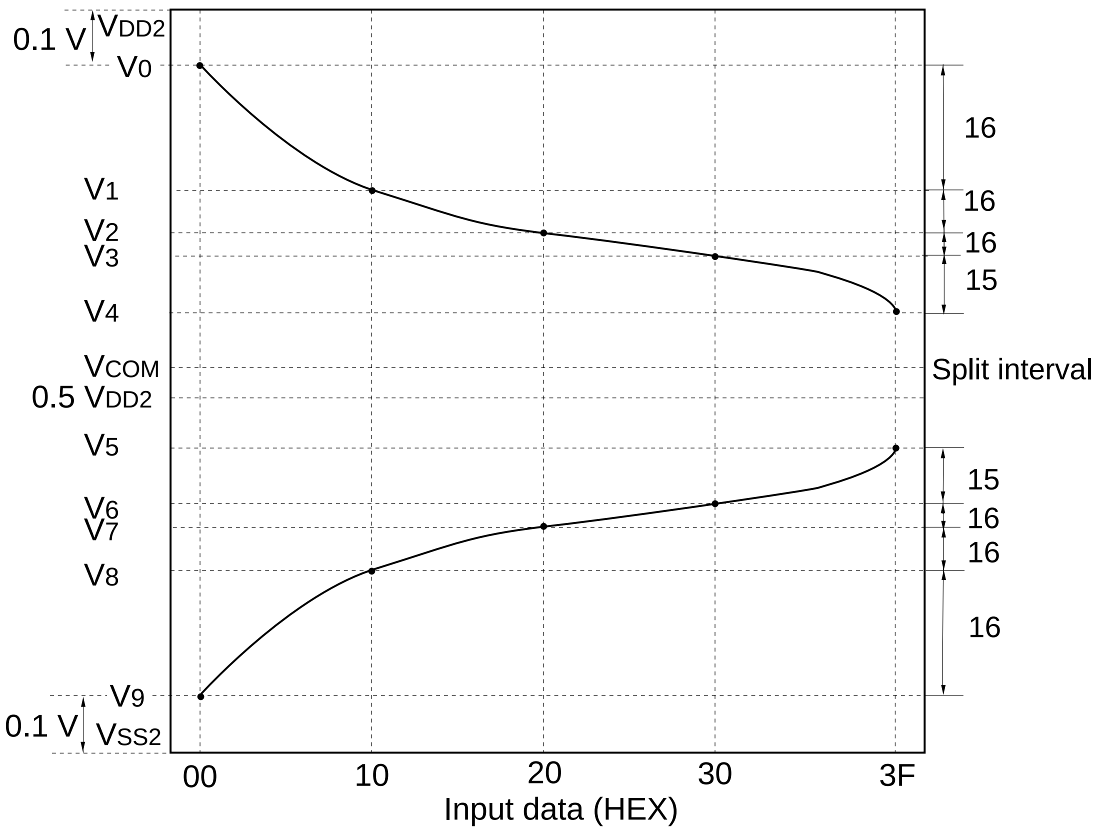
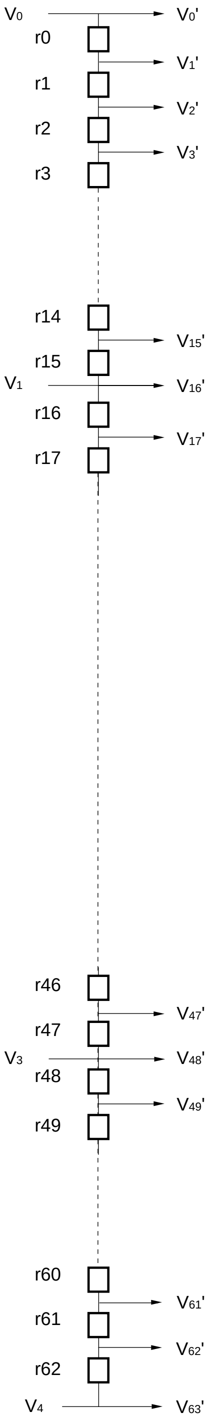


Figure 5–2. Relationship between Input Data and Output Voltage

V_{DD2} – 0.1 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 V_{DD2}, POL21, POL22 = L



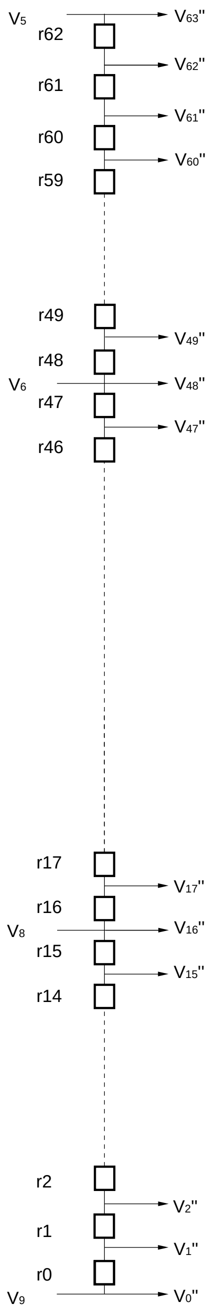
Data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0'	V0
01H	0	0	0	0	0	1	V1'	V1+(V0-V1)× 7250 / 8050
02H	0	0	0	0	1	0	V2'	V1+(V0-V1)× 6500 / 8050
03H	0	0	0	0	1	1	V3'	V1+(V0-V1)× 5800 / 8050
04H	0	0	0	1	0	0	V4'	V1+(V0-V1)× 5150 / 8050
05H	0	0	0	1	0	1	V5'	V1+(V0-V1)× 4550 / 8050
06H	0	0	0	1	1	0	V6'	V1+(V0-V1)× 4000 / 8050
07H	0	0	0	1	1	1	V7'	V1+(V0-V1)× 3450 / 8050
08H	0	0	1	0	0	0	V8'	V1+(V0-V1)× 2950 / 8050
09H	0	0	1	0	0	1	V9'	V1+(V0-V1)× 2450 / 8050
0AH	0	0	1	0	1	0	V10'	V1+(V0-V1)× 2050 / 8050
0BH	0	0	1	0	1	1	V11'	V1+(V0-V1)× 1650 / 8050
0CH	0	0	1	1	0	0	V12'	V1+(V0-V1)× 1300 / 8050
0DH	0	0	1	1	0	1	V13'	V1+(V0-V1)× 950 / 8050
0EH	0	0	1	1	1	0	V14'	V1+(V0-V1)× 600 / 8050
0FH	0	0	1	1	1	1	V15'	V1+(V0-V1)× 300 / 8050
10H	0	1	0	0	0	0	V16'	V1
11H	0	1	0	0	0	1	V17	V2+(V1-V2)× 2450 / 2750
12H	0	1	0	0	1	0	V18'	V2+(V1-V2)× 2200 / 2750
13H	0	1	0	0	1	1	V19'	V2+(V1-V2)× 1950 / 2750
14H	0	1	0	1	0	0	V20'	V2+(V1-V2)× 1700 / 2750
15H	0	1	0	1	0	1	V21'	V2+(V1-V2)× 1500 / 2750
16H	0	1	0	1	1	0	V22'	V2+(V1-V2)× 1300 / 2750
17H	0	1	0	1	1	1	V23'	V2+(V1-V2)× 1100 / 2750
18H	0	1	1	0	0	0	V24'	V2+(V1-V2)× 950 / 2750
19H	0	1	1	0	0	1	V25'	V2+(V1-V2)× 800 / 2750
1AH	0	1	1	0	1	0	V26'	V2+(V1-V2)× 650 / 2750
1BH	0	1	1	0	1	1	V27'	V2+(V1-V2)× 500 / 2750
1CH	0	1	1	1	0	0	V28'	V2+(V1-V2)× 400 / 2750
1DH	0	1	1	1	0	1	V29'	V2+(V1-V2)× 300 / 2750
1EH	0	1	1	1	1	0	V30'	V2+(V1-V2)× 200 / 2750
1FH	0	1	1	1	1	1	V31'	V2+(V1-V2)× 100 / 2750
20H	1	0	0	0	0	0	V32'	V2
21H	1	0	0	0	0	1	V33'	V3+(V2-V3)× 1500 / 1600
22H	1	0	0	0	1	0	V34'	V3+(V2-V3)× 1400 / 1600
23H	1	0	0	0	1	1	V35'	V3+(V2-V3)× 1300 / 1600
24H	1	0	0	1	0	0	V36'	V3+(V2-V3)× 1200 / 1600
25H	1	0	0	1	0	1	V37'	V3+(V2-V3)× 1100 / 1600
26H	1	0	0	1	1	0	V38'	V3+(V2-V3)× 1000 / 1600
27H	1	0	0	1	1	1	V39'	V3+(V2-V3)× 900 / 1600
28H	1	0	1	0	0	0	V40'	V3+(V2-V3)× 800 / 1600
29H	1	0	1	0	0	1	V41'	V3+(V2-V3)× 700 / 1600
2AH	1	0	1	0	1	0	V42'	V3+(V2-V3)× 600 / 1600
2BH	1	0	1	0	1	1	V43'	V3+(V2-V3)× 500 / 1600
2CH	1	0	1	1	0	0	V44'	V3+(V2-V3)× 400 / 1600
2DH	1	0	1	1	0	1	V45'	V3+(V2-V3)× 300 / 1600
2EH	1	0	1	1	1	0	V46'	V3+(V2-V3)× 200 / 1600
2FH	1	0	1	1	1	1	V47'	V3+(V2-V3)× 100 / 1600
30H	1	1	0	0	0	0	V48'	V3
31H	1	1	0	0	0	1	V49'	V4+(V3-V4)× 3350 / 3450
32H	1	1	0	0	1	0	V50'	V4+(V3-V4)× 3250 / 3450
33H	1	1	0	0	1	1	V51'	V4+(V3-V4)× 3150 / 3450
34H	1	1	0	1	0	0	V52'	V4+(V3-V4)× 3050 / 3450
35H	1	1	0	1	0	1	V53'	V4+(V3-V4)× 2950 / 3450
36H	1	1	0	1	1	0	V54'	V4+(V3-V4)× 2800 / 3450
37H	1	1	0	1	1	1	V55'	V4+(V3-V4)× 2650 / 3450
38H	1	1	1	0	0	0	V56'	V4+(V3-V4)× 2500 / 3450
39H	1	1	1	0	0	1	V57'	V4+(V3-V4)× 2300 / 3450
3AH	1	1	1	0	1	0	V58'	V4+(V3-V4)× 2100 / 3450
3BH	1	1	1	0	1	1	V59'	V4+(V3-V4)× 1850 / 3450
3CH	1	1	1	1	0	0	V60'	V4+(V3-V4)× 1600 / 3450
3DH	1	1	1	1	0	1	V61'	V4+(V3-V4)× 1300 / 3450
3EH	1	1	1	1	1	0	V62'	V4+(V3-V4)× 800 / 3450
3FH	1	1	1	1	1	1	V63'	V4

rn	Resitance ratio
r0	800
r1	750
r2	700
r3	650
r4	600
r5	550
r6	550
r7	500
r8	500
r9	400
r10	400
r11	350
r12	350
r13	350
r14	300
r15	300
r16	300
r17	250
r18	250
r19	250
r20	200
r21	200
r22	200
r23	150
r24	150
r25	150
r26	150
r27	100
r28	100
r29	100
r30	100
r31	100
r32	100
r33	100
r34	100
r35	100
r36	100
r37	100
r38	100
r39	100
r40	100
r41	100
r42	100
r43	100
r44	100
r45	100
r46	100
r47	100
r48	100
r49	100
r50	100
r51	100
r52	100
r53	150
r54	150
r55	150
r56	200
r57	200
r58	250
r59	250
r60	300
r61	500
r62	800

Caution There is no connection between V_4 and V_5 terminal in the chip.

Figure 5–3. Relationship between Input Data and Output Voltage

0.5 $V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2}$ + 0.1 V, POL21, POL22 = L



Data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0"	V9
01H	0	0	0	0	0	1	V1"	V9+(V8-V9)× 800 / 8050
02H	0	0	0	0	1	0	V2"	V9+(V8-V9)× 1550 / 8050
03H	0	0	0	0	1	1	V3"	V9+(V8-V9)× 2250 / 8050
04H	0	0	0	1	0	0	V4"	V9+(V8-V9)× 2900 / 8050
05H	0	0	0	1	0	1	V5"	V9+(V8-V9)× 3500 / 8050
06H	0	0	0	1	1	0	V6"	V9+(V8-V9)× 4050 / 8050
07H	0	0	0	1	1	1	V7"	V9+(V8-V9)× 4600 / 8050
08H	0	0	1	0	0	0	V8"	V9+(V8-V9)× 5100 / 8050
09H	0	0	1	0	0	1	V9"	V9+(V8-V9)× 5600 / 8050
0AH	0	0	1	0	1	0	V10"	V9+(V8-V9)× 6000 / 8050
0BH	0	0	1	0	1	1	V11"	V9+(V8-V9)× 6400 / 8050
0CH	0	0	1	1	0	0	V12"	V9+(V8-V9)× 6750 / 8050
0DH	0	0	1	1	0	1	V13"	V9+(V8-V9)× 7100 / 8050
0EH	0	0	1	1	1	0	V14"	V9+(V8-V9)× 7450 / 8050
0FH	0	0	1	1	1	1	V15"	V9+(V8-V9)× 7750 8050
10H	0	1	0	0	0	0	V16"	V8
11H	0	1	0	0	0	1	V17"	V8+(V7-V8)× 300 / 2750
12H	0	1	0	0	1	0	V18"	V8+(V7-V8)× 550 / 2750
13H	0	1	0	0	1	1	V19"	V8+(V7-V8)× 800 / 2750
14H	0	1	0	1	0	0	V20"	V8+(V7-V8)× 1050 / 2750
15H	0	1	0	1	0	1	V21"	V8+(V7-V8)× 1250 / 2750
16H	0	1	0	1	1	0	V22"	V8+(V7-V8)× 1450 / 2750
17H	0	1	0	1	1	1	V23"	V8+(V7-V8)× 1650 / 2750
18H	0	1	1	0	0	0	V24"	V8+(V7-V8)× 1800 / 2750
19H	0	1	1	0	0	1	V25"	V8+(V7-V8)× 1950 / 2750
1AH	0	1	1	0	1	0	V26"	V8+(V7-V8)× 2100 / 2750
1BH	0	1	1	0	1	1	V27"	V8+(V7-V8)× 2250 / 2750
1CH	0	1	1	1	0	0	V28"	V8+(V7-V8)× 2350 / 2750
1DH	0	1	1	1	0	1	V29"	V8+(V7-V8)× 2450 / 2750
1EH	0	1	1	1	1	0	V30"	V8+(V7-V8)× 2550 / 2750
1FH	0	1	1	1	1	1	V31"	V8+(V7-V8)× 2650 2750
20H	1	0	0	0	0	0	V32"	V7
21H	1	0	0	0	0	1	V33"	V7+(V6-V7)× 100 / 1600
22H	1	0	0	0	1	0	V34"	V7+(V6-V7)× 200 / 1600
23H	1	0	0	0	1	1	V35"	V7+(V6-V7)× 300 / 1600
24H	1	0	0	1	0	0	V36"	V7+(V6-V7)× 400 / 1600
25H	1	0	0	1	0	1	V37"	V7+(V6-V7)× 500 / 1600
26H	1	0	0	1	1	0	V38"	V7+(V6-V7)× 600 / 1600
27H	1	0	0	1	1	1	V39"	V7+(V6-V7)× 700 / 1600
28H	1	0	1	0	0	0	V40"	V7+(V6-V7)× 800 / 1600
29H	1	0	1	0	0	1	V41"	V7+(V6-V7)× 900 / 1600
2AH	1	0	1	0	1	0	V42"	V7+(V6-V7)× 1000 / 1600
2BH	1	0	1	0	1	1	V43"	V7+(V6-V7)× 1100 / 1600
2CH	1	0	1	1	0	0	V44"	V7+(V6-V7)× 1200 / 1600
2DH	1	0	1	1	0	1	V45"	V7+(V6-V7)× 1300 / 1600
2EH	1	0	1	1	1	0	V46"	V7+(V6-V7)× 1400 / 1600
2FH	1	0	1	1	1	1	V47"	V7+(V6-V7)× 1500 / 1600
30H	1	1	0	0	0	0	V48"	V6
31H	1	1	0	0	0	1	V49"	V6+(V5-V6)× 100 / 3450
32H	1	1	0	0	1	0	V50"	V6+(V5-V6)× 200 / 3450
33H	1	1	0	0	1	1	V51"	V6+(V5-V6)× 300 / 3450
34H	1	1	0	1	0	0	V52"	V6+(V5-V6)× 400 / 3450
35H	1	1	0	1	0	1	V53"	V6+(V5-V6)× 500 / 3450
36H	1	1	0	1	1	0	V54"	V6+(V5-V6)× 650 / 3450
37H	1	1	0	1	1	1	V55"	V6+(V5-V6)× 800 / 3450
38H	1	1	1	0	0	0	V56"	V6+(V5-V6)× 950 / 3450
39H	1	1	1	0	0	1	V57"	V6+(V5-V6)× 1150 / 3450
3AH	1	1	1	0	1	0	V58"	V6+(V5-V6)× 1350 / 3450
3BH	1	1	1	0	1	1	V59"	V6+(V5-V6)× 1600 / 3450
3CH	1	1	1	1	0	0	V60"	V6+(V5-V6)× 1850 / 3450
3DH	1	1	1	1	0	1	V61"	V6+(V5-V6)× 2150 / 3450
3EH	1	1	1	1	1	0	V62"	V6+(V5-V6)× 2650 / 3450
3FH	1	1	1	1	1	1	V63"	V5

rn	Resistance ratio
r0	800
r1	750
r2	700
r3	650
r4	600
r5	550
r6	550
r7	500
r8	500
r9	400
r10	400
r11	350
r12	350
r13	350
r14	300
r15	300
r16	300
r17	250
r18	250
r19	250
r20	200
r21	200
r22	200
r23	150
r24	150
r25	150
r26	150
r27	100
r28	100
r29	100
r30	100
r31	100
r32	100
r33	100
r34	100
r35	100
r36	100
r37	100
r38	100
r39	100
r40	100
r41	100
r42	100
r43	100
r44	100
r45	100
r46	100
r47	100
r48	100
r49	100
r50	100
r51	100
r52	100
r53	150
r54	150
r55	150
r56	200
r57	200
r58	250
r59	250
r60	300
r61	500
r62	800

Caution There is no connection between V_4 and V_5 terminal in the chip.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	...	S_{401}	S_{402}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (Left shift)

Output	S_1	S_2	S3	S4	...	S_{401}	S_{402}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

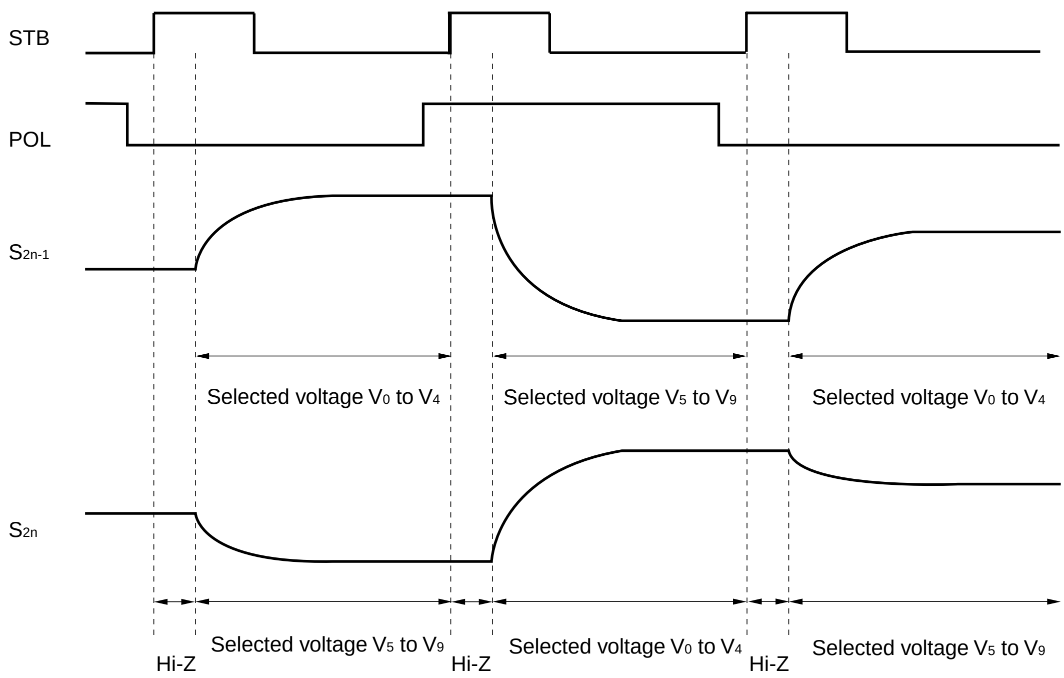
POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output), n = 1, 2, ... 201

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The gray-scale voltage is output 4 clocks after the start of D/A conversion in the LSI, in synchronization with the rising edge of STB.

During this 4-clock period, Hi-Z is output.



8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–20 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –20 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.7	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}		5.225	5.5	5.775	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		0.5 V_{DD2}		V_{DD2}–0.1	V
	V_5 to V_9		0.1		0.5 V_{DD2}	V
Driver Part Output Voltage	V_O		0.1		V_{DD2}–0.1	V
Clock Frequency	f_{CLK}				45	MHz

Electrical Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{DD2} = 5.5 V ± 0.275 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
γ-Corrected Resistance	R_γ	V_{DD2} = 5.5 V V_0 to V_4 = V_5 to V_9 = 2.0 V		6.0	12.0	18.0	kΩ
Driver Output Current	I_{VOH}	V_{DD2} = 5.5 V, V_X = 5.0 V, V_{OUT} = 4.5 V Note1			–150	–70	μA
	I_{VOL}	V_{DD2} = 5.5 V, V_X = 0.5 V, V_{OUT} = 1.0 V Note1		70	250		μA
Output Voltage Deviation	ΔV_O	T_A = 25°C, V_{SS2} + 1.0 V to V_{DD2} – 1.0 V			±5	±20	mV
Output Swing Difference Deviation	ΔV_{P-P1}	V_{DD1} = 3.3 V	V_{OUT} = 1.2 to 4.3 V		±3	±15	mV
	ΔV_{P-P2}	V_{DD2} = 5.5 V	V_{OUT} = 0.8 to 4.7 V		±7	±20	mV
	ΔV_{P-P3}	T_A = 25°C	V_{OUT} = 0.1 to 5.4 V		±15	±30	mV
Logic Part Dynamic Current Consumption Note2,3,4	I_{DD1}	V_{DD1}			1.0	6.0	mA
Driver Part Dynamic Current Consumption Note2,4	I_{DD2}	V_{DD2}, with no load			3.7	7.0	mA

Notes 1. V_X refers to the output voltage of analog output pins S_1 to S_{402}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{402}.

2. f_{STB} = 48 kHz, f_{CLK} = 32.5 MHz

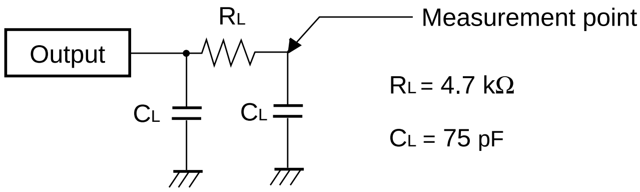
3. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{DD2} = 5.5 V ± 0.275 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF		9	18	ns
Driver Output Delay Time	t_{PLH2} Note	C_L = 150 pF, R_L = 4.7 kΩ		3.8	5.0	μs
	t_{PLH3} Note			5.4	8.5	μs
	t_{PHL2} Note			3.3	5.0	μs
	t_{PHL3} Note			4.4	8.5	μs
Input Capacitance	C_{I1}	Logic input other than STHR (STHL) is T_A = 25°C		5	10	pF
	C_{I2}	STHR (STHL),T_A = 25°C		8	15	pF

Note t_{PLH2} and t_{PHL2} are the time until the voltage reached its target voltage ±10% from the falling edge of STB.
t_{PLH2} and t_{PHL2} are the time until the voltage reached its target voltage ±20 mV from the falling edge of STB.



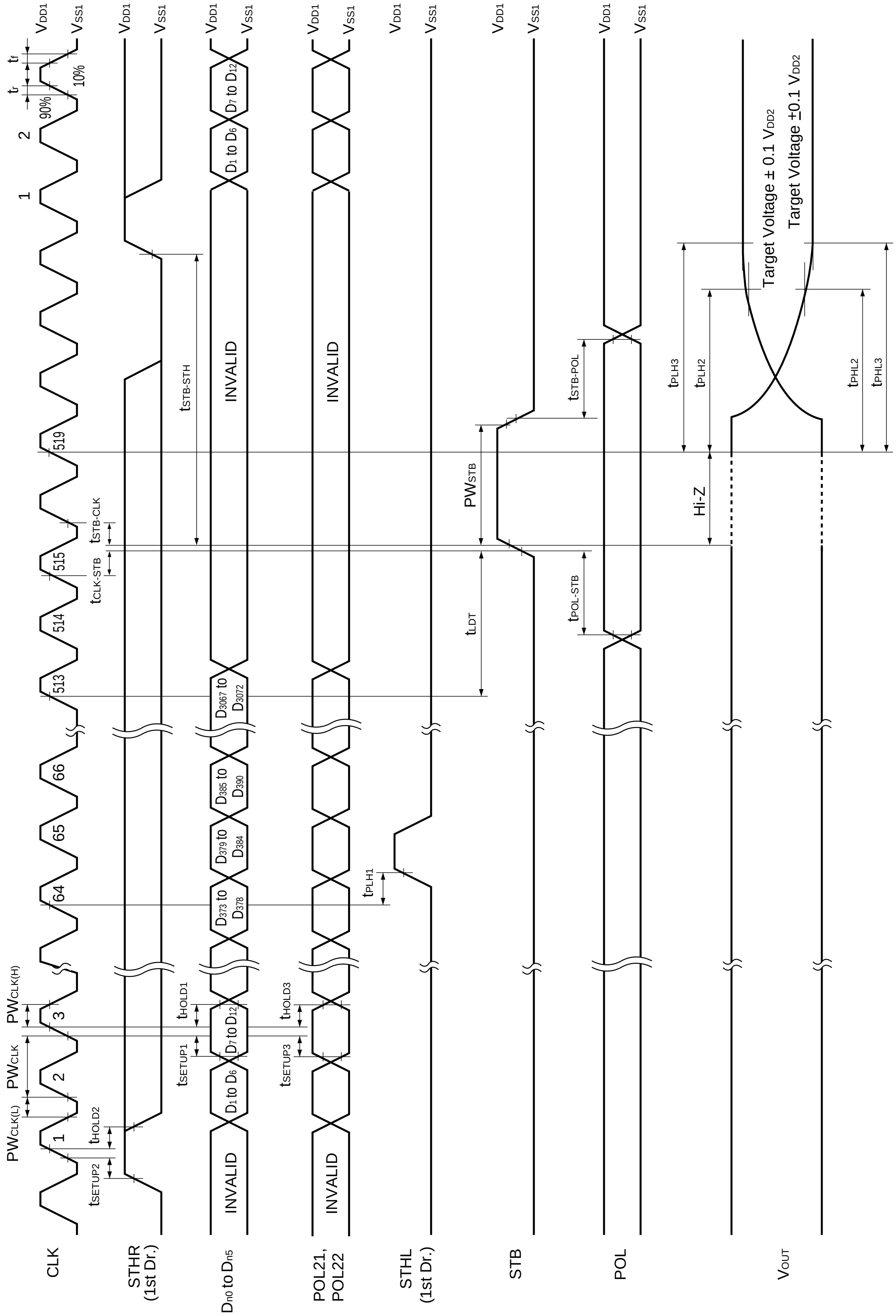
Timing Requirements (T_A = –20 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{SS1} = 0 V, t_r = t_f = 5.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		2			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
POL21/22 Setup Time	t_{SETUP3}		2			ns
POL21/22 Hold Time	t_{HOLD3}		3			ns
STB Pulse Width	PW_{STB}		4			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK\text{-}STB}$	CLK ↑ → STB ↑	4			ns
STB-CLK Time	$t_{STB\text{-}CLK}$	STB ↑ → CLK ↑	4			ns
Time Between STB and Start Pulse	$t_{STB\text{-}STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL\text{-}STB}$	POL ↑ or ↓ → STB ↑	6			ns
STB-POL Time	$t_{STB\text{-}POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

★ **Switching Characteristic Waveform(R,/L= H)**

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1} (the clock and display data numbers are examples when the resolution is XGA).



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD160903.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD160903N-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)