

512 Kbit / 1 Mbit / 2 Mbit (x8) Many-Time Programmable Flash

SST27SF512 / SST27SF010 / SST27SF020



Data Sheet

FEATURES:

- **Organized as 64K x8 / 128K x8 / 256K x8**
- **4.5-5.5V Read Operation**
- **Superior Reliability**
 - Endurance: At least 1000 Cycles
 - Greater than 100 years Data Retention
- **Low Power Consumption**
 - Active Current: 20 mA (typical)
 - Standby Current: 10 μ A (typical)
- **Fast Read Access Time**
 - 70 ns
 - 90 ns
- **Fast Byte-Program Operation**
 - Byte-Program Time: 20 μ s (typical)
 - Chip Program Time:
 - 1.4 seconds (typical) for SST27SF512
 - 2.8 seconds (typical) for SST27SF010
 - 5.6 seconds (typical) for SST27SF020
- **Electrical Erase Using Programmer**
 - Does not require UV source
 - Chip-Erase Time: 100 ms (typical)
- **TTL I/O Compatibility**
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **Packages Available**
 - 32-lead PLCC
 - 32-lead TSOP (8mm x 14mm)
 - 28-pin PDIP for SST27SF512
 - 32-pin PDIP for SST27SF010/020

PRODUCT DESCRIPTION

The SST27SF512/010/020 are a 64K x8 / 128K x8 / 256K x8 CMOS, Many-Time Programmable (MTP) low cost flash, manufactured with SST's proprietary, high performance SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. These MTP devices can be electrically erased and programmed at least 1000 times using an external programmer with a 12V power supply. They have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide memories.

Featuring high performance Byte-Program, the SST27SF512/010/020 provide a Byte-Program time of 20 μ s. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST27SF512/010/020 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST27SF512 are offered in 32-lead PLCC, 32-lead TSOP, and 28-pin PDIP packages. The SST27SF010/020 are offered in 32-pin PDIP, 32-lead PLCC, and 32-lead TSOP packages. See Figures 1, 2, and 3 for pin assignments.

Device Operation

The SST27SF512/010/020 are a low cost flash solution that can be used to replace existing UV-EPROM, OTP, and mask ROM sockets. These devices are functionally (read and program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, these devices also support electrical Erase operation via an external programmer. They do not require a UV source to erase, and therefore the packages do not have a window.

Read

The Read operation of the SST27SF512/010/020 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of T_{OE} from the falling edge of OE#, assuming that CE# pin has been low and the addresses have been stable for at least $T_{CE}-T_{OE}$. When the CE# pin is high, the chip is deselected and a typical standby current of 10 μ A is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.



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Byte-Program Operation

The SST27SF512/010/020 are programmed by using an external programmer. The programming mode for SST27SF010/020 is activated by asserting 11.4-12.6V on V_{PP} pin, $V_{DD} = 4.5-5.5V$, V_{IL} on CE# pin, and V_{IH} on OE# pin. The programming mode for SST27SF512 is activated by asserting 11.4-12.6V on OE#/ V_{PP} pin, $V_{DD} = 4.5-5.5V$, and V_{IL} on CE# pin. These devices are programmed byte-by-byte with the desired data at the desired address using a single pulse (CE# pin low for SST27SF512 and PGM# pin low for SST27SF010/020) of 20 μs . Using the MTP programming algorithm, the Byte-Programming process continues byte-by-byte until the entire chip has been programmed.

Chip-Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". Unlike traditional EPROMs, which use UV light to do the Chip-Erase, the SST27SF512/010/020 uses an electrical Chip-Erase operation. This saves a significant amount of time (about 30 minutes for each Erase operation). The entire chip can be erased in a single pulse of 100 ms (CE# pin low for SST27SF512 and PGM# pin for SST27SF010/020). In order to activate the Erase mode for SST27SF010/020, the 11.4-12.6V is applied to V_{PP} and A_9 pins, $V_{DD} = 4.5-5.5V$, V_{IL} on CE# pin, and V_{IH} on OE# pin. In order to activate Erase mode for SST27SF512, the 11.4-12.6V is applied to OE#/ V_{PP} and A_9 pins, $V_{DD} = 4.5-5.5V$, and V_{IL} on CE# pin. All other address and data pins are "don't care". The falling edge of CE# (PGM# for SST27SF010/020) will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FFH. Refer to Figures 11 and 12 for the flowcharts.

Product Identification Mode

The Product Identification mode identifies the devices as the SST27SF512, SST27SF010 and SST27SF020 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode for SST27SF010/020, the programming equipment must force V_H (11.4-12.6V) on address A_9 with V_{PP} pin at V_{DD} (4.5-5.5V) or V_{SS} . To activate this mode for SST27SF512, the programming equipment must force V_H (11.4-12.6V) on address A_9 with OE#/ V_{PP} pin at V_{IL} . Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 . For details, see Tables 3 and 4 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST27SF512	0001H	A4H
SST27SF010	0001H	A5H
SST27SF020	0001H	A6H

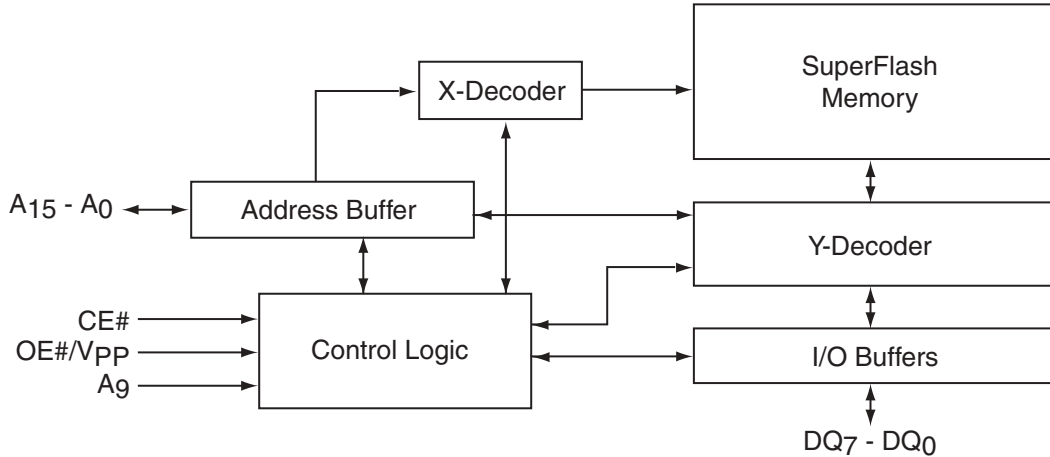
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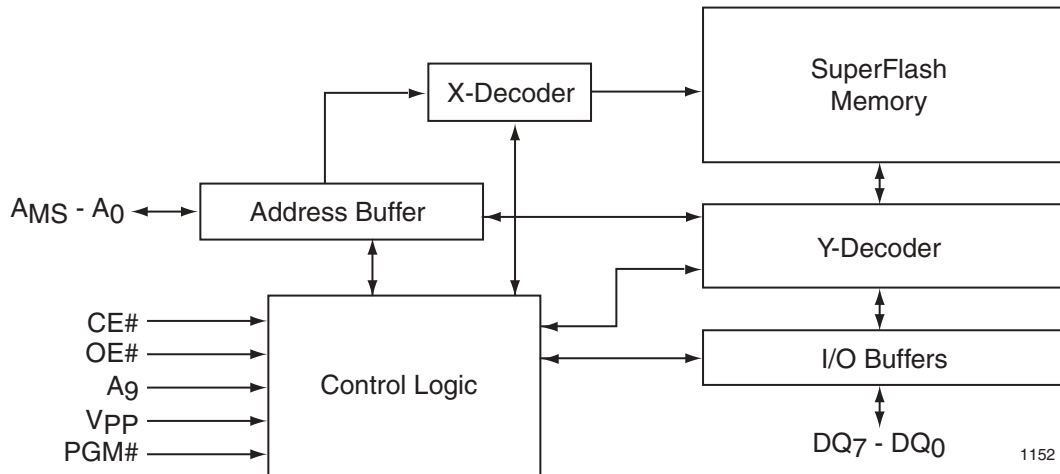
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FUNCTIONAL BLOCK DIAGRAM OF THE SST27SF512



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FUNCTIONAL BLOCK DIAGRAM OF THE SST27SF010/020



AMS = A₁₇ for SST27SF020, A₁₆ for SST27SF010

1152 B3.2



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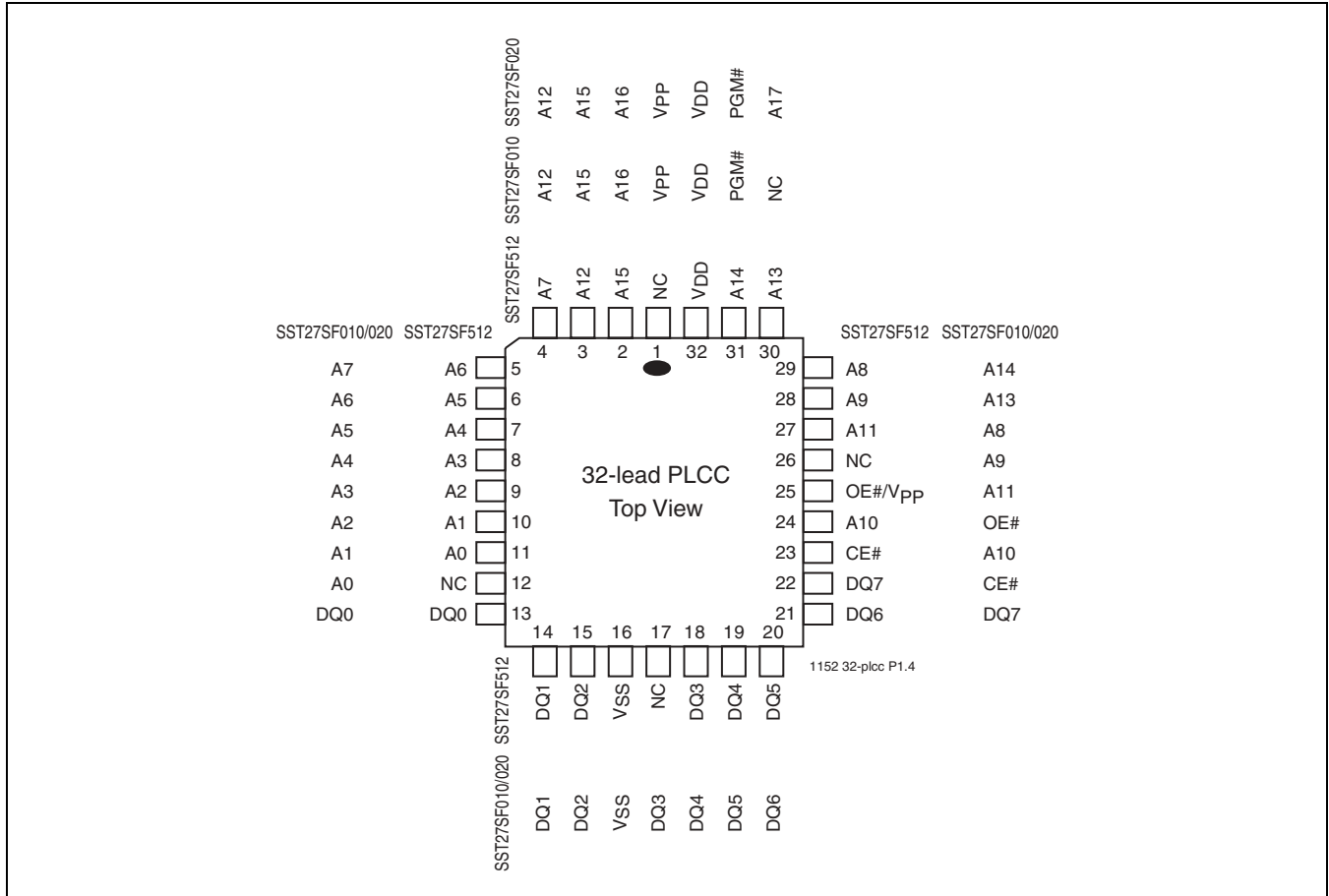


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

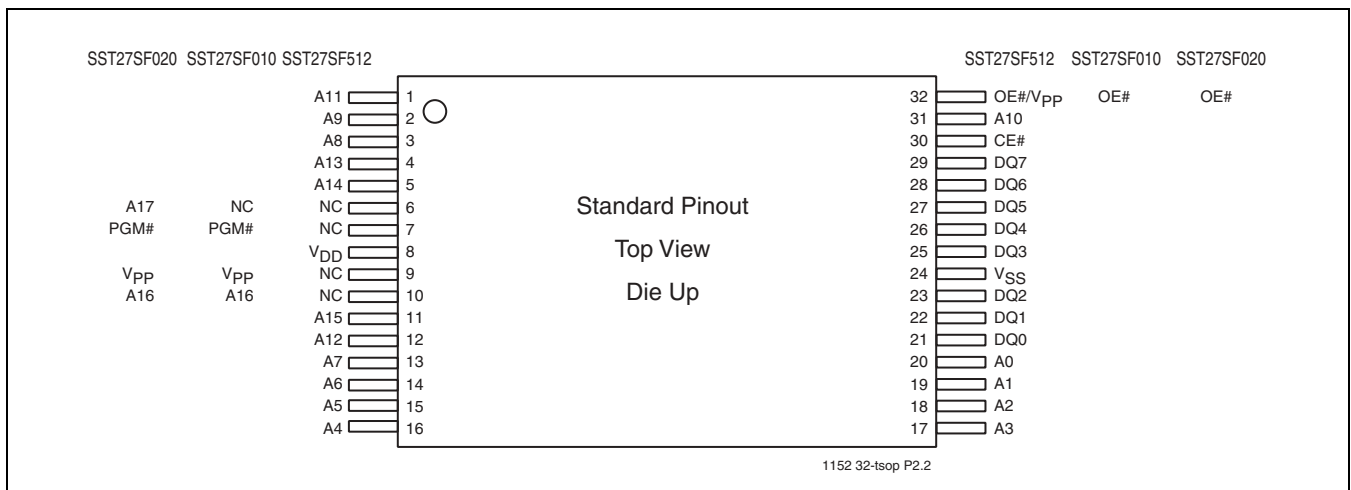


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)

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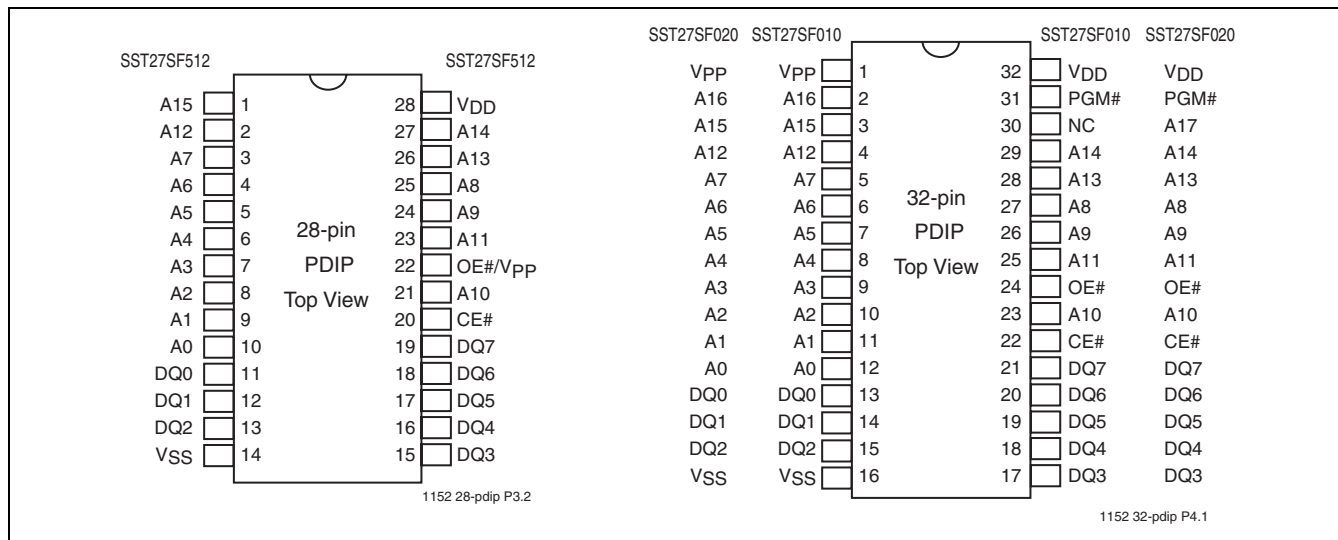


FIGURE 3: PIN ASSIGNMENTS FOR 28-PIN AND 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
$A_{MS}^1-A_0$	Address Inputs	To provide memory addresses
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Program cycles The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low
OE#	Output Enable	For SST27SF010/020, to gate the data output buffers during Read operation
OE#/V _{PP}	Output Enable/V _{PP}	For SST27SF512, to gate the data output buffers during Read operation and high voltage pin during Chip-Erase and programming operation
V _{PP}	Power Supply for Program or Erase	For SST27SF010/020, high voltage pin during Chip-Erase and programming operation 11.4-12.6V
V _{DD}	Power Supply	To provide 5.0V supply (4.5-5.5V)
V _{SS}	Ground	
NC	No Connection	Unconnected pins.

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1. A_{MS} = Most significant address
 A_{MS} = A_{15} for SST27SF512, A_{16} for SST27SF010, and A_{17} for SST27SF020



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TABLE 3: OPERATION MODES SELECTION FOR SST27SF512

Mode	CE#	OE#/V _{PP}	A ₉	DQ	Address
Read	V _{IL}	V _{IL}	A _{IN}	D _{OUT}	A _{IN}
Output Disable	V _{IL}	V _{IH}	X ¹	High Z	X
Program	V _{IL}	V _{PPH}	A _{IN}	D _{IN}	A _{IN}
Standby	V _{IH}	X	X	High Z	X
Chip-Erase	V _{IL}	V _{PPH}	V _H	High Z	X
Program/Erase Inhibit	V _{IH}	V _{PPH}	X	High Z	X
Product Identification	V _{IL}	V _{IL}	V _H	Manufacturer's ID (BFH) Device ID (A4H)	A ₁₅ -A ₁ =V _{IL} , A ₀ =V _{IL} A ₁₅ -A ₁ =V _{IL} , A ₀ =V _{IH}

T3.2 1152

1. X can be V_{IL} or V_{IH}, but no other value.

Note: V_{PPH} = 11.4-12.6V, V_H = 11.4-12.6V

TABLE 4: OPERATION MODES SELECTION FOR SST27SF010/020

Mode	CE#	OE#	PGM#	A ₉	V _{PP}	DQ	Address
Read	V _{IL}	V _{IL}	X ¹	A _{IN}	V _{DD} or V _{SS}	D _{OUT}	A _{IN}
Output Disable	V _{IL}	V _{IH}	X	X	V _{DD} or V _{SS}	High Z	A _{IN}
Program	V _{IL}	V _{IH}	V _{IL}	A _{IN}	V _{PPH}	D _{IN}	A _{IN}
Standby	V _{IH}	X	X	X	V _{DD} or V _{SS}	High Z	X
Chip-Erase	V _{IL}	V _{IH}	V _{IL}	V _H	V _{PPH}	High Z	X
Program/Erase Inhibit	V _{IH}	X	X	X	V _{PPH}	High Z	X
Product Identification	V _{IL}	V _{IL}	X	V _H	V _{DD} or V _{SS}	Manufacturer's ID (BFH) Device ID ²	A _{MS} ³ - A ₁ =V _{IL} , A ₀ =V _{IL} A _{MS} ³ - A ₁ =V _{IL} , A ₀ =V _{IH}

T4.2 1152

1. X can be V_{IL} or V_{IH}, but no other value.

2. Device ID = A5H for SST27SF010 and A6H for SST27SF020

3. A_{MS} = Most significant address

A_{MS} = A₁₆ for SST27SF010 and A₁₇ for SST27SF020

Note: V_{PPH} = 11.4-12.6V, V_H = 11.4-12.6V



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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{DD}+0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to $V_{DD}+2.0V$
Voltage on A_9 and V_{PP} Pin to Ground Potential	-0.5V to 14.0V
Package Power Dissipation Capability ($T_a = 25^\circ C$)	1.0W
Through Hold Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ¹	100 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}	V_{PP}
Commercial	0°C to +70°C	4.5-5.5V	11.4-12.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	10 ns
Output Load	$C_L = 100$ pF for 90 ns
Output Load	$C_L = 30$ pF for 70 ns
See Figures 9 and 10	

TABLE 5: READ MODE DC OPERATING CHARACTERISTICS FOR SST27SF512/010/020
 $V_{DD} = 4.5-5.5V$, $V_{PP}=V_{DD}$ OR V_{SS} ($T_a = 0^\circ C$ to +70°C (Commercial))

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	V_{DD} Read Current		30	mA	Address input= V_{ILT}/V_{IHT} at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max
I_{PPR}	V_{PP} Read Current		100	μA	CE#=OE#= V_{IL} , all I/Os open Address input= V_{ILT}/V_{IHT} at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max, $V_{PP}=V_{DD}$
I_{SB1}	Standby V_{DD} Current (TTL input)		3	mA	CE#= V_{IH} , $V_{DD}=V_{DD}$ Max
I_{SB2}	Standby V_{DD} Current (CMOS input)		100	μA	CE#= $V_{DD}-0.3$ $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{IH}	Input High Voltage	2.0	$V_{DD}+0.5$	V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.2	V	$I_{OL}=2.1$ mA, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	2.4		V	$I_{OH}=-400$ μA , $V_{DD}=V_{DD}$ Min
I_H	Supervoltage Current for A_9		200	μA	CE#=OE#= V_{IL} , $A_9=V_H$ Max

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TABLE 6: PROGRAM/ERASE DC OPERATING CHARACTERISTICS FOR SST27SF512
 $V_{DD}=4.5-5.5V$, $V_{PP}=V_{PPH}$ ($T_a=25^{\circ}C \pm 5^{\circ}C$)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	V_{DD} Erase or Program Current		30	mA	$CE\#=V_{IL}$, $OE\#/V_{PP}=11.4-12.6V$, $V_{DD}=V_{DD}$ Max
I_{PP}	V_{PP} Erase or Program Current		3	mA	$CE\#=V_{IL}$, $OE\#/V_{PP}=11.4-12.6V$, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
V_H	Supervoltage for A_9	11.4	12.6	V	$CE\#=OE\#/V_{PP}=V_{IL}$,
I_H	Supervoltage Current for A_9		200	μA	$CE\#=OE\#/V_{PP}=V_{IL}$, $A_9=V_H$ Max
V_{PPH}	High Voltage for $OE\#/V_{PP}$ Pin	11.4	12.6	V	

T6.5 1152

TABLE 7: PROGRAM/ERASE DC OPERATING CHARACTERISTICS FOR SST27SF010/020
 $V_{DD}=4.5-5.5V$, $V_{PP}=V_{PPH}$ ($T_a=25^{\circ}C \pm 5^{\circ}C$)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	V_{DD} Erase or Program Current		30	mA	$CE\#=PGM\#=V_{IL}$, $OE\#=V_{IH}$, $V_{PP}=11.4-12.6V$, $V_{DD}=V_{DD}$ Max
I_{PP}	V_{PP} Erase or Program Current		3	mA	$CE\#=PGM\#=V_{IL}$, $OE\#=V_{IH}$, $V_{PP}=11.4-12.6V$, $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
V_H	Supervoltage for A_9	11.4	12.6	V	$CE\#=OE\#=V_{IL}$,
I_H	Supervoltage Current for A_9		200	μA	$CE\#=OE\#=V_{IL}$, $A_9=V_H$ Max
V_{PPH}	High Voltage for V_{PP} Pin	11.4	12.6	V	

T7.5 1152

TABLE 8: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	μs
$T_{PU-WRITE}^1$	Power-up to Write Operation	100	μs

T8.1 1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: CAPACITANCE ($T_a = 25^{\circ}C$, $f=1$ Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
C_{IN}^1	Input Capacitance	$V_{IN} = 0V$	6 pF

T9.0 1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}^1	Endurance	1000	Cycles	JEDEC Standard A117
T_{DR}^1	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}^1	Latch Up	100	mA	JEDEC Standard 78

T10.2 1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



AC CHARACTERISTICS

TABLE 11: READ CYCLE TIMING PARAMETERS $V_{DD} = 4.5-5.5V$ ($T_a = 0^\circ C$ to $+70^\circ C$ (Commercial))

Symbol	Parameter	SST27SF512-70 SST27SF010-70 SST27SF020-70		SST27SF512-90 SST27SF010-90 SST27SF020-90		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}^1	CE# Low to Active Output	0		0		ns
T_{OLZ}^1	OE# Low to Active Output	0		0		ns
T_{CHZ}^1	CE# High to High-Z Output		25		30	ns
T_{OHZ}^1	OE# High to High-Z Output		25		30	ns
T_{OH}^1	Output Hold from Address Change	0		0		ns

T11.2 1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: PROGRAM/ERASE CYCLE TIMING PARAMETERS FOR SST27SF512

Symbol	Parameter	Min	Max	Units
T_{AS}	Address Setup Time	1		μs
T_{AH}	Address Hold Time	1		μs
T_{PRT}	OE#/V _{PP} Pulse Rise Time	50		ns
T_{VPS}	OE#/V _{PP} Setup Time	1		μs
T_{VPH}	OE#/V _{PP} Hold Time	1		μs
T_{PW}	CE# Program Pulse Width	20	30	μs
T_{EW}	CE# Erase Pulse Width	100	500	ms
T_{DS}	Data Setup Time	1		μs
T_{DH}	Data Hold Time	1		μs
T_{VR}	OE#/V _{PP} and A ₉ Recovery Time	1		μs
T_{ART}	A ₉ Rise Time to 12V during Erase	50		ns
T_{A9S}	A ₉ Setup Time during Erase	1		μs
T_{A9H}	A ₉ Hold Time during Erase	1		μs

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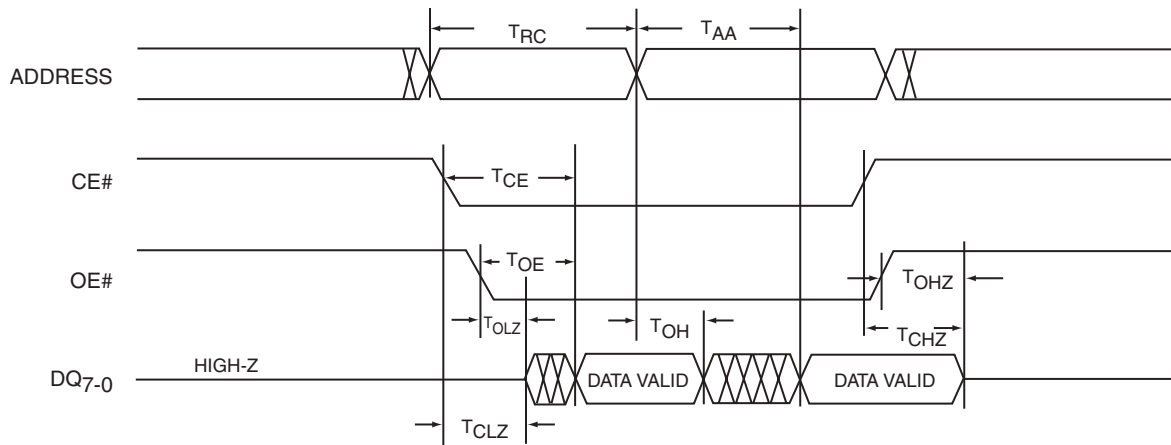
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TABLE 13: PROGRAM/ERASE CYCLE TIMING PARAMETERS FOR SST27SF010/020

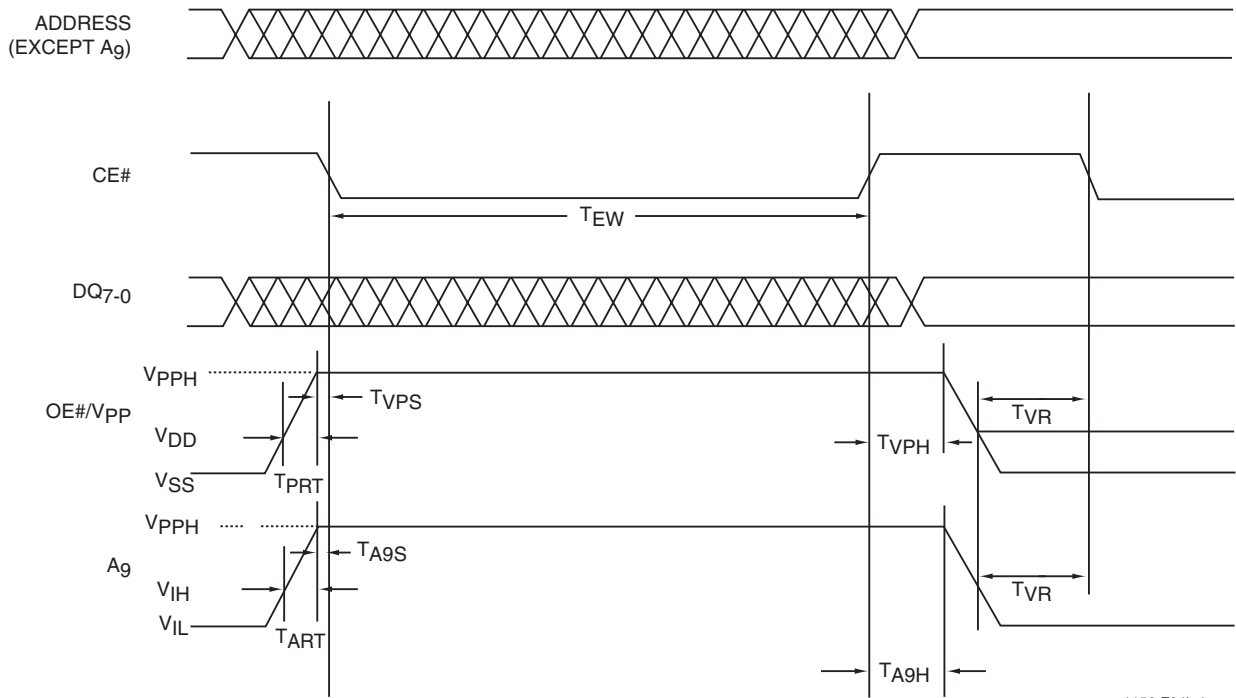
Symbol	Parameter	Min	Max	Units
T _{CES}	CE# Setup Time	1		μs
T _{CEH}	CE# Hold Time	1		μs
T _{AS}	Address Setup Time	1		μs
T _{AH}	Address Hold Time	1		μs
T _{PRT}	V _{PP} Pulse Rise Time	50		ns
T _{VPS}	V _{PP} Setup Time	1		μs
T _{VPH}	V _{PP} Hold Time	1		μs
T _{PW}	PGM# Program Pulse Width	20	30	μs
T _{EW}	PGM# Erase Pulse Width	100	500	ms
T _{DS}	Data Setup Time	1		μs
T _{DH}	Data Hold Time	1		μs
T _{VR}	A ₉ Recovery Time for Erase	1		μs
T _{ART}	A ₉ Rise Time to 12V during Erase	50		ns
T _{A9S}	A ₉ Setup Time during Erase	1		μs
T _{A9H}	A ₉ Hold Time during Erase	1		μs

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FIGURE 4: READ CYCLE TIMING DIAGRAM FOR SST27SF512/010/020



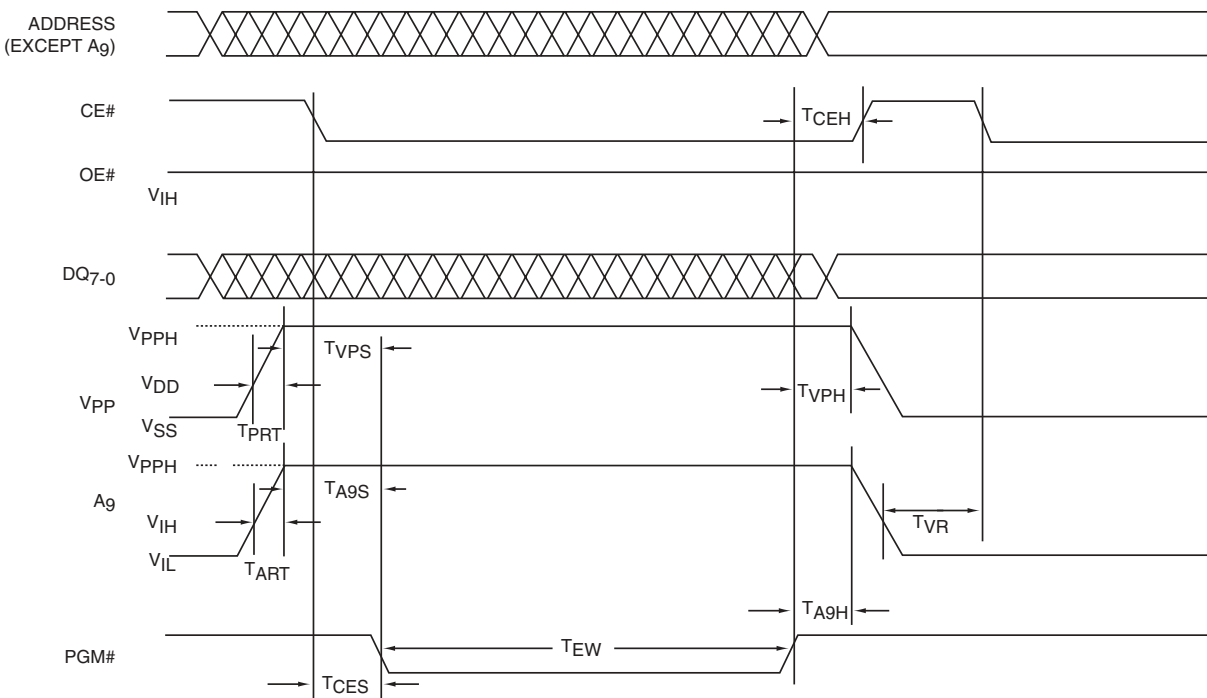
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FIGURE 5: CHIP-ERASE TIMING DIAGRAM FOR SST27SF512



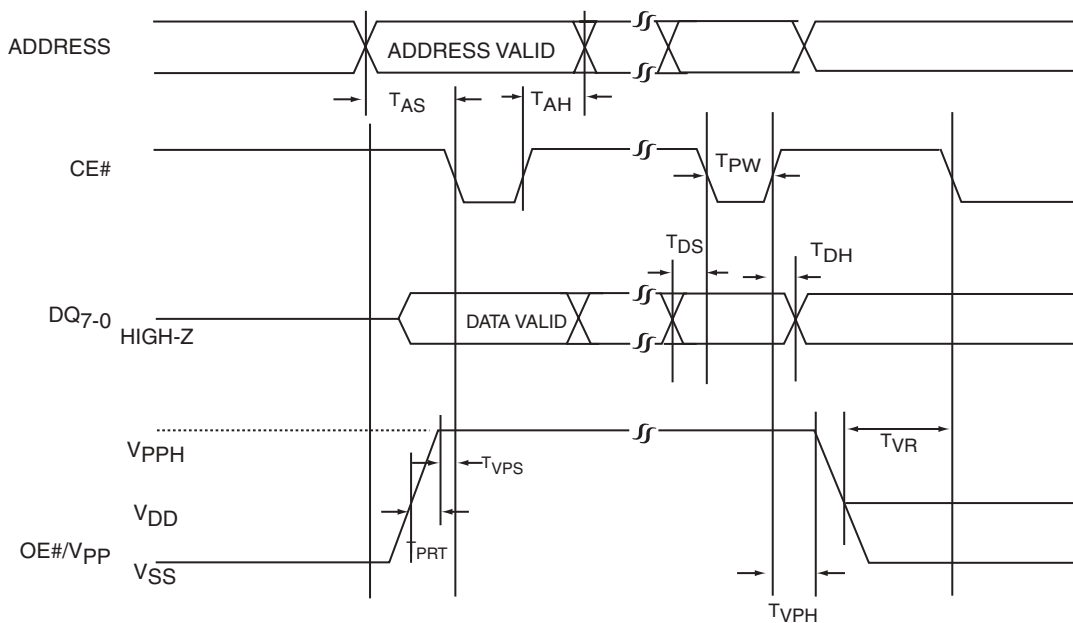
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FIGURE 6: CHIP-ERASE TIMING DIAGRAM FOR SST27SF010/020



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FIGURE 7: BYTE-PHASE PROGRAMMING TIMING DIAGRAM FOR SST27SF512

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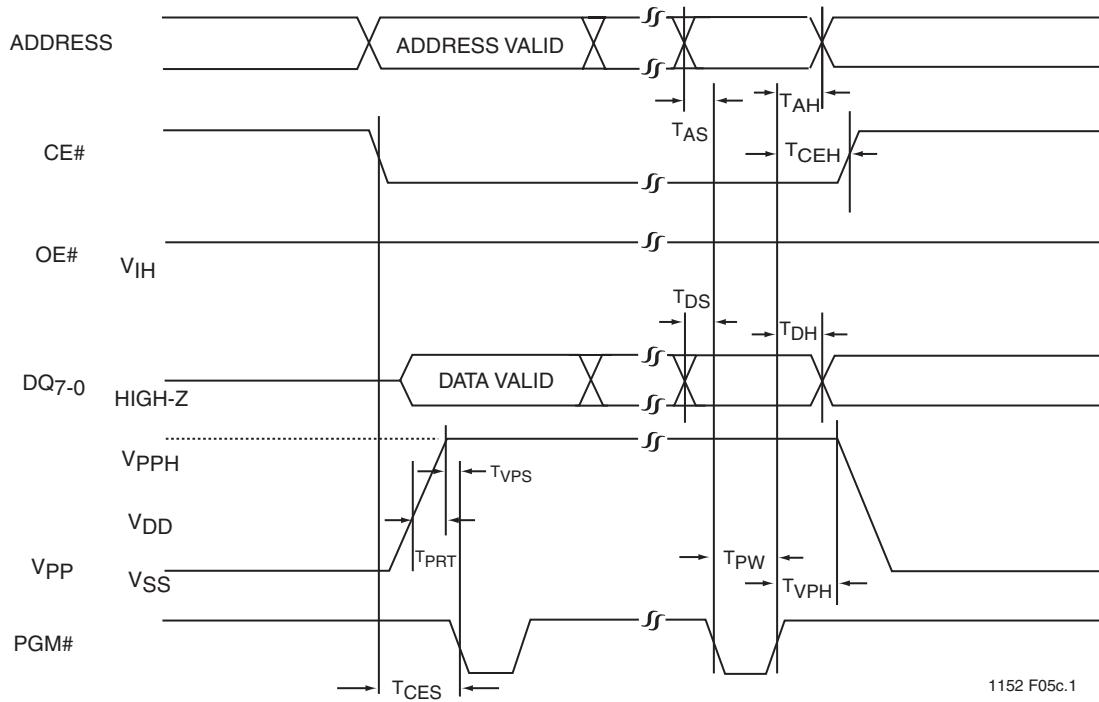
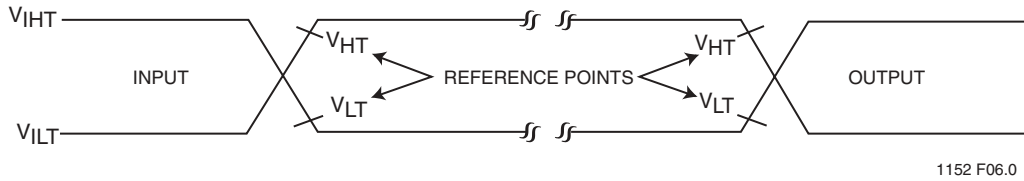


FIGURE 8: BYTE-PROGRAM TIMING DIAGRAM FOR SST27SF010/020



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AC test inputs are driven at V_{IHT} (2.4 V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Input rise and fall times (10% \leftrightarrow 90%) are <10 ns.

Note: V_{HT} - V_{HIGH} Test
 V_{LT} - V_{LOW} Test
 V_{IHT} - $V_{INPUT HIGH}$ Test
 V_{ILT} - $V_{INPUT LOW}$ Test

FIGURE 9: AC INPUT/OUTPUT REFERENCE WAVEFORMS

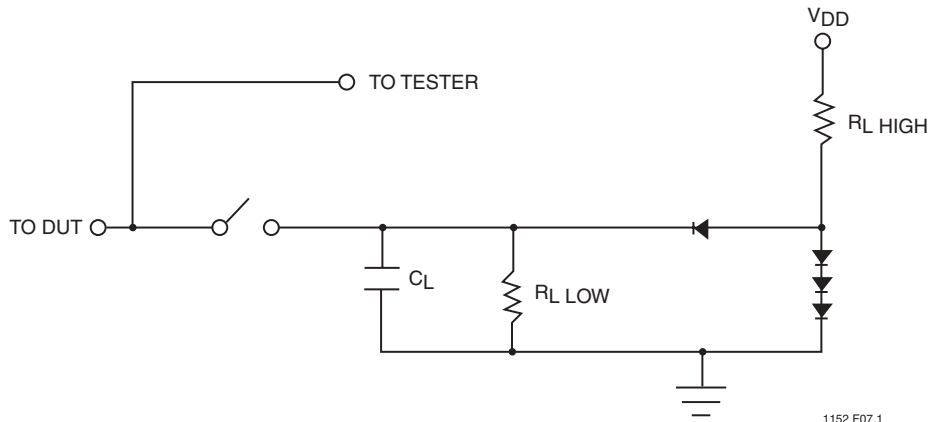


FIGURE 10: A TEST LOAD EXAMPLE

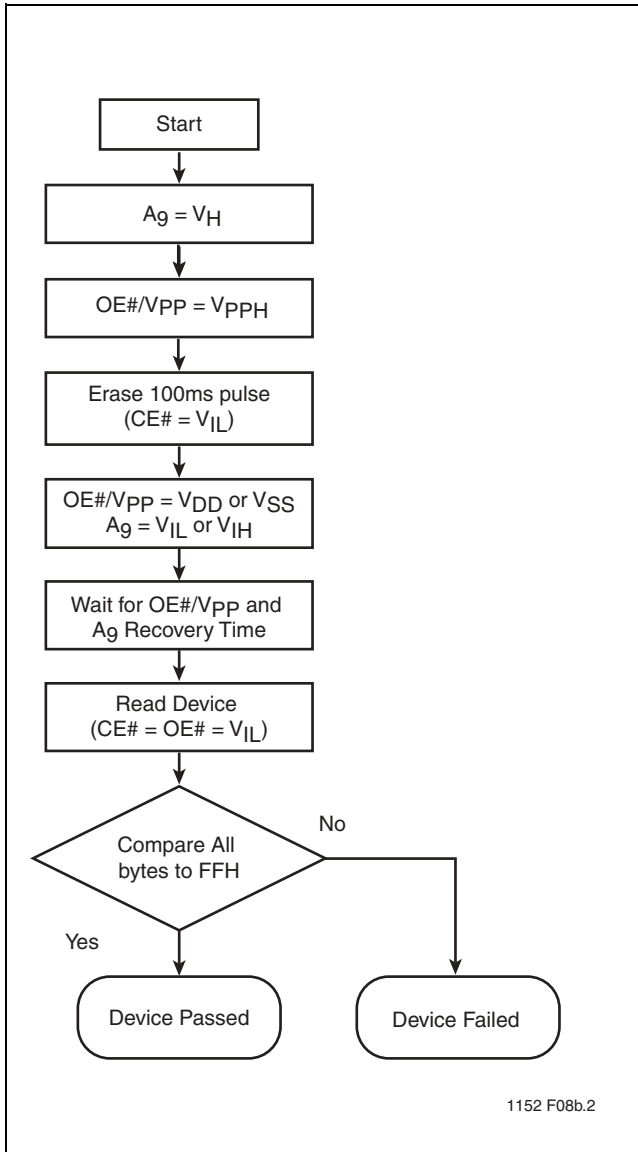


FIGURE 11: CHIP-ERASE ALGORITHM FOR
 SST27SF512

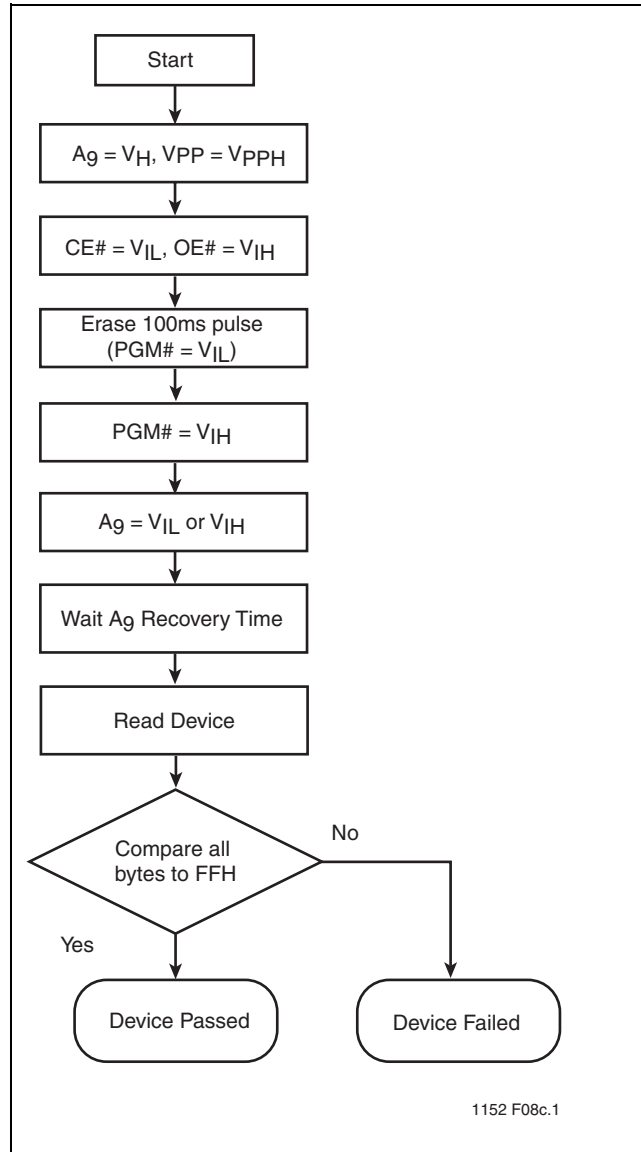


FIGURE 12: CHIP-ERASE ALGORITHM FOR
 SST27SF010/020



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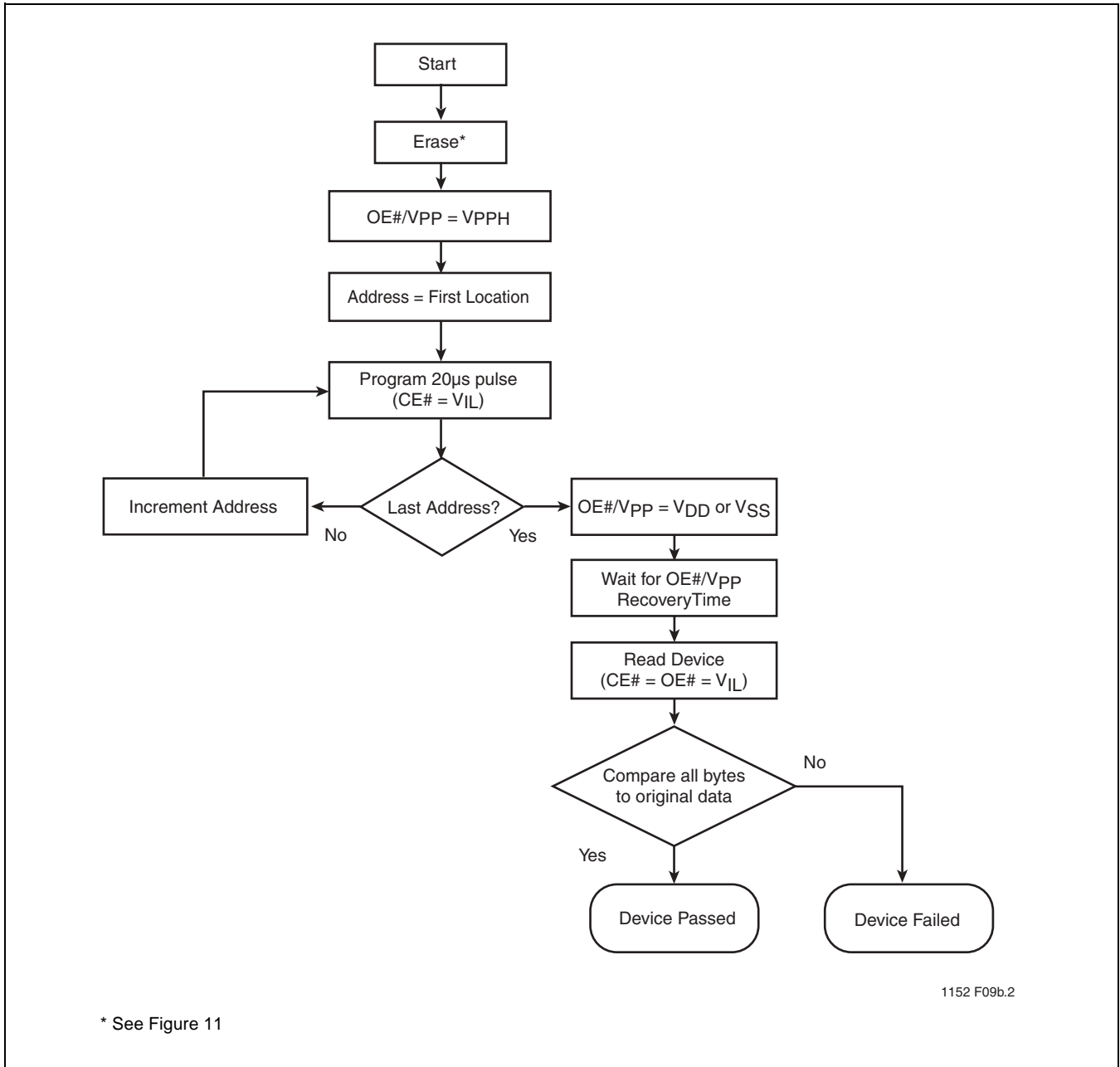
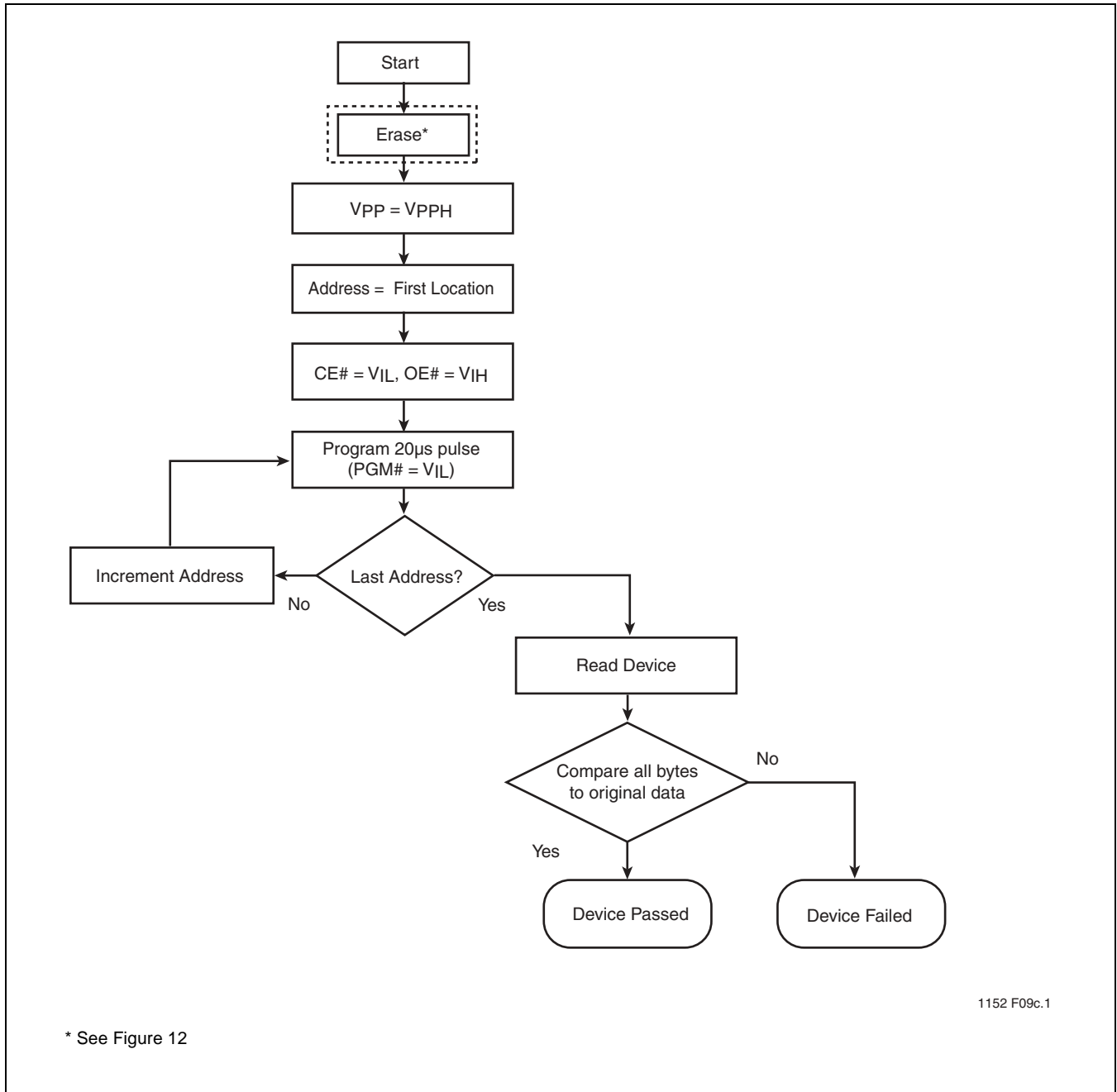


FIGURE 13: BYTE-PROGRAM ALGORITHM FOR SST27SF512



* See Figure 12

1152 F09c.1

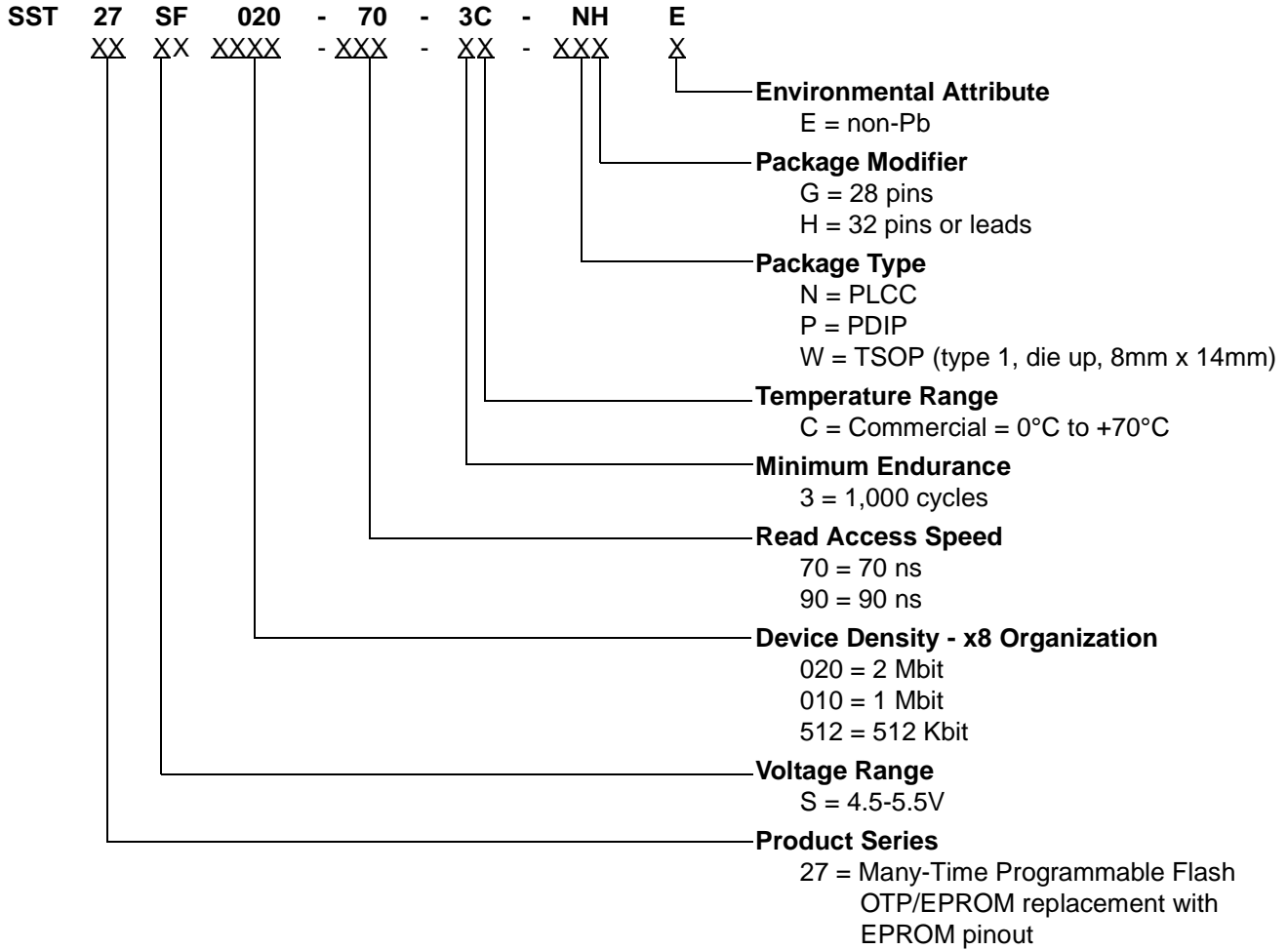
FIGURE 14: BYTE-PROGRAM ALGORITHM FOR SST27SF010/020



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PRODUCT ORDERING INFORMATION





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Valid combinations for SST27SF512

SST27SF512-70-3C-NH	SST27SF512-70-3C-WH	SST27SF512-70-3C-PG
SST27SF512-70-3C-NHE	SST27SF512-70-3C-WHE	SST27SF512-70-3C-PGE
SST27SF512-90-3C-NH	SST27SF512-90-3C-WH	SST27SF512-90-3C-PG
SST27SF512-90-3C-NHE	SST27SF512-90-3C-WHE	SST27SF512-90-3C-PGE

Valid combinations for SST27SF010

SST27SF010-70-3C-NH	SST27SF010-70-3C-WH	SST27SF010-70-3C-PH
SST27SF010-70-3C-NHE	SST27SF010-70-3C-WHE	SST27SF010-70-3C-PHE
SST27SF010-90-3C-NH	SST27SF010-90-3C-WH	SST27SF010-90-3C-PH
SST27SF010-90-3C-NHE	SST27SF010-90-3C-WHE	SST27SF010-90-3C-PHE

Valid combinations for SST27SF020

SST27SF020-70-3C-NH	SST27SF020-70-3C-WH	SST27SF020-70-3C-PH
SST27SF020-70-3C-NHE	SST27SF020-70-3C-WHE	SST27SF020-70-3C-PHE
SST27SF020-90-3C-NH	SST27SF020-90-3C-WH	SST27SF020-90-3C-PH
SST27SF020-90-3C-NHE	SST27SF020-90-3C-WHE	SST27SF020-90-3C-PHE

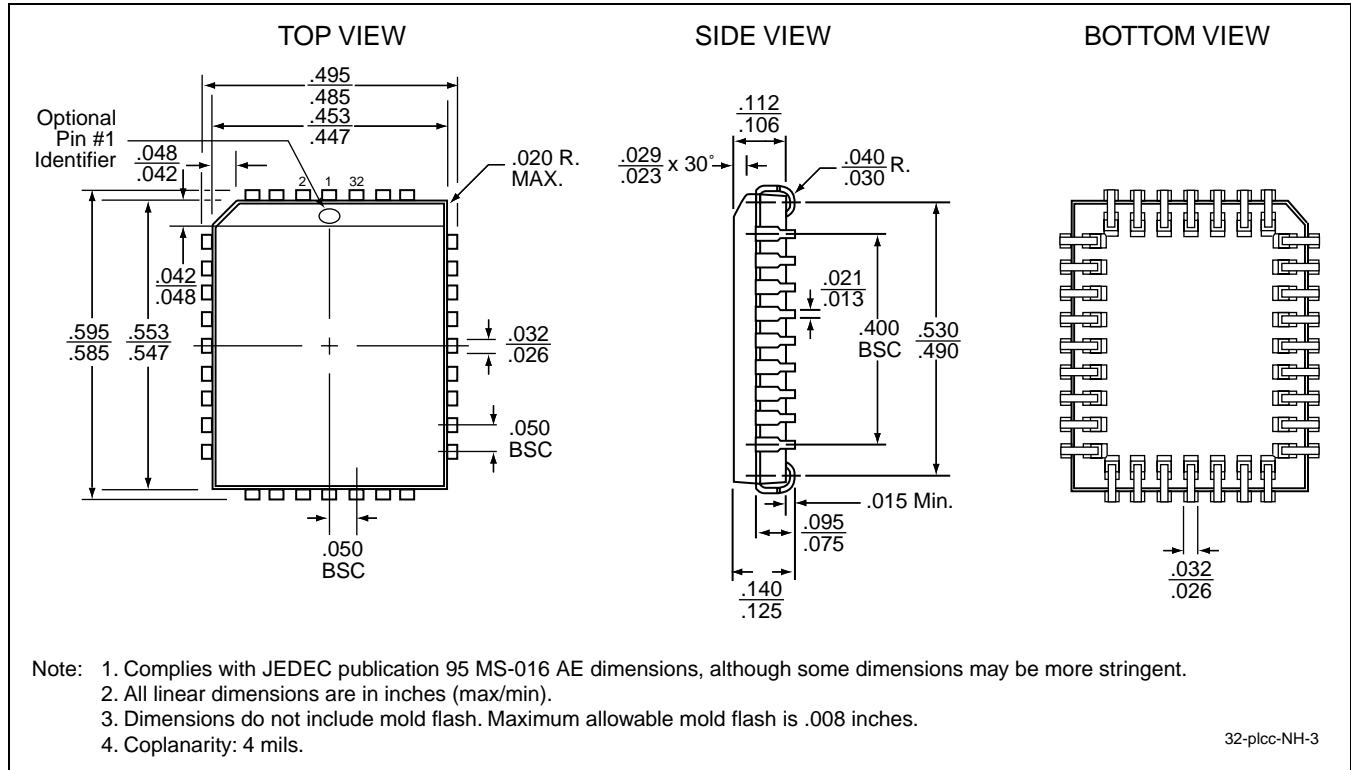
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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PACKAGING DIAGRAMS

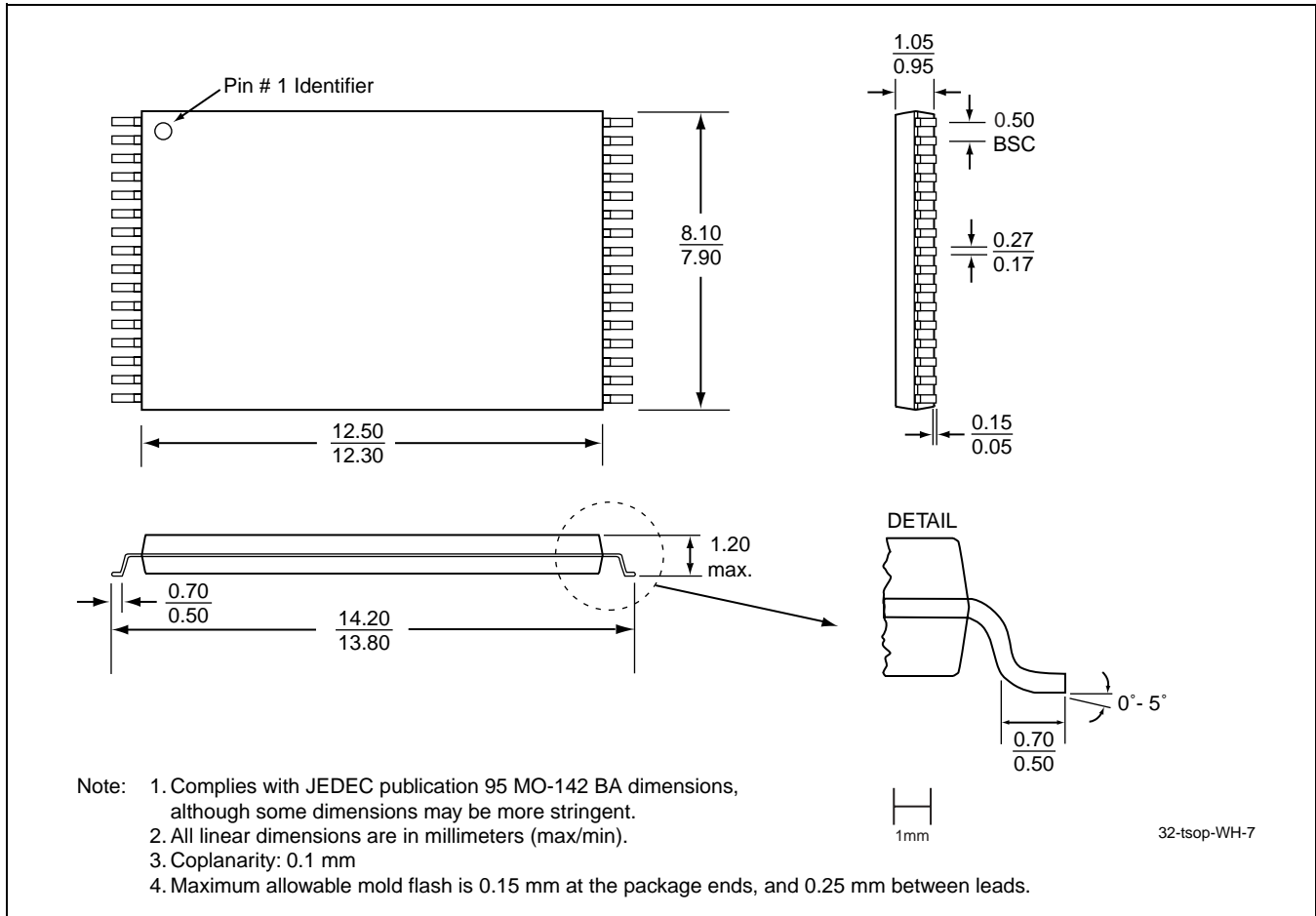


32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



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Data Sheet

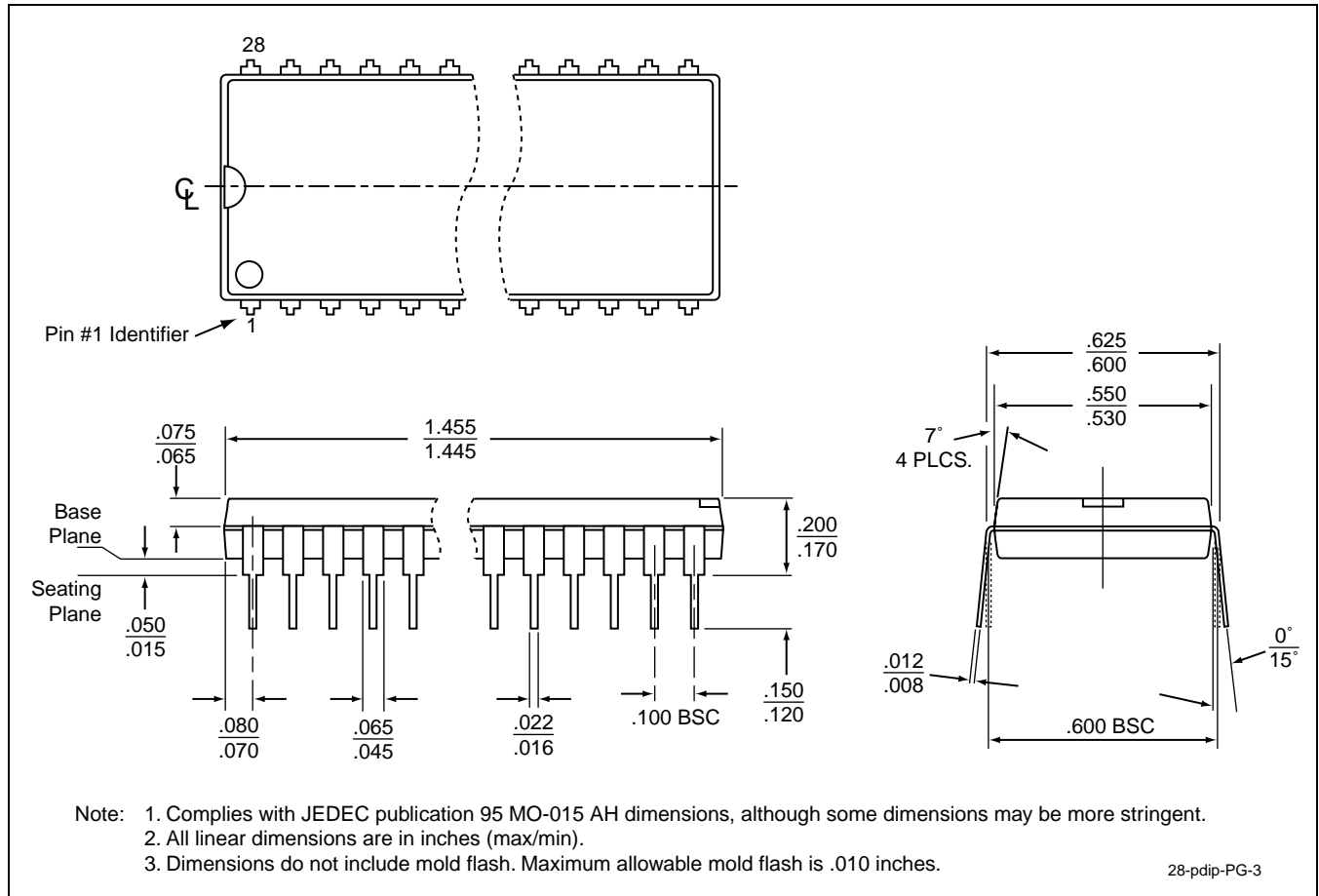


32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH



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Data Sheet

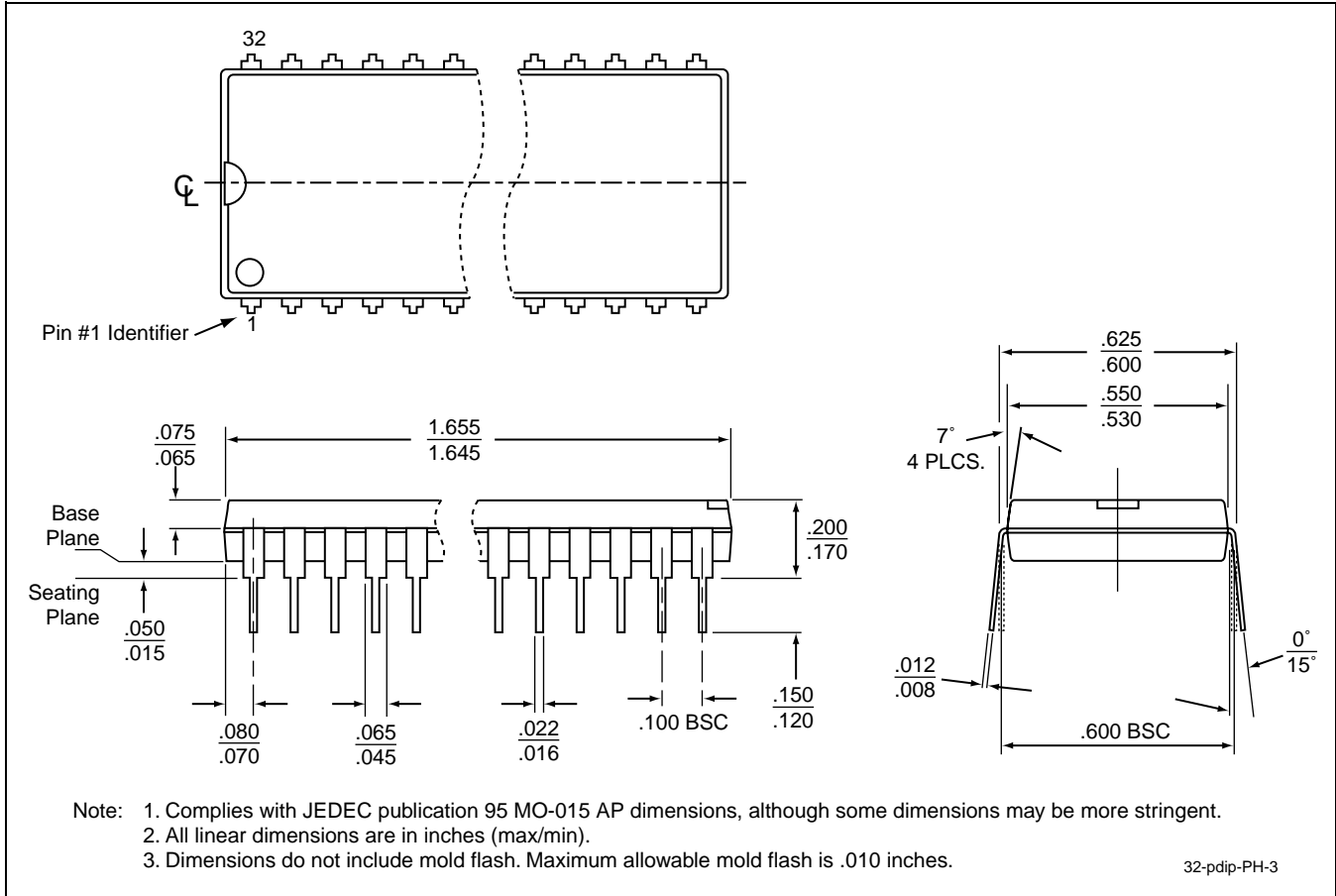


28-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PG



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32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)

SST PACKAGE CODE: PH

TABLE 14: REVISION HISTORY

Number	Description	Date
02	• 2002 Data Book	Feb 2002
03	• Document Control Release (SST Internal): No technical changes	Apr 2002
04	• Corrected I _H Supervoltage Current for A ₉ from 100μA to 200μA in Tables 5, 6, and 7	Jul 2002
05	• Corrected the Test Conditions for I _{DD} and I _{PPR} in Table 5 on page 7	Sep 2003
06	• Corrected the Max value for I _{PP} from 1 mA to 3 mA (See Tables 6 and 7) • Added MPNs for non-PB packages (See page 19)	Nov 2003
07	• 2004 Data Book • Corrected caption for Figure 5 from “Read Cycle” to “Chip-Erase”	Nov 2003
08	• Removed 256 Kbit parts - refer to EOL Product Data Sheet S71152(02)	Apr 2004