DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC842GR-9LG, μPC4742GR-9LG

SINGLE POWER SUPPLY, HIGH SPEED, WIDE BAND, DUAL OPERATIONAL AMPLIFIERS

DESCRIPTION

The μPC842GR-9LG, μPC4742GR-9LG are a high speed version of the operational amplifier μPC1251GR-9LG, μPC1251MP-KAA, μPC358GR-9LG for general single power supply use with high speed pulse response and high stabilization. A high speed PNP transistor is used in the circuit which improves the characteristics such as a slew rate, gain-bandwidth product, stabilization of the withstand load capacitance, with no crossover distortion compared to μPC1251GR-9LG, μPC 1251MP-KAA, μPC358GR-9LG.

Therefore, μPC842GR-9LG, μPC4742GR-9LG can be used in a wide range of application circuits for single power supply AC amplifier, active filters, line driver and an amplifier for light receiving element etc.

The μPC842GR-9LG which expands temperature type is suited for wide operating ambient temperature use, and μPC4742GR-9LG is used for general purposes.

μPC844GR-9LG, μPC4744GR-9LG which are quad types with the same circuit configuration are also available as series of operational amplifiers.

FEATURES

- Slew Rate (A_V = +1) 7 V/μs (TYP.) (V^+ = +5 V, V^- = GND)
- Gain Band Width Product 3.5 MHz (TYP.)
- Input Offset Voltage ±2 mV (TYP.)
- Input Offset Current ±6 nA (TYP.)
- Wide operating ambient temperature range
  μPC842GR-9LG: T_A = –40 to +125°C, μPC4742GR-9LG: T_A = –40 to +85°C
- Small Package (The mounting area is reduced to about 60% compared to the conventional 8-pin plastic SOP (1.27 mm pitch))
- Stability to capacitive loads (load capacity, 1000 pF)
- Internal frequency compensation
- Output short-circuit protection
- A pin connection (pin compatible) of a standard dual operational amplifier.

ORDERING INFORMATION

Part Number	Selected Grade	Package	Package Type
μPC842GR-9LG-E1-A Note	Standard	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC842GR-9LG-E2-A Note	Standard	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC4742GR-9LG-E1-A Note	Standard	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC4742GR-9LG-E2-A Note	Standard	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

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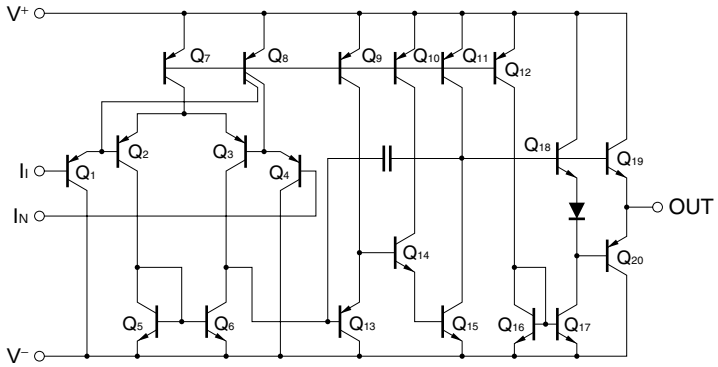
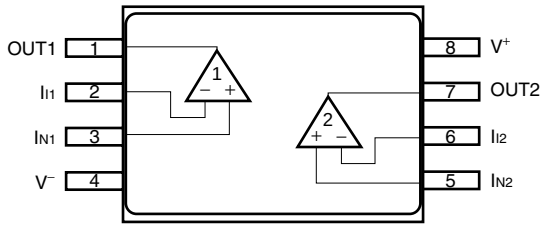
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Marking side)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	μPC842GR-9LG	μPC4742GR-9LG	Unit
Voltage between V^+ and V^- **Note1**	$V^+ - V^-$	−0.3 to +36		V
Differential Input Voltage	V_{ID}	±36		V
Input Voltage **Note2**	V_I	V^- − 0.3 to V^- + 36		V
Output applied Voltage **Note3**	V_O	V^- − 0.3 to V^+ + 0.3		V
Total Power Dissipation **Note4**	P_T	440		mW
Output Short Circuit Duration **Note5**	t_S	Indefinite		s
Operating Ambient Temperature	T_A	−40 to +125	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	−55 to +125	°C

Note1. Note that reverse connections of the power supply may damage ICs.

2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V^+. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

4. This is the value of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

μPC842GR-9LG: Derate at −5.5 mW/°C when T_A > 69°C.

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 183°C/W)

μPC4742GR-9LG: Derate at −5.5 mW/°C when T_A > 44°C.

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 183°C/W)

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, **Note 4**.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	±1.5		±16	V
Power Supply Voltage (V^- = GND)	V^+	+3	+5 to +30	+32	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1)	C_L			1000 Note	pF

Note This is the value during a feedback resistance (R_f) = 0 Ω.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V^{\pm}$ = ±15 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}			±2	±4.5	mV
Input Offset Current	I_{IO}			±6	±75	nA
Input Bias Current Note1	I_B			120	500	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2$ kΩ, V_O = ±10 V	25000	300000		
Circuit Current Note2	I_{CC}	I_O = 0 A		4.3	5.5	mA
Common Mode Rejection Ratio	CMR		70	86		dB
Supply Voltage Rejection Ratio	SVR		70	93		dB
Output Voltage Swing	V_{Om1}	R_L = 10 kΩ	±13.7	+14 −14.3		V
	V_{Om2}	$R_L \geq 2$ kΩ	±13.5			V
Common Mode Input Voltage Range	V_{ICM}		V^-		V^+ − 1.8	V
Slew Late	SR	A_V = +1 (rise)		8.5		V/μs
Gain Band Width Product	GBW	f = 100 kHz		3.5		MHz
Channel Separation		f = 20 Hz to 20 kHz		120		dB

T_A = 25°C, V^+ = +5 V, V^- = GND

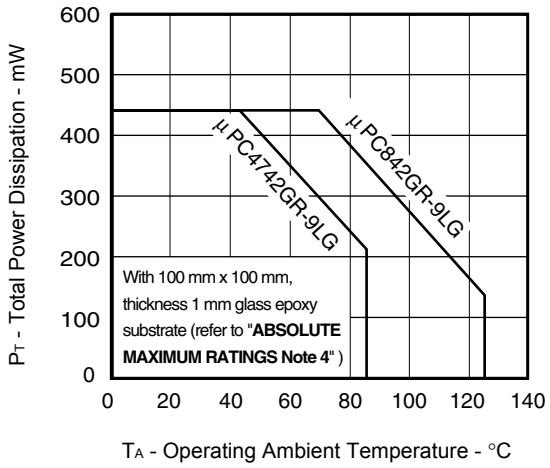
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}			±2	±5	mV
Input Offset Current	I_{IO}			±6	±75	nA
Input Bias Current Note1	I_B			140	500	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2$ kΩ	25000	300000		
Circuit Current Note2	I_{CC}	I_O = 0 A		3.3	4.5	mA
Common Mode Rejection Ratio	CMR		70	80		dB
Supply Voltage Rejection Ratio	SVR		70	95		dB
Output Voltage Swing	V_{Om}	$R_L \geq 2$ kΩ (Connect to GND)	3.7 0	4 0		V
Common Mode Input Voltage Range	V_{ICM}		0		V^+ − 1.8	V
Output Source Current	$I_{O\ SOURCE}$	$V_{IN(+)}$ = +1 V, $V_{IN(-)}$ = 0 V	10	30		mA
Output Sink Current	$I_{O\ SINK}$	$V_{IN(+)}$ = 0 V, $V_{IN(-)}$ = +1 V	10	30		mA
Slew Late	SR	A_V = +1 (rise)		7		V/μs

Notes1. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

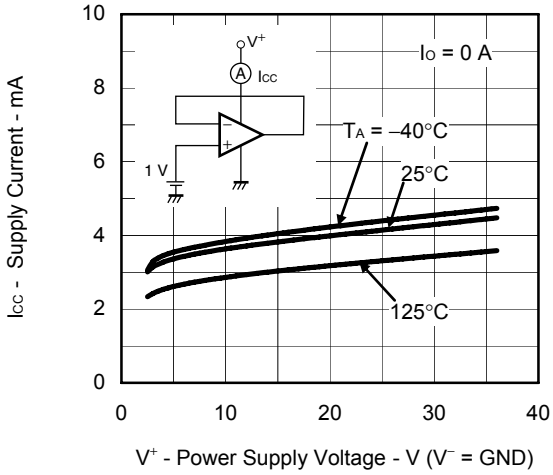
2. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, TYP.) (Reference value)

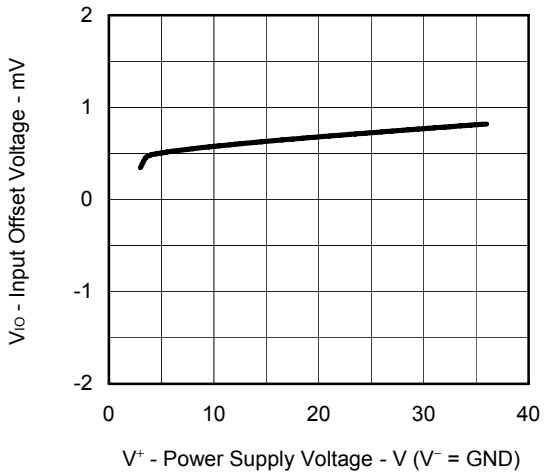
P_T vs. T_A



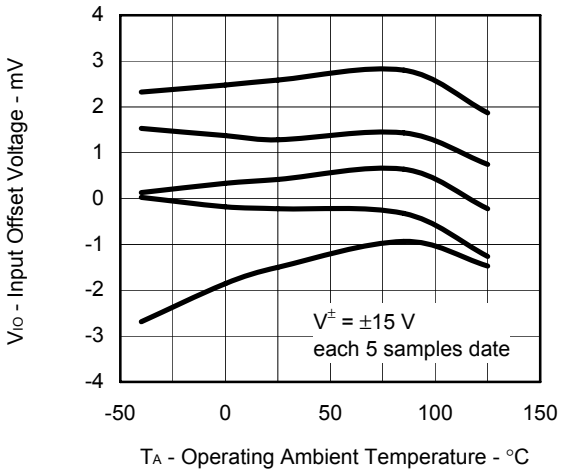
I_{CC} vs. V^+



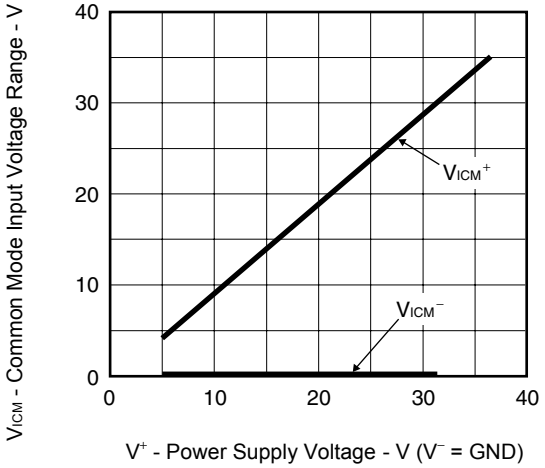
V_{IO} vs. V^+



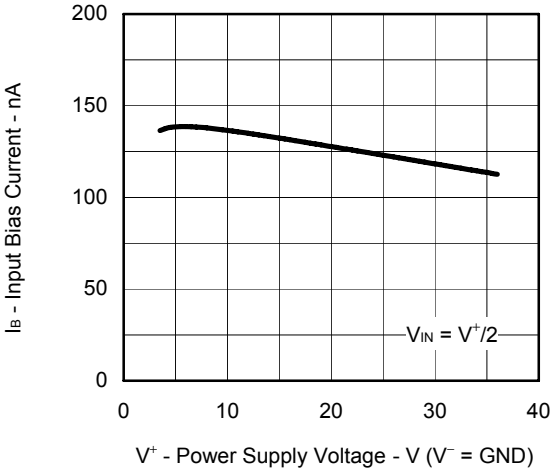
V_{IO} vs. T_A



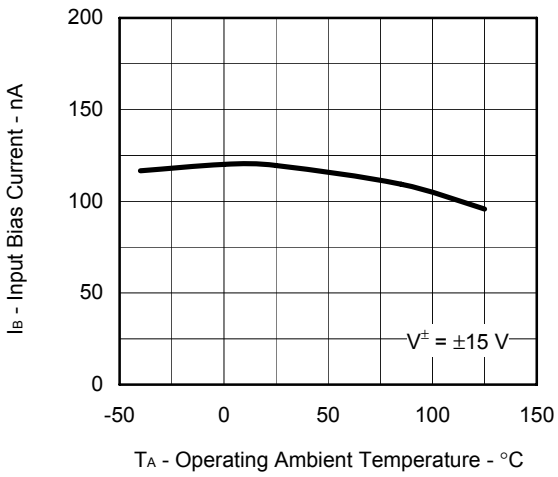
V_{ICM} vs. V^+



I_B vs. V^+



I_B vs. T_A



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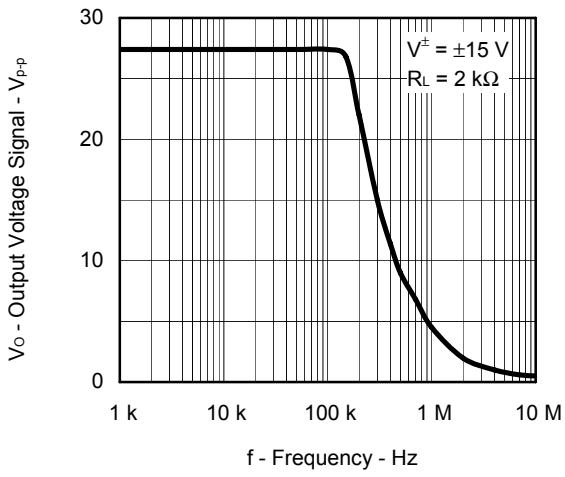
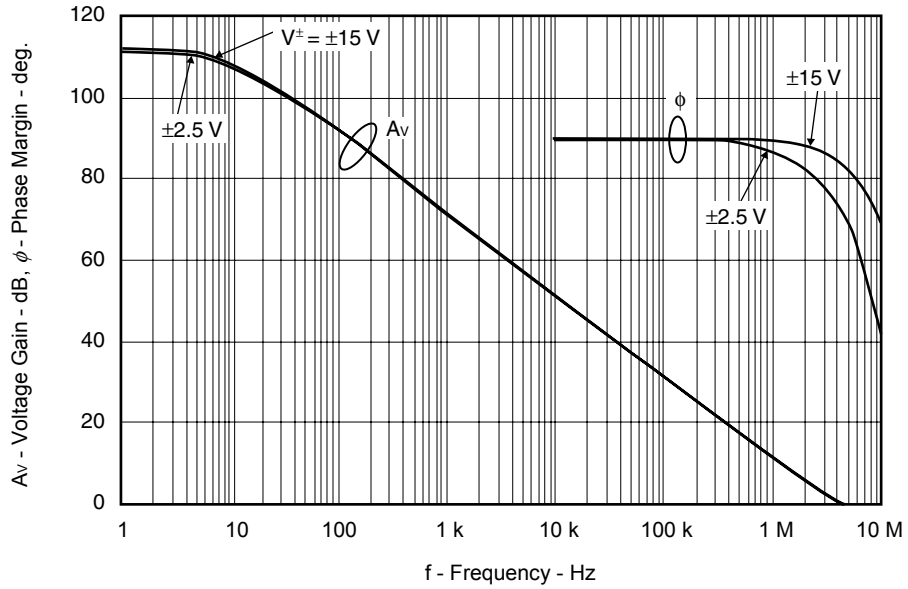
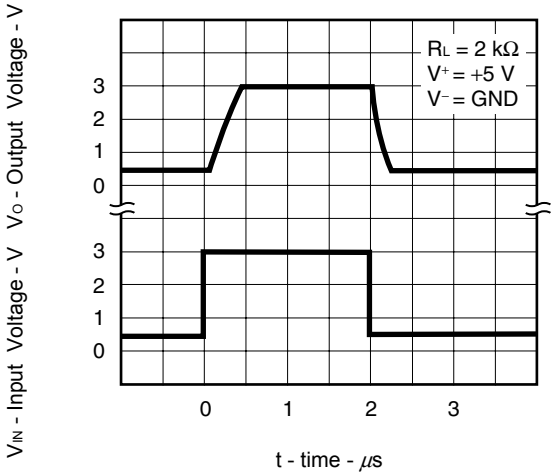
V_O vs. f



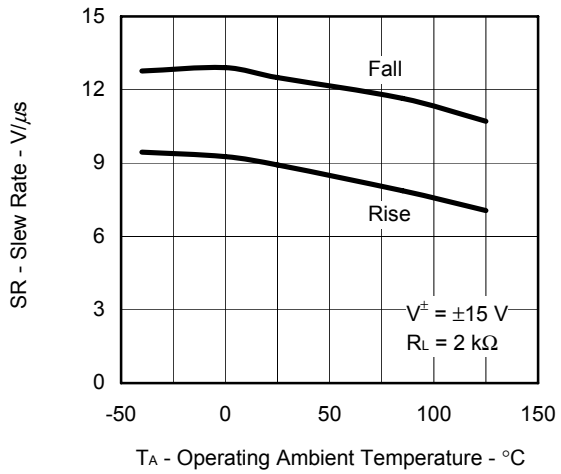
A_V, ϕ vs. f



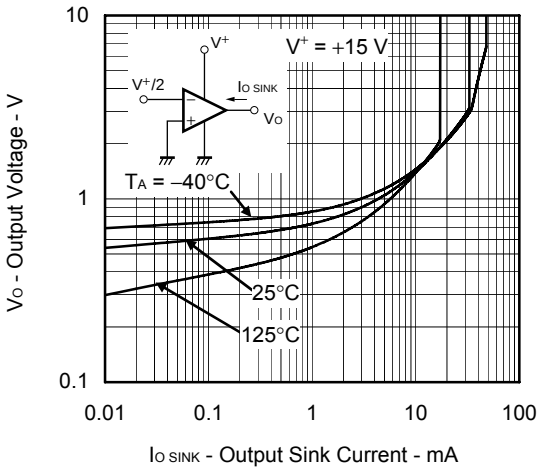
PULSE RESPONSE



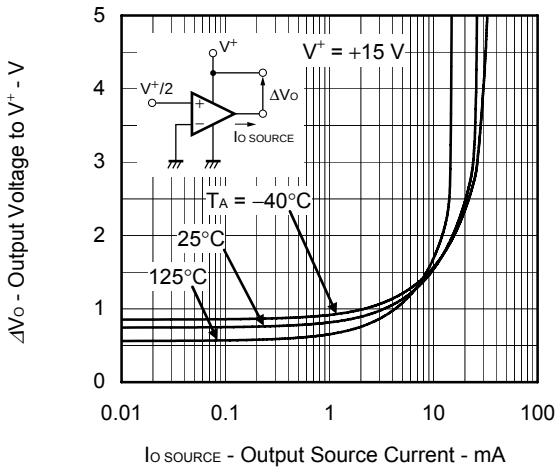
SR - T_A



V_O vs. $I_{O\ SINK}$



ΔV_O vs. $I_{O\ SOURCE}$

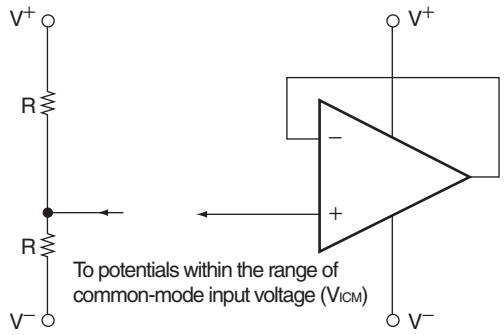


PRECAUTIONS FOR USE

O The process of unused circuits

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V^+ and V^- is applied to this example.

O Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^-, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

O Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

V_{ICM} (TYP.): V^- to $V^+ - 1.8$ (V) (T_A = 25°C)

During designing, temperature characteristics for use with allowance.

O The maximum output voltage

The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

V_{Om^+} (TYP.): $V^+ - 1$ (V) (T_A = 25°C), V_{Om^-} (TYP.): $V^- + 0.7$ (V) (T_A = 25°C)

During designing, consider variations in characteristics and temperature characteristics for use with allowance.

In addition, also note that the output voltage range ($V_{Om^+} - V_{Om^-}$) becomes narrow when an output current increases.

O Operation of output

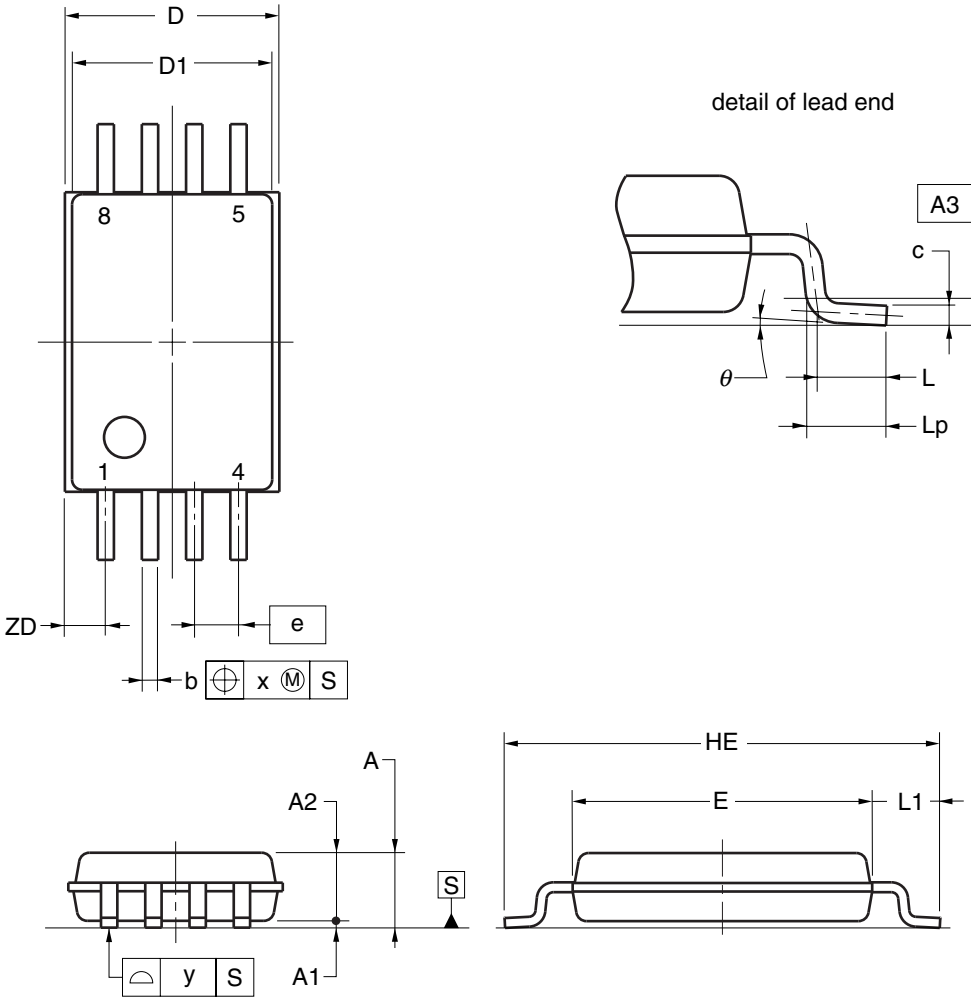
This IC will not operate an output current sinking when the output voltage is $V^- + 0.7$ V and below. In this situation, an output voltage and its level approach to the V^- side can be improved by connecting the load resistance to an output pin / V^- intermediate by sinking current at the load resistance side. (The effect will differ depending on the flow of current in the load resistance.)

O Handling of ICs

When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS (Unit: mm)

8-PIN PLASTIC TSSOP (5.72mm (225))



(UNIT:mm)

ITEM	DIMENSIONS
D	3.15±0.15
D1	3.00±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.24^{+0.06}_{-0.05}$
c	0.145±0.055
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.10
y	0.10
ZD	0.60

P8GR-65-9LG

NOTE
Each lead centerline is located within 0.10mm of its true position at maximum material condition.

RECOMMENDED SOLDERING CONDITIONS

The μPC842GR-9LG, μPC4742GR-9LG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPC842GR-9LG-A [Note], μPC4742GR-9LG-A [Note]: 8-pin plastic TSSOP (5.72 mm (225))

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 260°C, Reflow time: 60 seconds or less (at 220°C or higher), Maximum number of reflow processes: 3 times.	IR60-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Remark Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.

REFERENCE DOCUMENTS

Document Name	Document No.
QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNT MANUAL	http://www.necel.com/pkg/en/mount/index.html
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM-STANDARD LINEAR IC	IEI-1212
REVIEW OF QUALITY AND RELIABILITY HANDBOOK	C12769E
NEC SEMICONDUCTOR DEVICE RELIBIALITY/QUALITY CONTROL SYSTEM	C10983E

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