

# Radiation Hardened Ultra Low Noise, Precision Voltage Reference

## ISL71090SEH25

The ISL71090SEH25 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 4V to 30V. The ISL71090SEH25 uses the Intersil Advanced Bipolar technology to achieve sub  $2\mu V_{P-P}$  0.1Hz noise with an accuracy over temperature and radiation of 0.15%.

The ISL71090SEH25 offers a 2.5V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld Flatpack package.

The ISL71090SEH25 is ideal for high-end instrumentation, data acquisition and applications requiring high DC precision where low noise performance is critical.

## Applications

- RH voltage regulators precision outputs
- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications

## Features

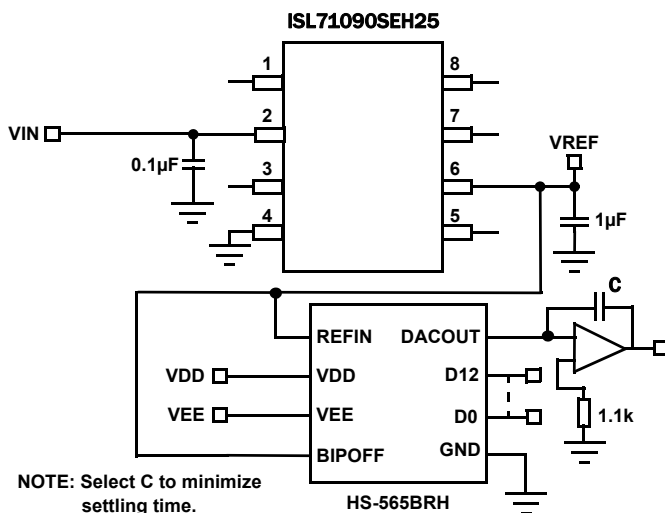
- Reference output voltage ..... **2.5V±0.05%**
- Accuracy over temperature and radiation ..... **±0.15%**
- Output voltage noise ..... **2μV<sub>P-P</sub> Typ (0.1Hz to 10Hz)**
- Supply current ..... **930μA (Typ)**
- Tempco (box method) ..... **10ppm/°C Max**
- Output current capability ..... **20mA**
- Line regulation ..... **.8ppm/V**
- Load regulation ..... **2.5ppm/mA**
- Operating temperature range ..... **-55°C to +125°C**
- Radiation environment
  - High dose rate (50-300rad(Si)/s) ..... **100krad(Si)**
  - Low dose rate (0.01rad(Si)/s) ..... **100krad(Si)\***
  - SET/SEL/SEB ..... **86MeV·cm<sup>2</sup>/mg**

\*Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate

- Electrically screened to SMD [5962-13211](#)

## Related Literature

- [AN1847](#), "ISL71090SEH25 Evaluation Board User's Guide"
- [AN1848](#), "SEE Testing of the ISL71090SEH25"
- [AN1849](#), "Radiation Report of the ISL71090SEH25"



NOTE: Select C to minimize settling time.

FIGURE 1. ISL71090SEH25 TYPICAL APPLICATION DIAGRAM

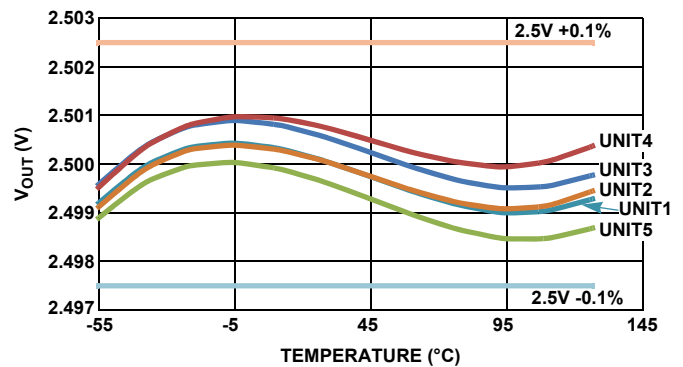


FIGURE 2.  $V_{OUT}$  vs TEMPERATURE

# ISL71090SEH25

## Ordering Information

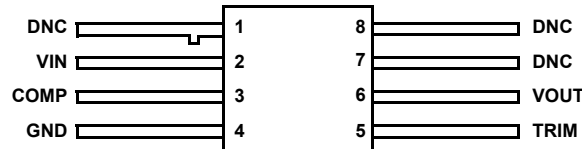
ORDERING NUMBER (Notes 1, 2, 3)	PART NUMBER	V <sub>OUT</sub> OPTION (V)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-Free)	PKG. DWG. #
5962R1321102VXC	ISL71090SEHVF25	2.50	-55 to +125	8 Ld Flatpack	K8.A
ISL71090SEHF25/PROTO	ISL71090SEHF25/PROTO	2.50	-55 to +125	8 Ld Flatpack	K8.A
ISL71090SEHF25EVAL1Z	Evaluation Board				

### NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for [ISL71090SEH25](#). For more information on MSL please see tech brief [TB363](#)
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in this "Ordering Information" table must be used when ordering.

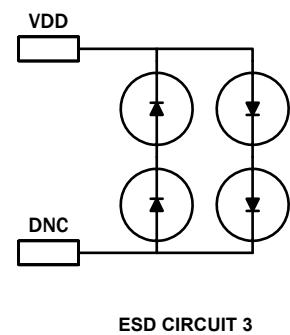
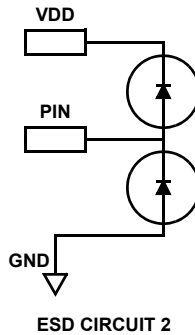
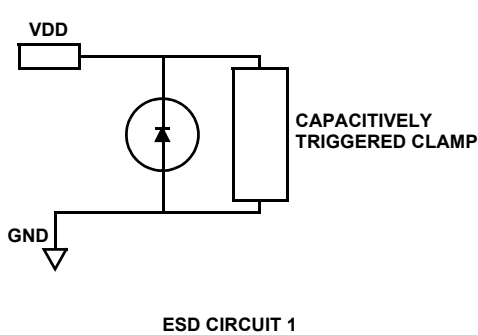
## Pin Configuration

ISL71090SEH25  
(8 LD FLATPACK)  
TOP VIEW

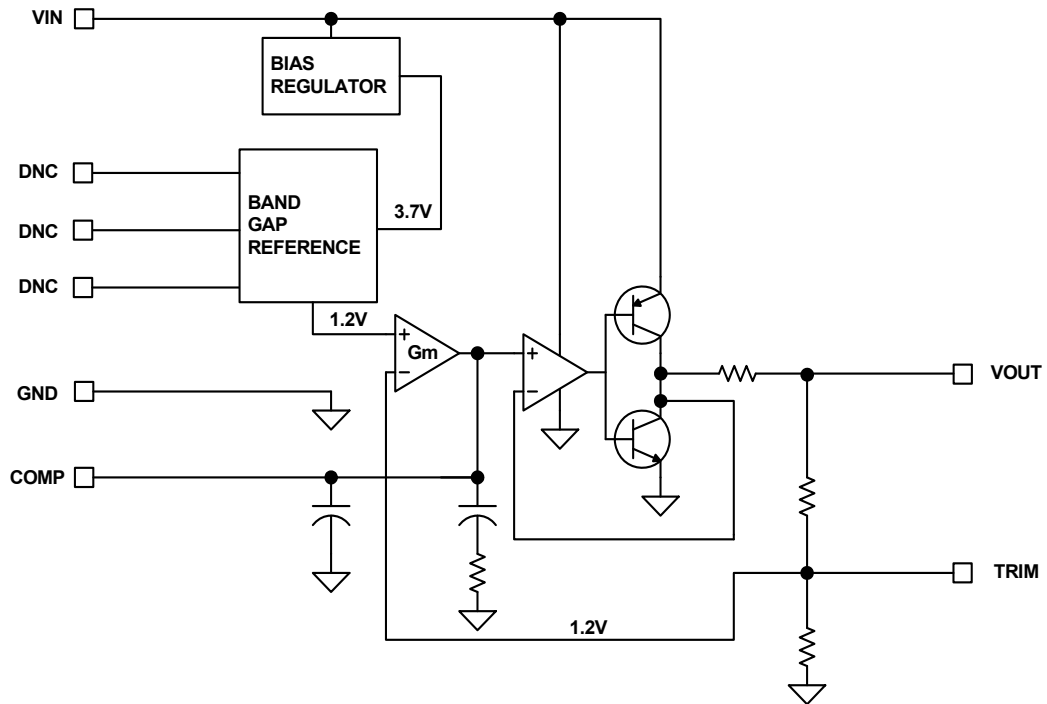


## Pin Descriptions

PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1	DNC	3	Do not Connect
2	VIN	1	Input Voltage Connection
3	COMP	2	Compensation and Noise Reduction Capacitor
4	GND	1	Ground Connection
5	TRIM	2	Voltage Reference Trim input
6	VOUT	2	Voltage Reference Output
7	DNC	3	Do not Connect
8	DNC	3	Do not Connect



## Functional Block Diagram



# ISL71090SEH25

## Absolute Maximum Ratings

Max Voltage	
$V_{IN}$ to GND	-0.5V to +40V
$V_{IN}$ to GND at an LET = 86MeV•cm <sup>2</sup> /mg	-0.5V to +36V
$V_{OUT}$ to GND (10s)	-0.5V to $V_{OUT} + 0.5V$
Voltage on any Pin to Ground	-0.5V to $+V_{OUT} + 0.5V$
Voltage on DNC Pins	No connections permitted to these pins
Input Voltage Slew Rate (Max)	0.1V/ $\mu$ s
ESD Ratings	
Human Body Model	3kV
Machine Model	200V
Charged Device Model	2kV

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld Flatpack Package (Notes 4, 5)	140	15
Storage Temperature Range	-65°C to +150°C	
Maximum Junction Temperature ( $T_{JMAX}$ )	+150°C	
Pb-Free Reflow Profile (Note 6)	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

## Recommended Operating Conditions

$V_{IN}$	4.0V to +30V
Temperature Range	-55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the ceramic on the package underside.
- Post-reflow drift for the ISL71090SEH25 devices can be 100 $\mu$ V typical based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.
- Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate.
- The output capacitance used for SEE testing is 0.1 $\mu$ F for  $C_{IN}$  and  $C_{OUT}$ .

**Electrical Specifications**  $V_{IN} = 5V$ ,  $I_{OUT} = 0$ , unless otherwise specified. **Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$V_{OUT}$	Output Voltage	$V_{IN} = 5V$		2.5		V
$V_{OA}$	$V_{OUT}$ Accuracy @ $T_A = +25^\circ C$ (Note 6)	$V_{OUT} = 2.5V$	-0.05		+0.05	%
$V_{OA}$	$V_{OUT}$ Accuracy @ $T_A = -55^\circ C$ to +125°C	$V_{OUT} = 2.5V$	<b>-0.15</b>		<b>+0.15</b>	%
$V_{OA}$	$V_{OUT}$ Accuracy @ $T_A = -55^\circ C$ to +125°C, Post Rad	$V_{OUT} = 2.5V$	<b>-0.152</b>		<b>+0.152</b>	%
TC $V_{OUT}$	Output Voltage Temperature Coefficient (Note 10)				<b>10</b>	ppm/°C
$V_{IN}$	Input Voltage Range	$V_{OUT} = 2.5V$	<b>4</b>		<b>30</b>	V
$I_{IN}$	Supply Current			0.930	<b>1.28</b>	mA
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	$V_{IN} = 4V$ to 30V, $V_{OUT} = 2.5V$		8	<b>18</b>	ppm/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	Sourcing: 0mA $\leq I_{OUT} \leq$ 20mA		20	<b>35</b>	ppm/mA
		Sinking: -10mA $\leq I_{OUT} \leq$ 0mA		40	<b>70</b>	ppm/mA
$V_D$	Dropout Voltage (Note 11)	$V_{OUT} = 2.5V$ @ 10mA		1.1	<b>1.7</b>	V
$I_{SC+}$	Short Circuit Current	$T_A = +25^\circ C$ , $V_{OUT}$ tied to GND		55		mA
$I_{SC-}$	Short Circuit Current	$T_A = +25^\circ C$ , $V_{OUT}$ tied to $V_{IN}$		-61		mA
$t_R$	Turn-on Settling Time	90% of final value, $C_L = 1.0\mu F$ , $C_C =$ open		150		$\mu$ s
	Ripple Rejection	$f = 120Hz$		90		dB
$e_N$	Output Voltage Noise	0.1Hz $\leq f \leq$ 10Hz, $V_{OUT} = 2.5V$		1.9		$\mu V_{P-P}$
$V_N$	Broadband Voltage Noise	10Hz $\leq f \leq$ 1kHz, $V_{OUT} = 2.5V$		1.6		$\mu V_{RMS}$
	Noise Density	$f = 1kHz$ , $V_{OUT} = 2.5V$		50		nV/ $\sqrt{Hz}$
$\Delta V_{OUT} / \Delta t$	Long Term Drift	$T_A = +125^\circ C$ , 1000Hrs		15		ppm

### NOTES:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in  $V_{OUT}$  is divided by the temperature range; in this case, = 180°C. (i.e., -55°C to +125°C).
- Dropout Voltage is the minimum  $V_{IN} - V_{OUT}$  differential voltage measured at the point where  $V_{OUT}$  drops 1mV from  $V_{IN} =$  nominal at  $T_A = +25^\circ C$ .

## Typical Performance Curves $V_{IN} = 5V, V_{OUT} = 2.5V, T_A = +25^\circ C$ , unless otherwise specified.

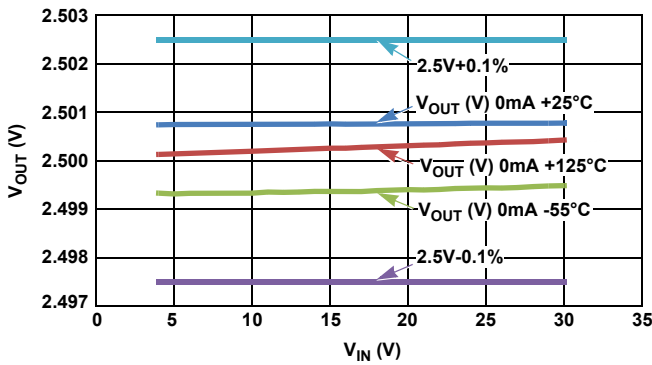


FIGURE 3.  $V_{OUT}$  ACCURACY OVER TEMPERATURE

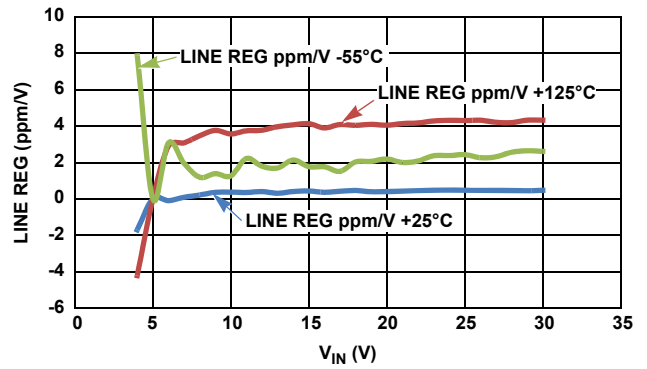


FIGURE 4. LINE REGULATION OVER TEMPERATURE (0mA)

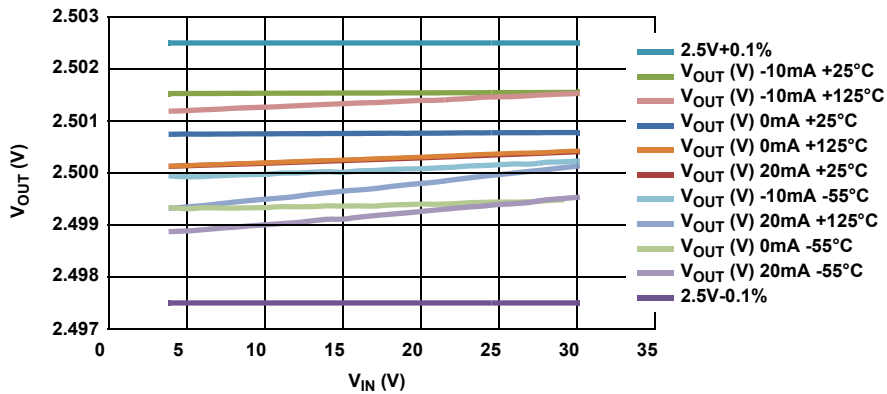


FIGURE 5.  $V_{OUT}$  vs  $V_{IN}$  AT 0mA, 20mA AND -10mA

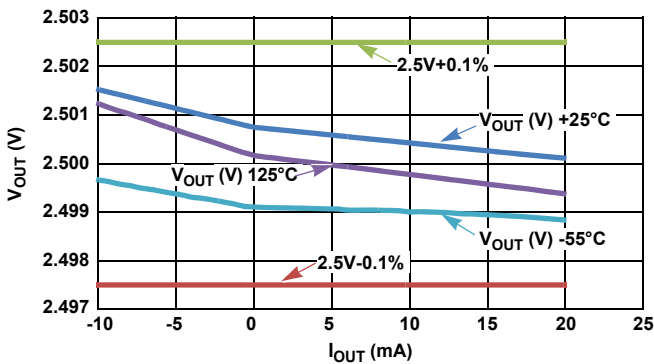


FIGURE 6. LOAD REGULATION OVER TEMPERATURE AT  $V_{IN} = 5V$

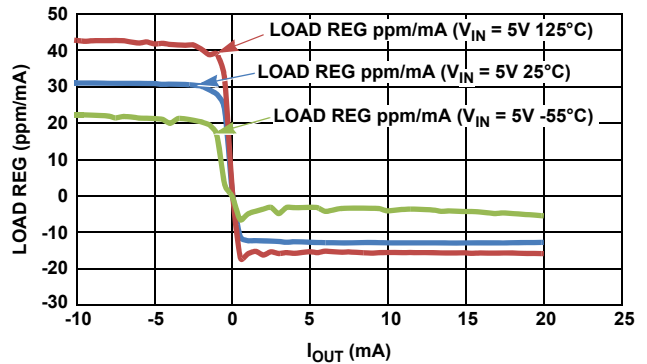


FIGURE 7. LOAD REGULATION OVER TEMPERATURE AT  $V_{IN} = 5V$  (ppm/mA)

## Typical Performance Curves $V_{IN} = 5V$ , $V_{OUT} = 2.5V$ , $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

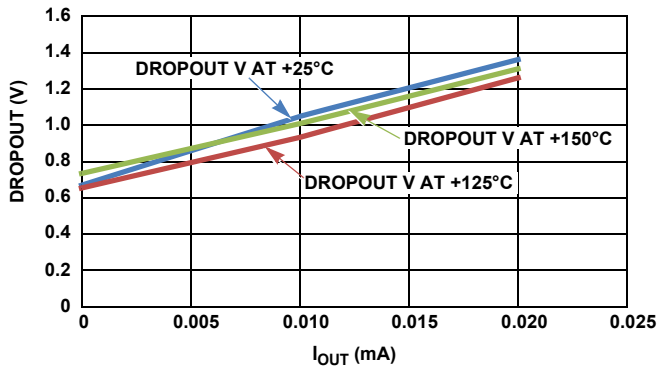


FIGURE 8. DROPOUT VOLTAGE FOR 2.5V

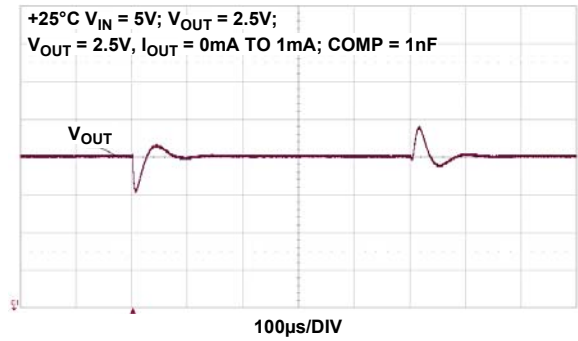


FIGURE 9. LOAD TRANSIENT (0mA TO 1mA)

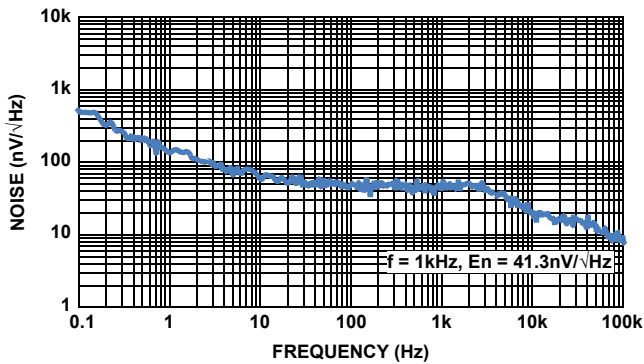


FIGURE 10. NOISE DENSITY vs FREQUENCY ( $V_{IN} = 5V$ ,  $I_{OUT} = 0mA$ )

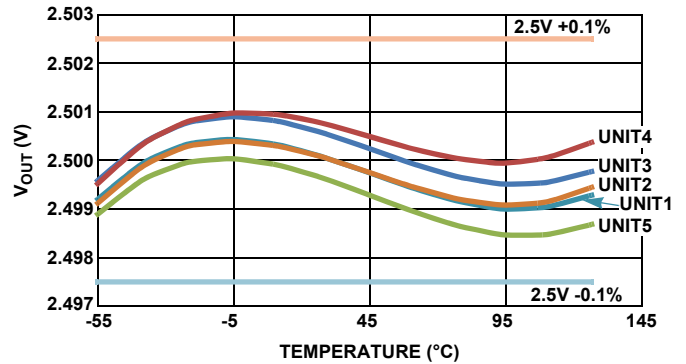


FIGURE 11. TYPICAL TEMPERATURE COEFFICIENT PLOT FOR 5 UNITS

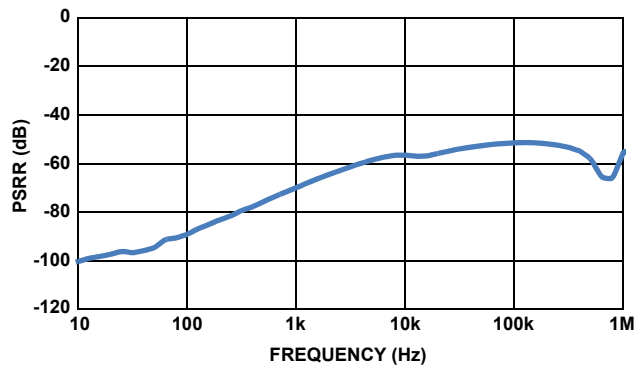


FIGURE 12. PSRR ( $+25^\circ C$ ,  $V_{IN} = 5V$ ,  $V_{OUT} = 2.5V$ ,  $I_{OUT} = 0mA$ ,  $C_{IN} = C_{OUT} = 0.1\mu F$ ,  $COMP = 1nF$ ,  $VSIG = 300mV_{p-p}$ )

## Device Operation

### Bandgap Precision Reference

The ISL71090SEH25 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

## Applications Information

### Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the printed circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

### Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of typically 100 $\mu$ V can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

### Noise Performance and Reduction

The output noise voltage over the 0.1Hz to 10Hz bandwidth is typically 2 $\mu$ V<sub>P-P</sub> ( $V_{OUT} = 2.5V$ ). The noise measurement is made with a 9.9Hz bandpass filter. Noise in the 10Hz to 1kHz bandwidth is approximately 1.6 $\mu$ V<sub>RMS</sub> ( $V_{OUT} = 2.5V$ ), with 0.1 $\mu$ F capacitance on the output. This noise measurement is made with a band pass filter of 990Hz. Load capacitance up to 10 $\mu$ F (with COMP) can be added but will result in only marginal improvements in output noise and transient response.

### Turn-On Time

Normal turn-on time is typically 150 $\mu$ s, the circuit designer must take this into account when looking at power-up delays or sequencing.

### Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures which provide for the maximum voltage deviation and take the total variation, ( $V_{HIGH} - V_{LOW}$ ), this is then divided by the temperature extremes of measurement ( $T_{HIGH} - T_{LOW}$ ). The result is divided by the nominal reference voltage (at  $T = +25^{\circ}C$ ) and multiplied by  $10^6$  to yield ppm/ $^{\circ}C$ . This is the "Box" method for specifying temperature coefficient.

## Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The positive input of the amplifier is about 1.216V, and in feedback, so will be the trim voltage. The suggested method to adjust the output is to connect a 1M $\Omega$  external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100k $\Omega$  resistance and whose outer terminals connect to  $V_{OUT}$  and ground. If a 1M $\Omega$  resistor is connected to trim, the output adjust range will be  $\pm 6.3mV$ . The TRIM pin should not have any capacitor tied to its output, also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

## Output Stage

The output stage of the device has a push pull configuration with an high side PNP and a low side NPN. This helps the device to act as a source and sink. The device can source 20mA and sink 10mA.

## Use of COMP Cap

The reference can be compensated for the  $C_{OUT}$  capacitors used by adding a capacitor from COMP pin to GND. See Table 1 for recommended values. of the COMP capacitor.

TABLE 1.

$C_{OUT}$ ( $\mu$ F)	$C_{COMP}$ (nF)
0.1	1
1	1
10	10

## SEE Testing

The device was tested under ion beam at an LET of 86MeV  $\cdot$  cm<sup>2</sup>/mg. The device did not latch up or burn out to a VDD of 36V and at +125 $^{\circ}C$ . Single Event transients were observed and are summarized in the Table 2:

TABLE 2.

$V_{IN}$ (V)	$I_{OUT}$ (A)	$C_{OUT}$ ( $\mu$ F)	SET (% $V_{OUT}$ )
4	5	1	-4.6
30	5	1	-4.4
30	5	10	-1.0

## DNC Pins

These pins are for trimming purpose and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

# ISL71090SEH25

## Package Characteristics

### Weight of Packaged Device

0.31 Grams (Typical)

### Lid Characteristics

Finish: Gold

Potential: Connected to pin #4 (GND)

Case Isolation to Any Lead:  $20 \times 10^9 \Omega$  (min)

## Die Characteristics

### Die Dimensions

$1464\mu\text{m} \times 1744\mu\text{m}$  (58mils  $\times$  69mils)

Thickness:  $483\mu\text{m} \pm 25\mu\text{m}$  (19mils  $\pm$  1 mil)

### Interface Materials

#### GLASSIVATION

Type: Nitrox

Thickness:  $15\text{k}\text{\AA}$

### TOP METALLIZATION

Type: AlCu (99.5%/0.5%)

Thickness:  $30\text{k}\text{\AA}$

### BACKSIDE FINISH

Silicon

## ASSEMBLY RELATED INFORMATION

### SUBSTRATE POTENTIAL

Floating

## ADDITIONAL INFORMATION

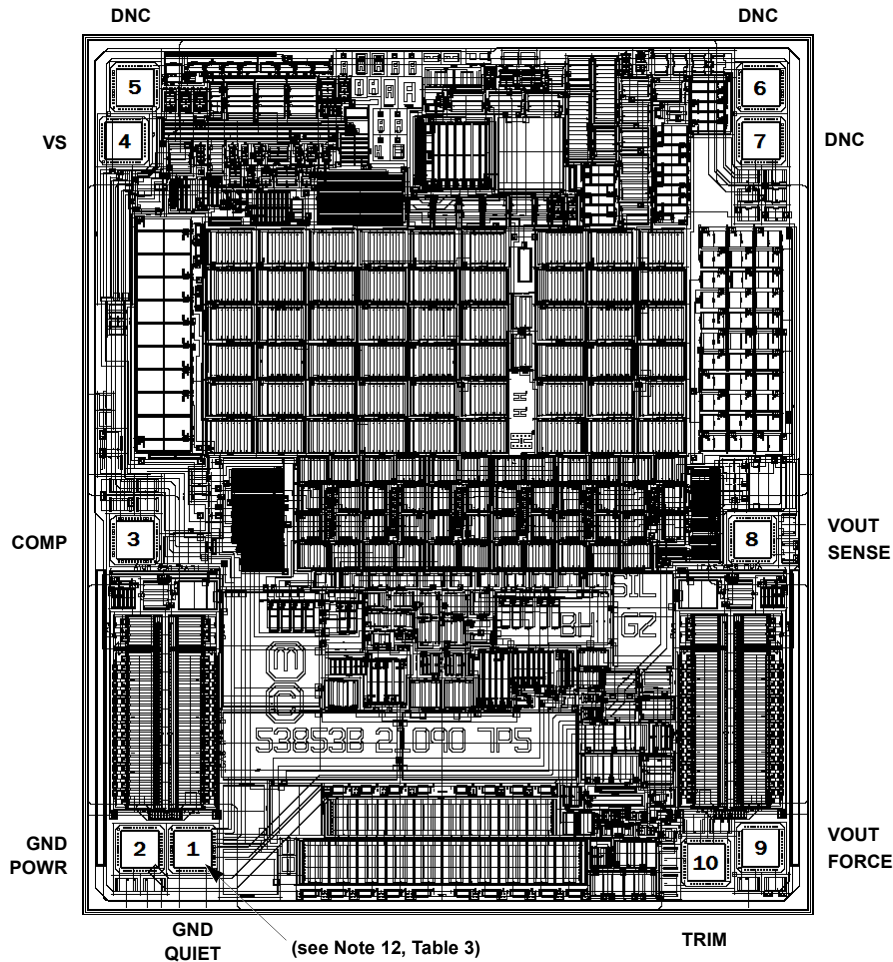
### WORST CASE CURRENT DENSITY

$< 2 \times 10^5 \text{ A/cm}^2$

### PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40

## Metallization Mask Layout





# ISL71090SEH25

TABLE 3. DIE LAYOUT X-Y COORDINATES

PAD NAME	PIN NUMBER	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	BOND WIRES PER PAD
GND PWR	4	-104	0	1
GND QUIET	4	0	0	1
COMP	3	-108	589	1
VS	2	-125	1350	1
DNC	1	-108	1452	1
DNC	8	1089	1452	1
DNC	7	1089	1350	1
VOUT SENSE	6	1072	598	1
VOUT FORCE	6	1088	1	1
TRIM	5	985	-25	1

NOTES:

- Origin of coordinates is the centroid of GND QUIET.
- Bond wire size is 1 mill.

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 6, 2013	FN8451.0	Initial Release.

## About Intersil

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For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com). You may report errors or suggestions for improving this datasheet by visiting [www.intersil.com/en/support/ask-an-expert.html](http://www.intersil.com/en/support/ask-an-expert.html). Reliability reports are also available from our website at <http://www.intersil.com/en/support/qualandreliability.html#reliability>

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