

HAT2137H

Silicon N Channel Power MOS FET
Power Switching

HITACHI

ADE-208-1579B (Z)

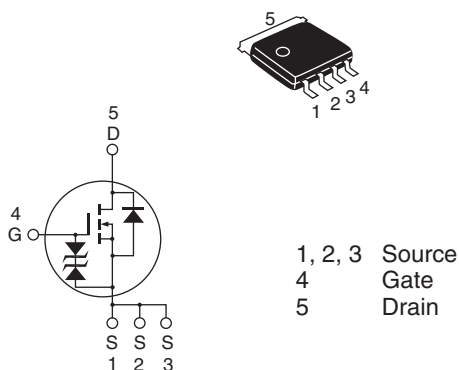
Preliminary
3rd. Edition
Dec. 2002

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 3.8 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

LFPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	40	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	45	A
Drain peak current	I _{D(pulse)} ^{Note1}	180	A
Body-drain diode reverse drain current	I _{DR}	45	A
Avalanche current	I _{AP} ^{Note 3}	30	A
Avalanche energy	E _{AR} ^{Note 3}	72	mJ
Channel dissipation	P _{ch} ^{Note2}	30	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	–55 to + 150	°C

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Tc = 25°C
3. Value at Tch = 25°C, Rg $\geq 50 \Omega$

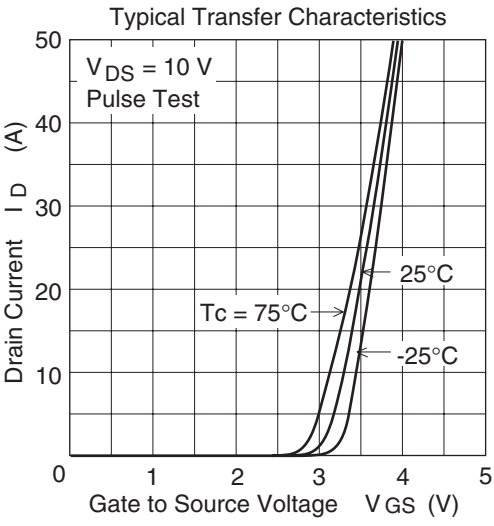
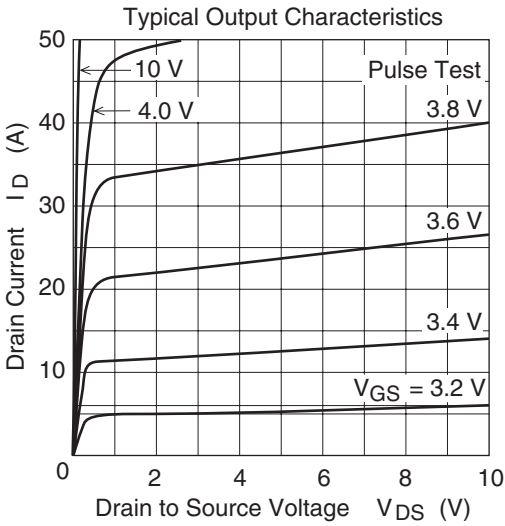
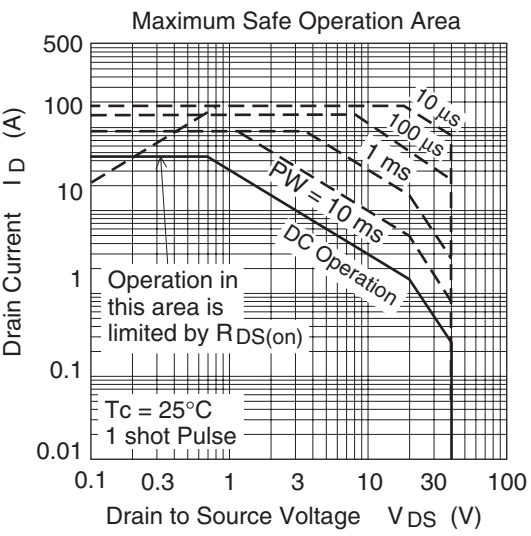
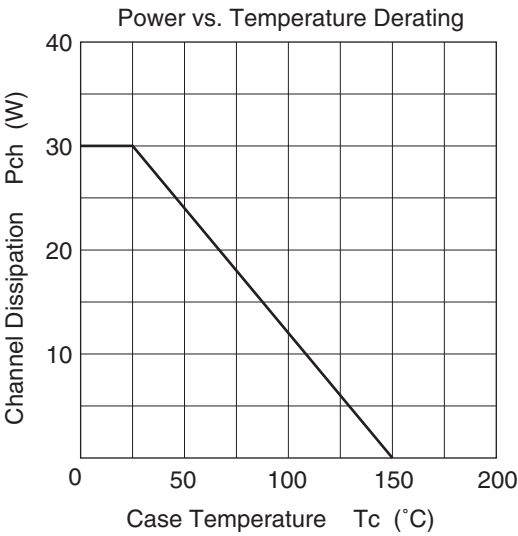
Electrical Characteristics

(Ta = 25°C)

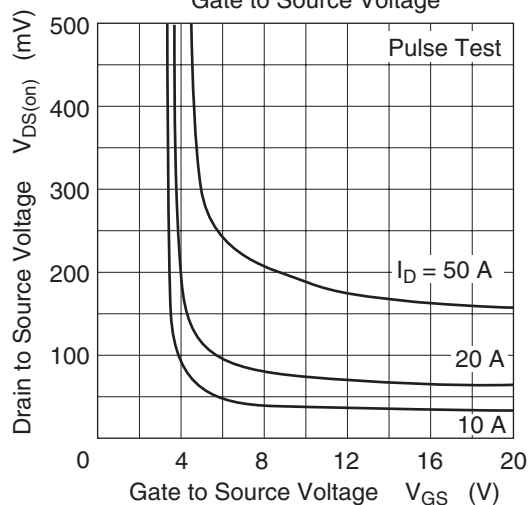
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.8	4.8	m Ω	$I_D = 22.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	4.4	6.0	m Ω	$I_D = 22.5 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	38	64	—	S	$I_D = 22.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	6200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	780	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	410	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	95	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	24	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	14	—	nc	$I_D = 45 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	27	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 22.5 \text{ A}$
Rise time	t_r	—	50	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	$R_L = 0.44 \text{ }\Omega$
Fall time	t_f	—	14	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 45 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 45 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 3. Pulse test

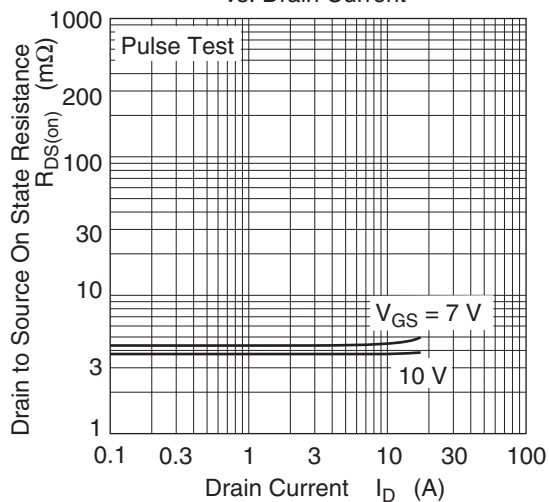
Main Characteristics



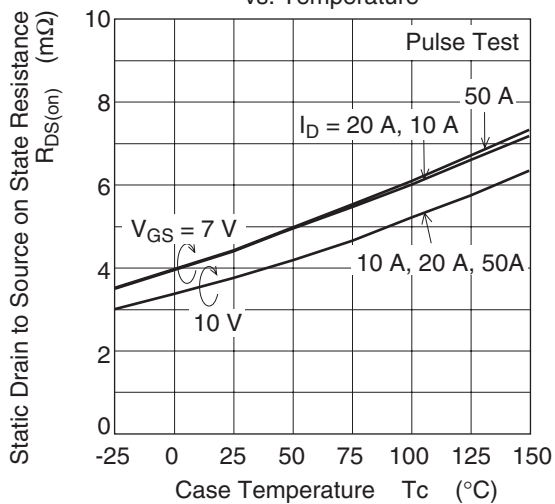
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



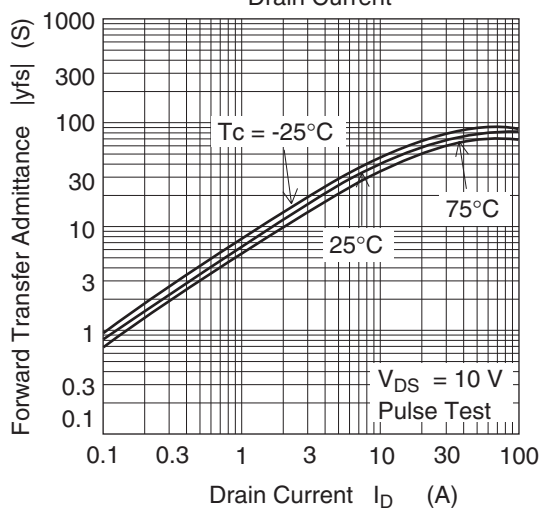
Static Drain to Source on State Resistance
vs. Drain Current

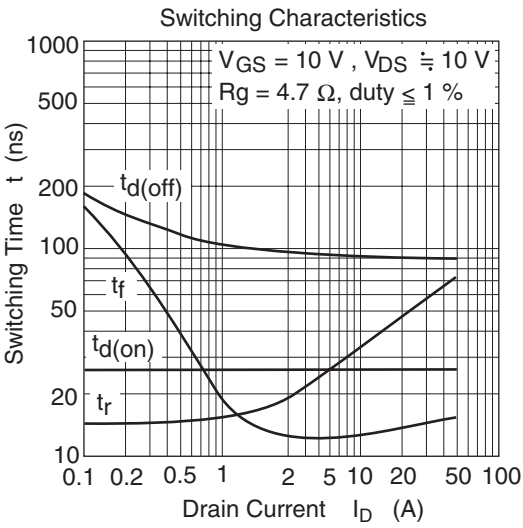
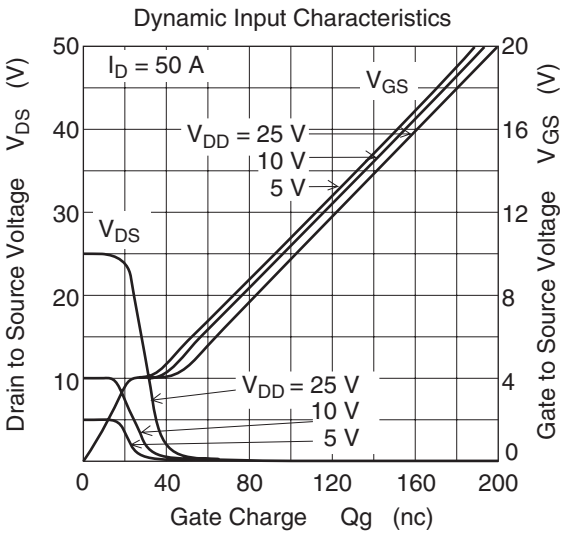
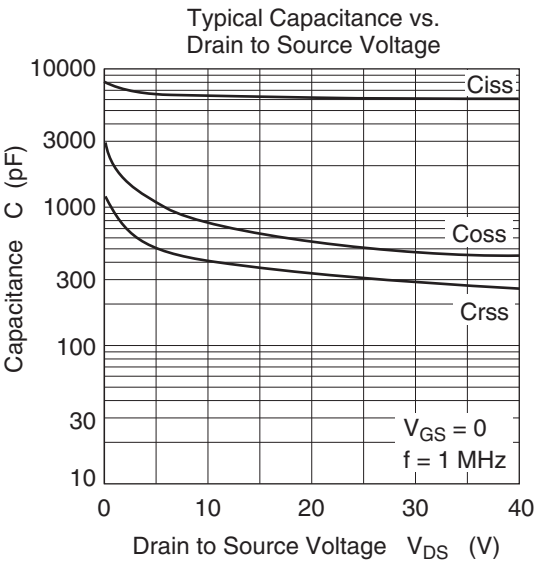
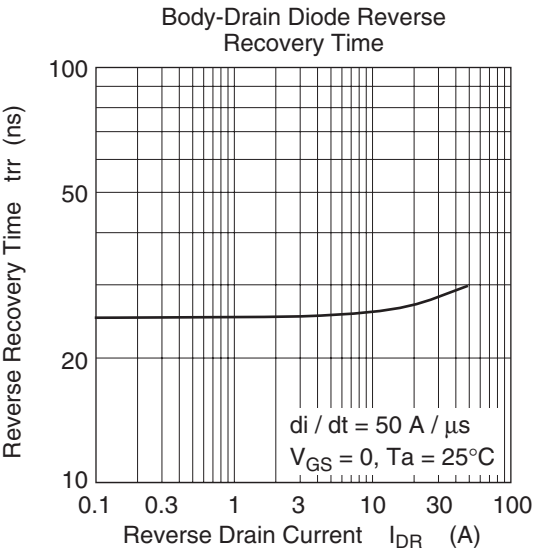


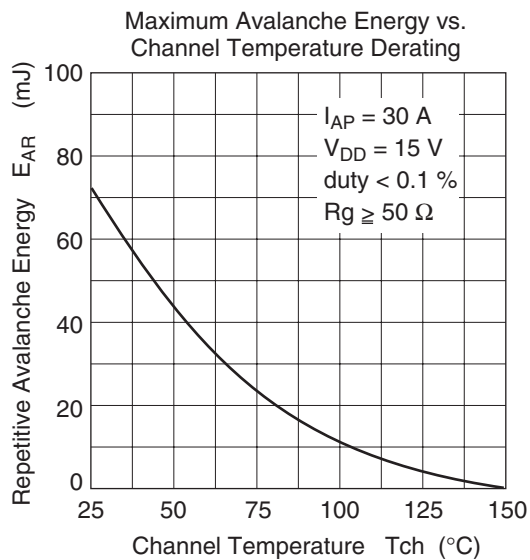
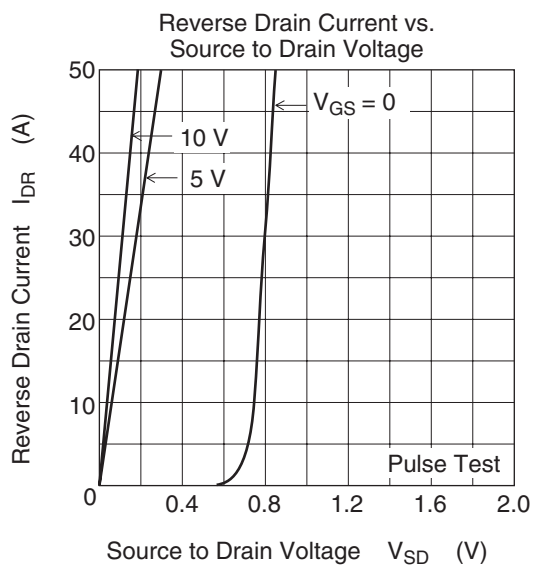
Static Drain to Source on State Resistance
vs. Temperature



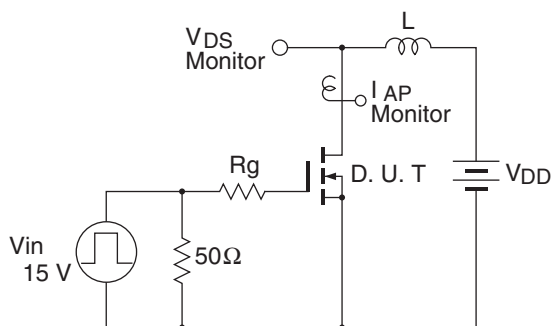
Forward Transfer Admittance vs.
Drain Current





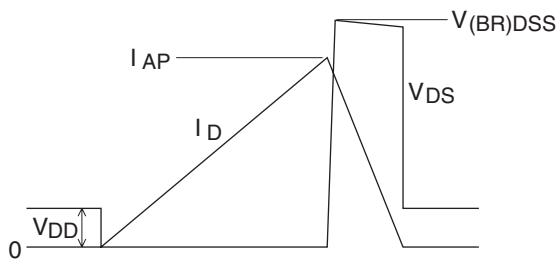


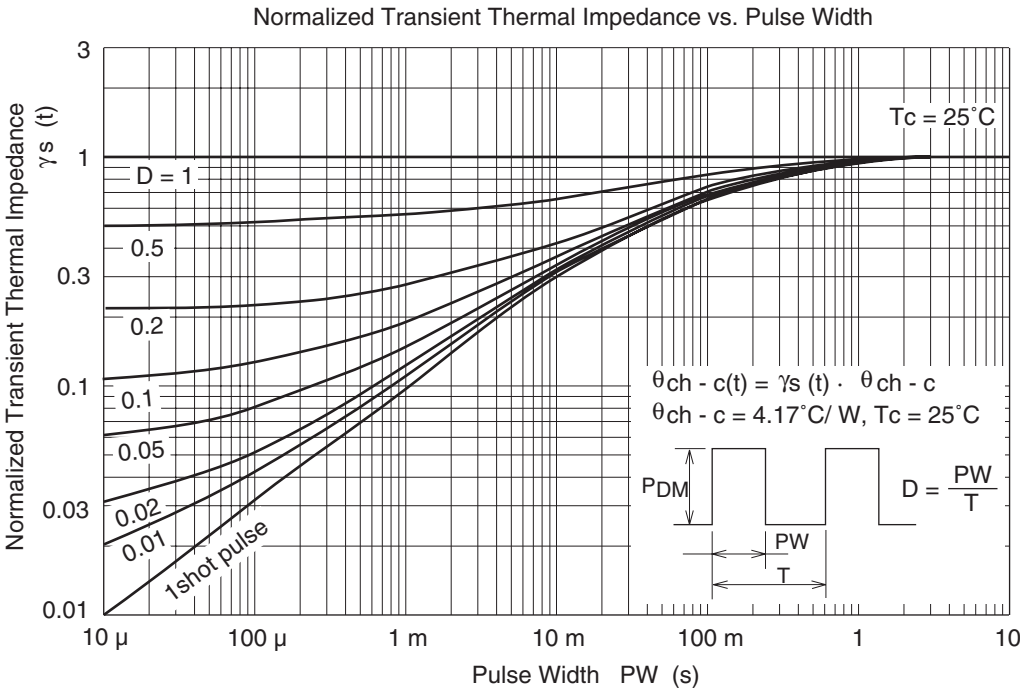
Avalanche Test Circuit



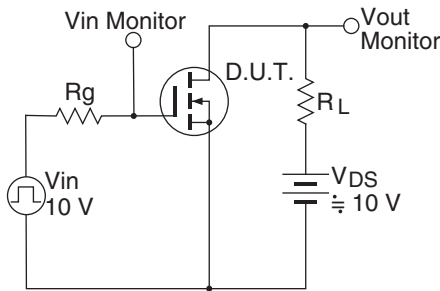
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

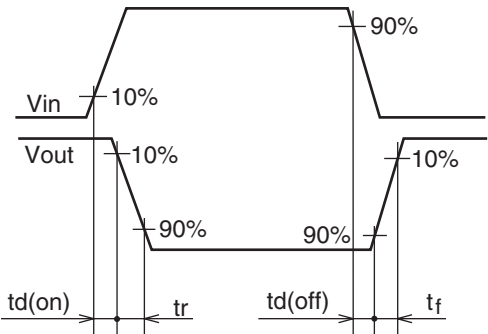




Switching Time Test Circuit

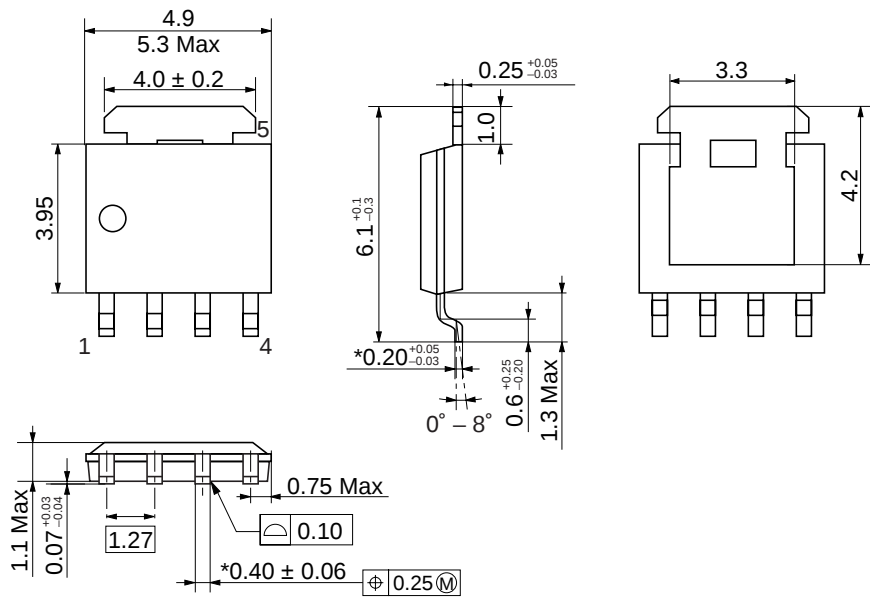
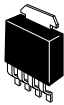


Switching Time Waveform



Package Dimensions

As of July, 2002
Unit: mm



*Ni/Pd/Au plating

Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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