512K × 36-Bit Dynamic RAM Module — HYM 365120S-80

Advanced Information

- 524 288 words by 36-bit organization
- Fast access and cycle time
  80 ns access time
  150 ns cycle time
- Fast page mode capability with
  55 ns cycle time
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4400 mW active
  CMOS – 200 mW standby
  TTL – 330 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh,
  $\overline{RAS}$-only refresh, hidden refresh,
  page mode capability
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 25.4 mm high single in-Line Memory Module (L-SIM-72-1000)
- Utilizes sixteen 256K × 4 DRAMs in SOJ and eight 256K × 1 DRAMs in PL-CC-packages
- 512 refresh cycles/8 ms

The HYM 365120S-80 is a 18 Mbit RAM module organized as 524 288 words by 36-bit in a 72-pin single in-line package comprising sixteen HYB 514256AJ 256K × 4 DRAMs and eight 256K × 1 DRAMs in PL-CC-packages mounted together with twelve 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

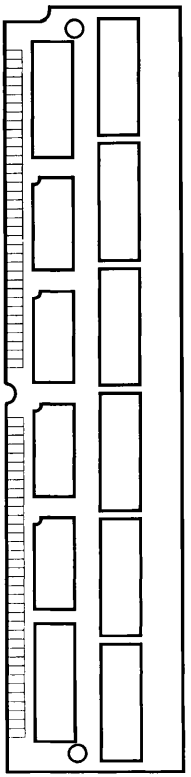
Each DRAM is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

Ordering Information

Type	Ordering Code	Package	Description
HYM 365120S-80	Q67100-Q549	L-SIM-72-1000-D	DRAM Module (access time 80 ns)

Pin Configuration

V_{SS}	1	DQ0	2
DQ18	3	DQ1	4
DQ19	5	DQ2	6
DQ20	7	DQ3	8
DQ21	9	V_{CC}	10
N.C.	11	A0	12
A1	13	A2	14
A3	15	A4	16
A5	17	A6	18
N.C.	19	DQ4	20
DQ22	21	DQ5	22
DQ23	23	DQ6	24
DQ24	25	DQ7	26
DQ25	27	A7	28
N.C.	29	V_{CC}	30
A8	31	N.C.	32
N.C.	33	$\overline{RAS2}$	34
DQ26	35	DQ8	36
DQ17	37	DQ35	38
V_{SS}	39	$\overline{CAS0}$	40
$\overline{CAS2}$	41	$\overline{CAS3}$	42
$\overline{CAS1}$	43	$\overline{RAS0}$	44
N.C.	45	N.C.	46
$\overline{WRITE}$	47	N.C.	48
DQ9	49	DQ27	50
DQ10	51	DQ28	52
DQ11	53	DQ29	54
DQ12	55	DQ30	56
DQ13	57	DQ31	58
V_{CC}	59	DQ32	60
DQ14	61	DQ33	62
DQ15	63	DQ34	64
DQ16	65	N.C.	66
V_{SS}	67	N.C.	68
N.C.	69	V_{SS}	70
N.C.	71	V_{SS}	72



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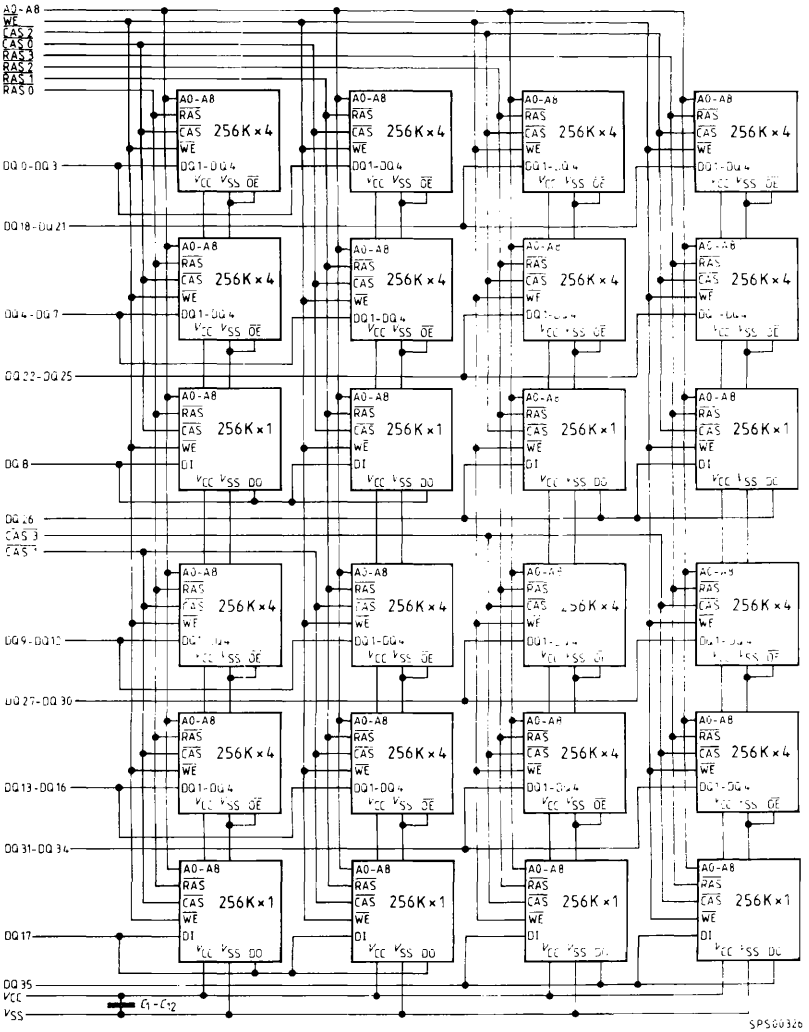
Pin Names

A0-A8	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$-$\overline{CAS2}$	Column Address Strobe
$\overline{RAS0}$-$\overline{RAS2}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power supply (+ 5 V)
V_{SS}	Ground (0 V)
N. C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/Output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation.....11.2 W
Data out current (short circuit) .....50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = 5 V± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 20	20	µA	–
I_{CC1}	Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	60	mA	1)
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC4}	Average V_{CC} supply current during fast page mode: ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	–	560	mA	1) 2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	36	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	–	800	mA	1)

Notes see page 203.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{RC}	Random read or write cycle time	150	–	ns
t_{PC}	Fast page mode cycle time	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	ns
t_{AA}	Access time from column address [6) 12)]	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	ns
t_T	Transition time (rise and fall) [5)]	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	16000	ns
t_{RSH}	$\overline{RAS}$ hold time	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	25	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	25	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	20	40	ns
t_{CRP}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	15	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	15	–	ns
t_{ASR}	Row address setup time	0	–	ns
t_{RAH}	Row address hold time	15	–	ns
t_{ASC}	Column address setup time	0	–	ns
t_{CAH}	Column address hold time	15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	65	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	ns
t_{RCS}	Read command setup time	0	–	ns

Notes see page 203.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{RCH}	Read command hold time [8]	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	ns
t_{WCH}	Write command hold time	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65	–	ns
t_{WP}	Write command pulse width	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	25	–	ns
t_{DS}	Data setup time [9]	0	–	ns
t_{DH}	Data hold time [9]	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	65	–	ns
t_{REF}	Refresh period	–	8	ms
t_{WCS}	Write command setup time [10]	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	15	–	ns

Notes see page 203.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %, f = 1 MHz

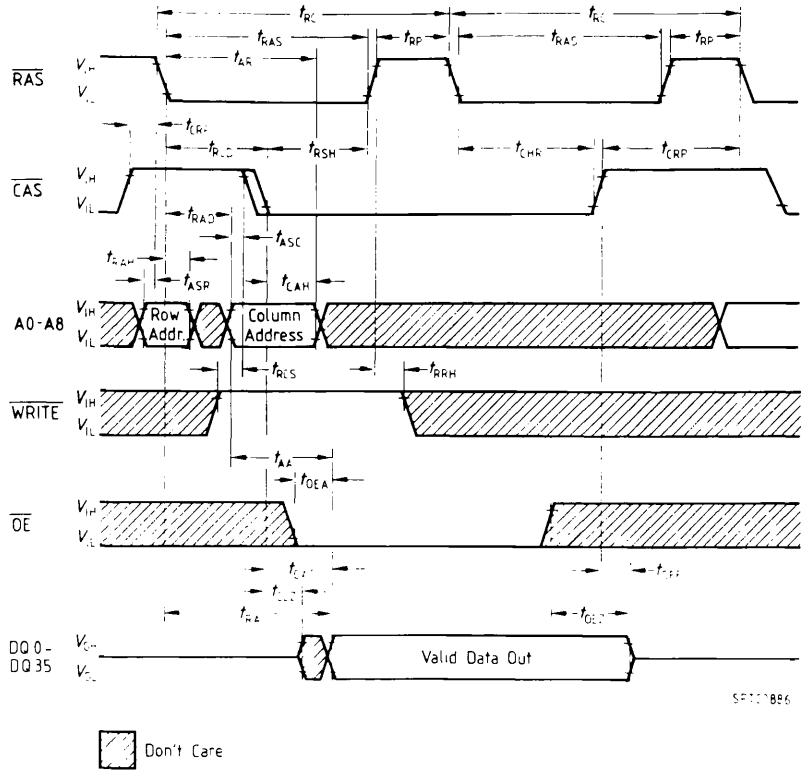
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A8, $\overline{WE}$)	–	160	pF
C_{I2}	Input capacitance ($\overline{RAS0}$-$\overline{RAS3}$, $\overline{CAS0}$-$\overline{CAS3}$)	–	40	pF
C_{IO}	I/O capacitance (DQ0-DQ35)	–	25	pF

Notes for pages 200 to 202

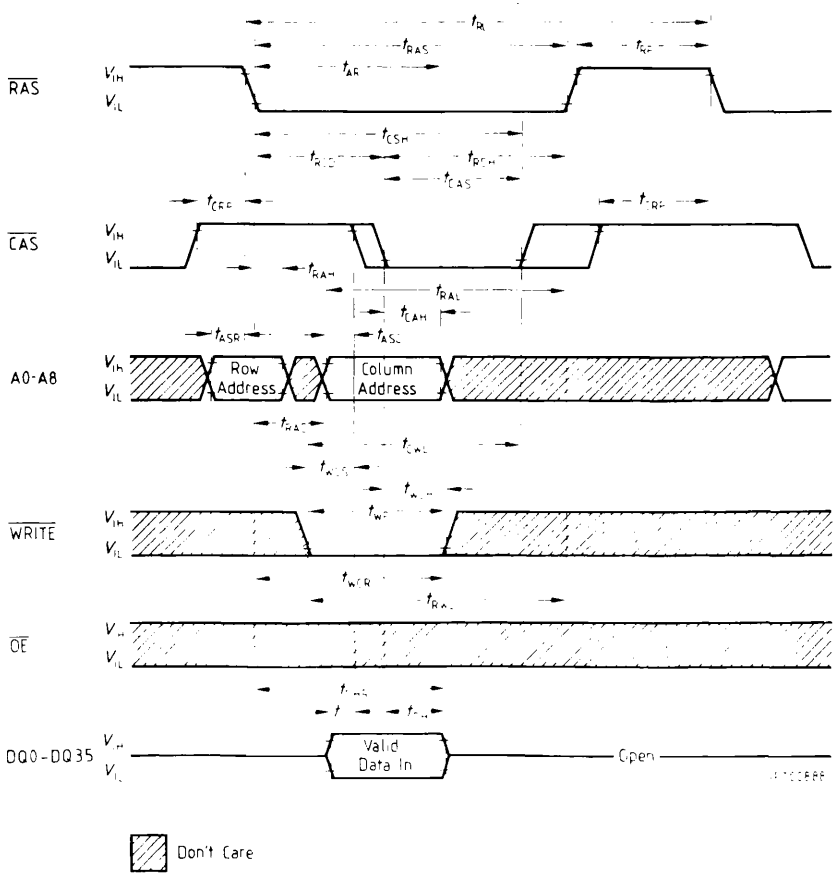
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

Waveforms

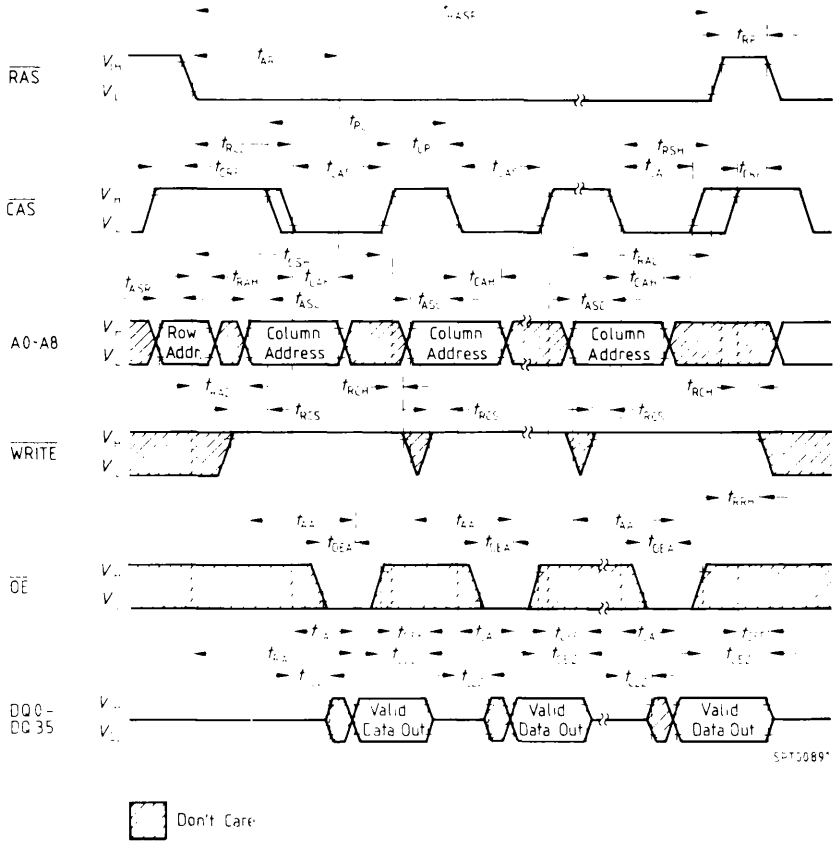
Read Cycle



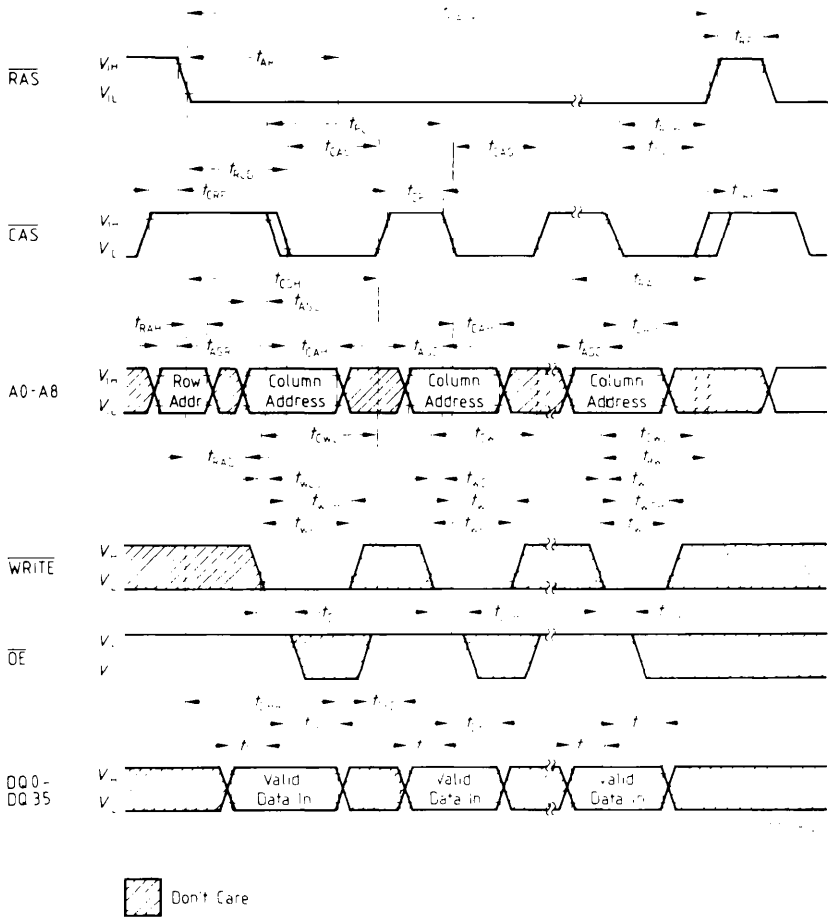
Write Cycle (early write)



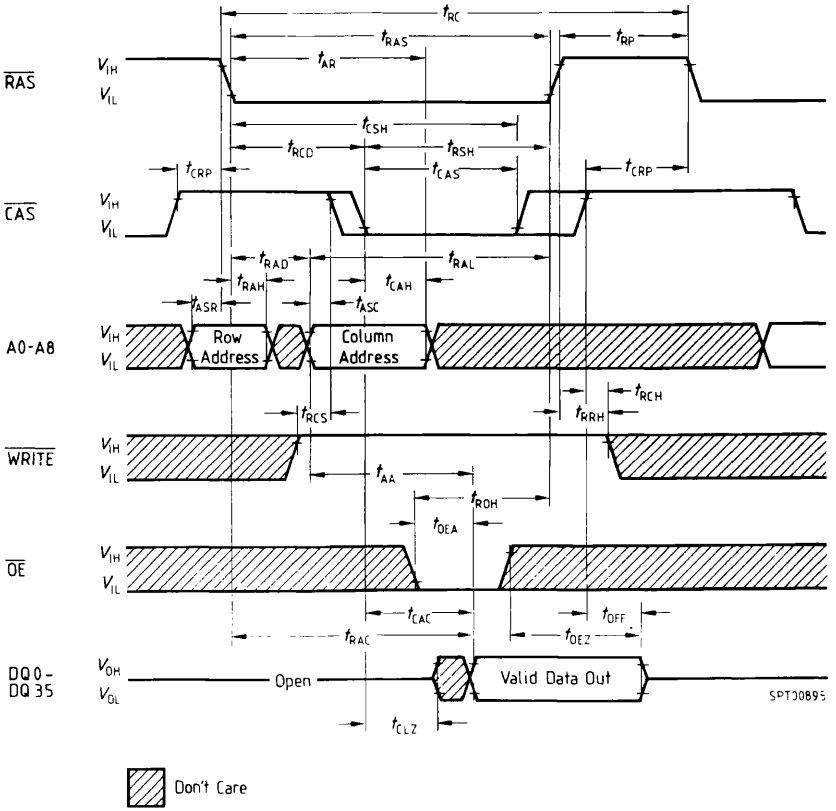
Fast Page Mode Read Cycle



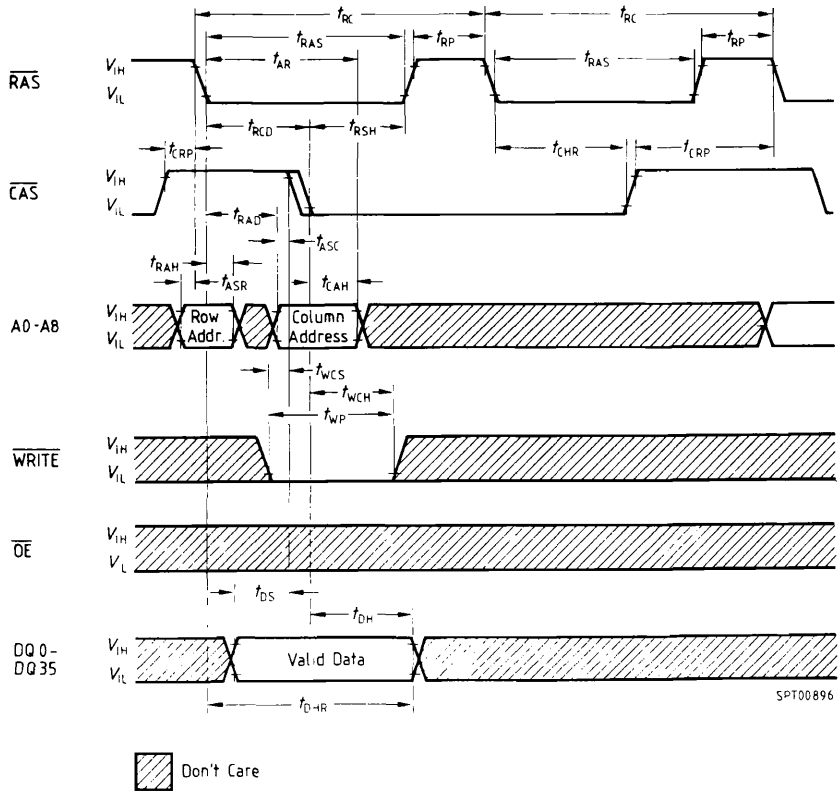
Fast Page Mode Write Cycle



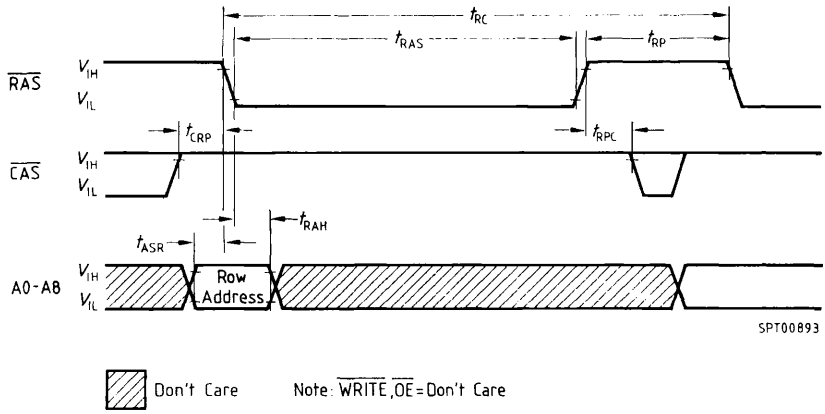
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)



$\overline{\text{RAS}}$-Only Refresh Cycle



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle