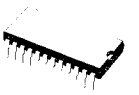
HCC/HCF4508B

DUAL 4-BIT LATCH

- TWO INDIPENDENT 4-BIT LATCHES
- INDIVIDUAL MASTER RESET FOR EACH 4-BIT-LATCH
- 3-STATE OUTPUTS WITH HIGH-IMPEDANCE STATE FOR BUS LINE APPLICATION
- MEDIUM-SPEED OPERATION : $t_{PHL} = t_{PLH} =$ 70ns (TYP.) AT $V_{DD} = 10V$ AND $C_L = 50pF$
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



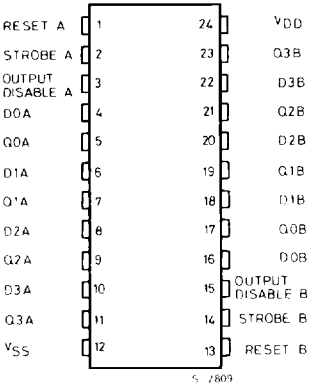
BEY
(Plastic Package)

BF
(Ceramic Frit Seal Package)

BM1
(Micro Package)

ORDER CODES :
HCC4508BF HCF4508BEY
HCF4508BM1

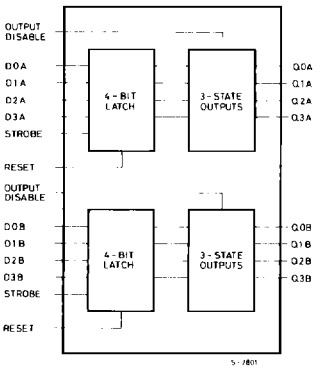
PIN CONNECTIONS



DESCRIPTION

The **HCC4508B** (extended temperature range) and the **HCF4508B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4508B** dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	− 0.5 to + 20 − 0.5 to + 18	V V
V_i	Input Voltage	− 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C
T_{stg}	Storage Temperature	− 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings "may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

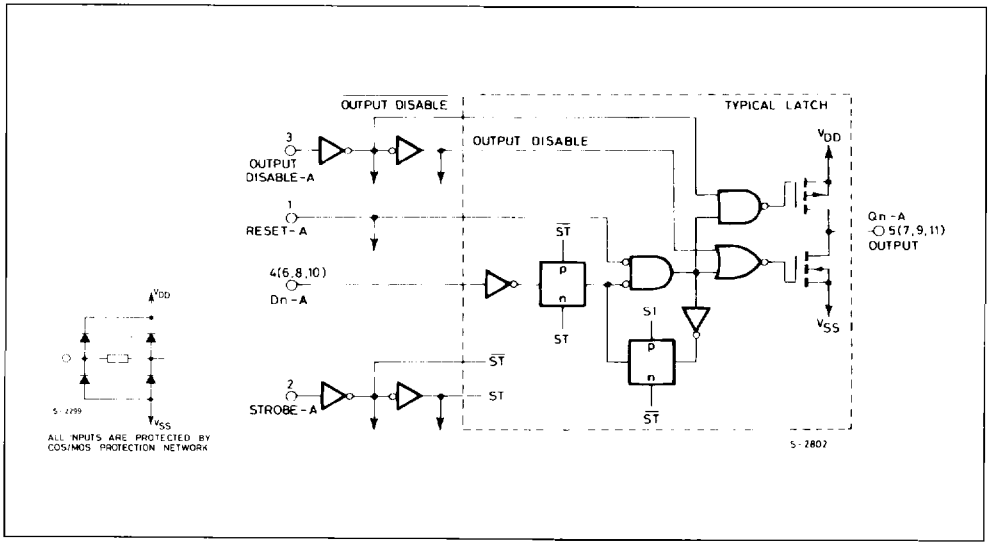
* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to + 18 3 to + 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C

LOGIC DIAGRAM (A section)

1 OF 4 IDENTICAL LATCHES WITH COMMON OUTPUT DISABLE, RESET AND STROBE



TRUTH TABLE

Reset	Disab.	Strobe	D Input	Q Input
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

1 = High level
0 = Low level

X = Don't care
Z = High impedance

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Value T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	− 2		− 1.6	− 3.2		− 1.15		mA
			0/ 5	4.6		5	− 0.64		− 0.51	− 1		− 0.36		
			0/10	9.5		10	− 1.6		− 1.3	− 2.6		− 0.9		
			0/15	13.5		15	− 4.2		− 3.4	− 6.8		− 2.4		
		HCF Types	0/ 5	2.5		5	− 1.53		− 1.36	− 3.2		− 1.1		
			0/ 5	4.6		5	− 0.52		− 0.44	− 1		− 0.36		
			0/10	9.5		10	− 1.3		− 1.1	− 2.6		− 0.9		
			0/15	13.5		15	− 3.6		− 3.0	− 6.8		− 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
I_O	3-state Output	HCC Types	0/18			18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μA
		HCF Types	0/15			15		± 1.0		$\pm 10^{-4}$	± 1.0		± 7.5	
C_I	Input Capacitance			Any Input						5	7.5			pF

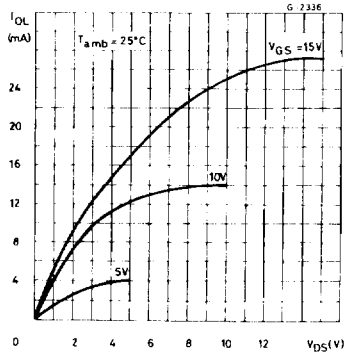
* T_{Low} = − 55°C for **HCC** device : − 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5 V min. with V_{DD} = 15V.

DYNAMIC ELECTRICAL CHARACTERISTICS

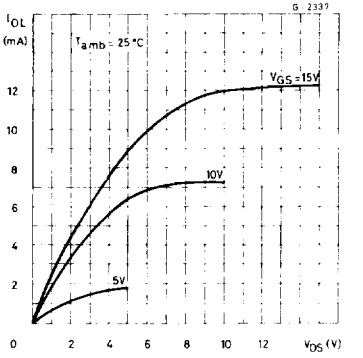
(T_{amb} = 25°C, input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ, unless otherwise specified)

Symbol	Parameter		Test Conditions V_{DD} (V)	Value Min.	Value Typ.	Value Max.	Unit
t_{THL}, t_{TLH}	Transition Time		5		100	200	
			10		50	100	ns
			15		40	80	
$t_{W(R)}$	Reset Pulse Width		5	200	100		
			10	140	70		ns
			15	100	50		
$t_{W(st)}$	Strobe Pulse Width		5	140	70		
			10	80	40		ns
			15	70	35		
t_{setup}	Setup Time		5	50	25		
			10	30	15		ns
			15	20	10		
t_H	Hold Time		5	0	0		
			10	0	0		ns
			15	0	0		
t_{PHL}, t_{PLH}	Propagation Delay Time:	Strobe to Data Out	5		130	260	
			10		70	140	ns
			15		50	100	
		Data in to Data Out	5		105	210	
			10		60	120	ns
			15		45	90	
		Reset to Data Out	5		90	180	
			10		50	100	ns
			15		40	80	
t_{PHZ}	3-State Propagation Delay Time Output High to High impedance		5		90	180	
			10		50	100	ns
			15		35	70	
t_{PZH}	High Impedance to Output High		5		90	180	
			10		50	100	ns
			15		35	70	
t_{PLZ}	Output Low to High Impedance		5		90	180	
			10		50	100	ns
			15		35	70	
t_{PZL}	High Impedance to Output Low		5		90	180	
			10		50	100	ns
			15		35	70	

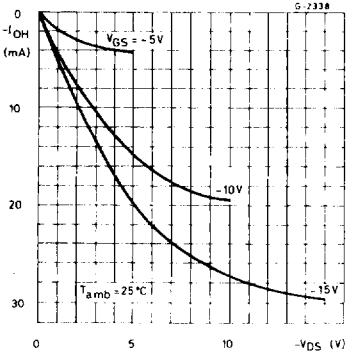
Typical Output Low (sink) Current Characteristics.



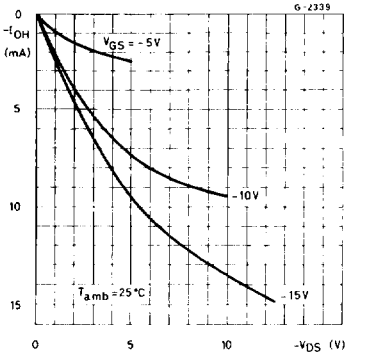
Minimum Output Low (sink) Current Characteristics.



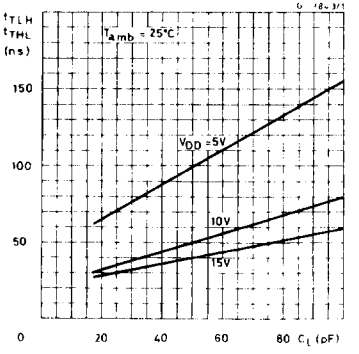
Typical Output High (source) Current Characteristics.



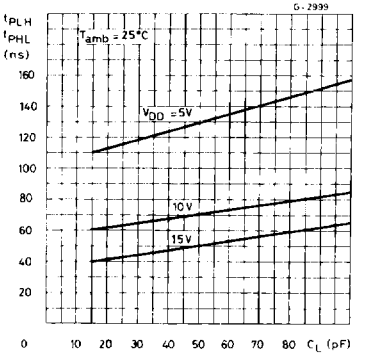
Minimum Output High (source) Current Characteristics.



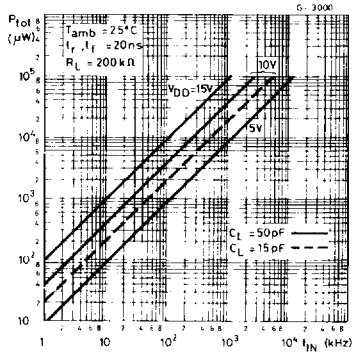
Typical Transition Time vs. Load Capacitance.



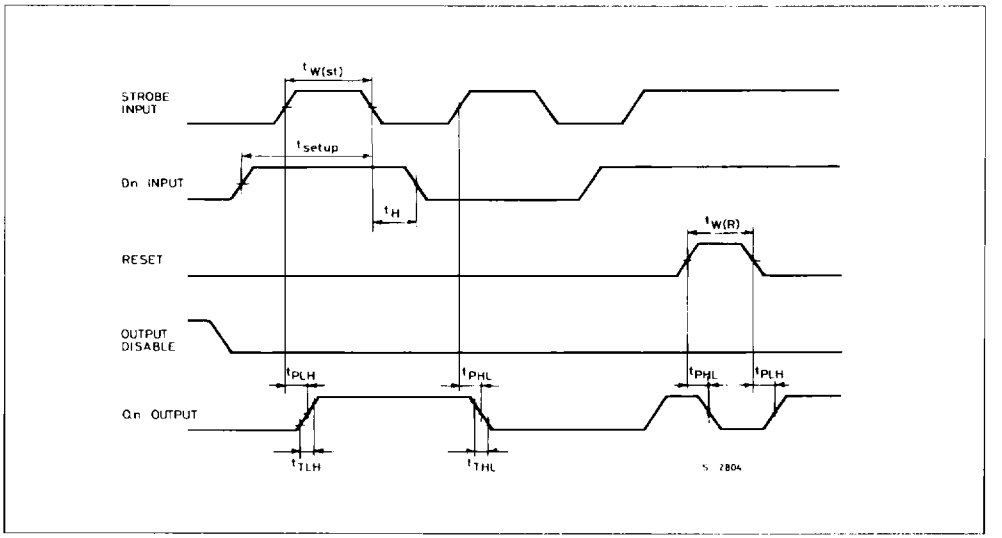
Typical Propagation Delay Time vs. Load Capacitance (strobe to dataout).



Typical Power Dissipation vs. Frequency .

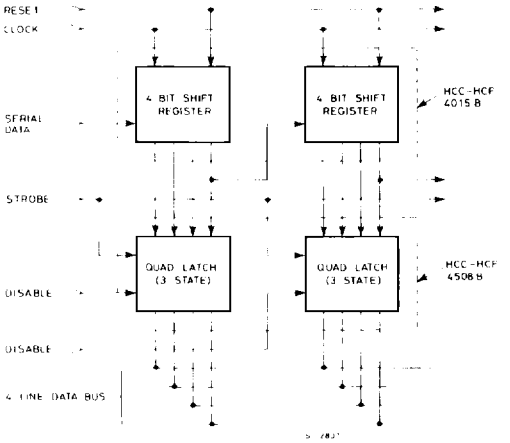


TEST WAVEFORM

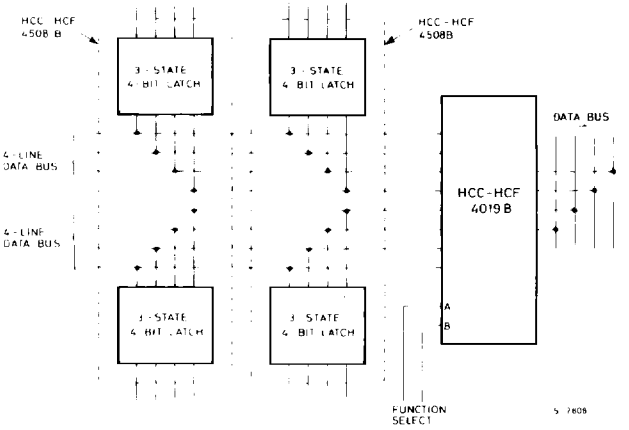


TYPICAL APPLICATIONS

A) **Figure 15** : Bus register.



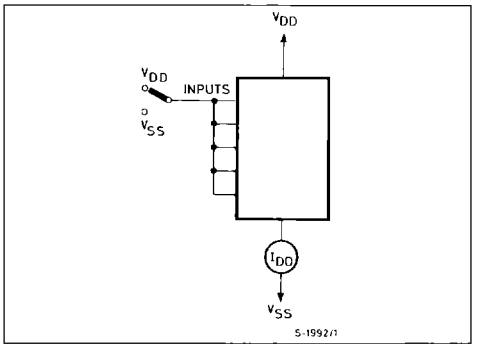
B) **Figure 16** : Dual multiplexed bus register with function select.



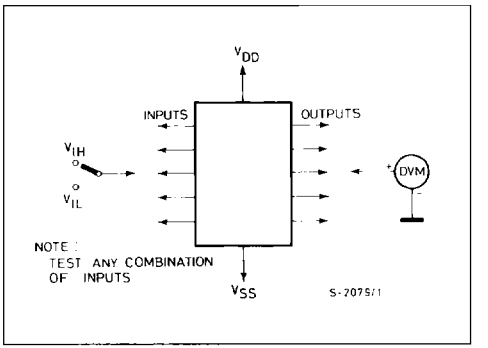
A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	A + B

TEST CIRCUITS

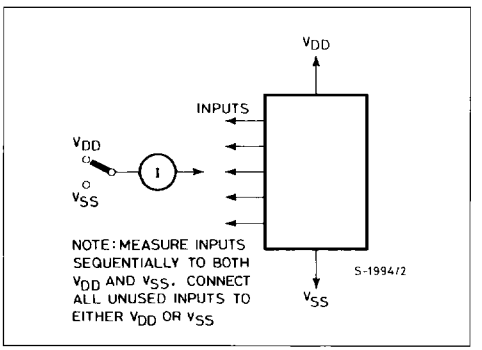
Quiescent Device Current Test Circuit.



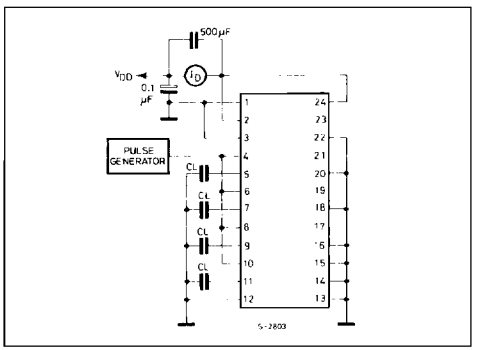
Input Voltage Test Circuit.



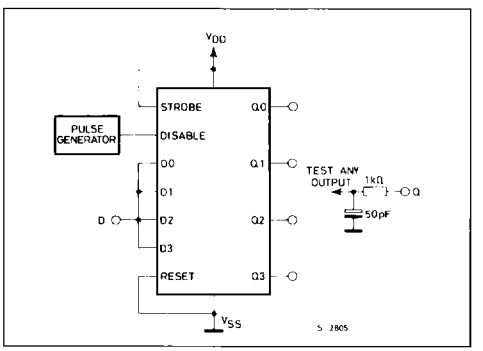
Input Current Test Circuit.



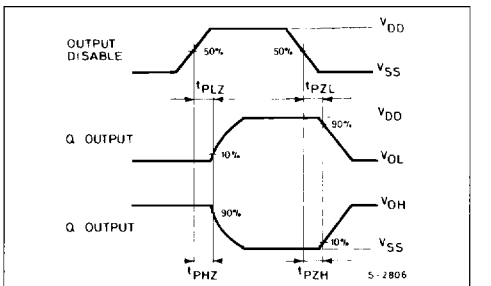
Power Dissipation Test Circuit.



Output Disable.



Waveform.



Char.	Test.	Volt.
	At D	At Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}