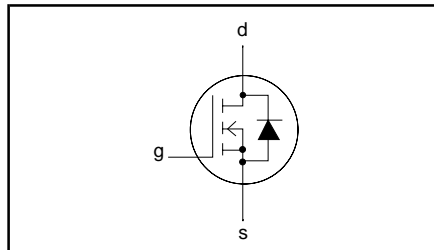# N-channel enhancement mode MOS transistor

BSH105

FEATURES

• Very low threshold voltage
• Fast switching
• Logic level compatible
• Subminiature surface mount package

SYMBOL

QUICK REFERENCE DATA

V_{DS} = 20 V

I_D = 1.05 A

$R_{DS(ON)} \leq 250$ mΩ (V_{GS} = 2.5 V)

$V_{GS(TO)} \geq 0.4$ V

GENERAL DESCRIPTION

N-channel, enhancement mode, logic level, field-effect power transistor. This device has very low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH105 is supplied in the SOT23 subminiature surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

SOT23

Top view
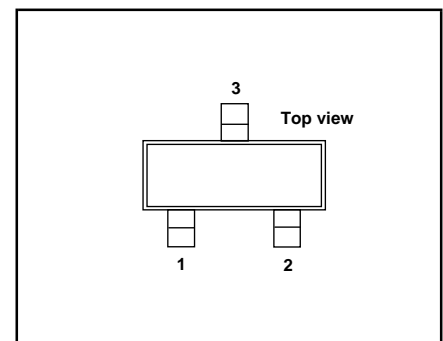
LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	20	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	20	V
V_{GS}	Gate-source voltage		-	± 8	V
I_D	Drain current (DC)	T_a = 25 ˚C	-	1.05	A
		T_a = 100 ˚C	-	0.67	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 ˚C	-	4.2	A
P_{tot}	Total power dissipation	T_a = 25 ˚C	-	0.417	W
		T_a = 100 ˚C	-	0.17	W
T_{stg}, T_j	Storage & operating temperature		- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

N-channel enhancement mode MOS transistor

BSH105

ELECTRICAL CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 10$ μA	20	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	0.4	0.57	-	V
		$T_j = 150˚C$	0.1	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 0.6$ A	-	140	200	mΩ
		$V_{GS} = 2.5$ V; $I_D = 0.6$ A	-	180	250	mΩ
		$V_{GS} = 1.8$ V; $I_D = 0.3$ A	-	240	300	mΩ
		$V_{GS} = 2.5$ V; $I_D = 0.6$ A; $T_j = 150˚C$	-	270	375	mΩ
g_{fs}	Forward transconductance	$V_{DS} = 16$ V; $I_D = 0.6$ A	0.5	1.6	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = ±8$ V; $V_{DS} = 0$ V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 16$ V; $V_{GS} = 0$ V;	-	50	100	nA
		$T_j = 150˚C$	-	1.3	10	μA
$Q_{g(tot)}$	Total gate charge	$I_D = 1$ A; $V_{DD} = 20$ V; $V_{GS} = 4.5$ V	-	3.9	-	nC
Q_{gs}	Gate-source charge		-	0.4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	1.4	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 20$ V; $I_D = 1$ A;	-	2	-	ns
t_r	Turn-on rise time	$V_{GS} = 8$ V; $R_G = 6$ Ω	-	4.5	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	45	-	ns
t_f	Turn-off fall time		-	20	-	ns
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 16$ V; f = 1 MHz	-	152	-	pF
C_{oss}	Output capacitance		-	71	-	pF
C_{rss}	Feedback capacitance		-	33	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_a = 25$ ˚C	-	-	1.05	A
I_{DRM}	Pulsed reverse drain current		-	-	4.2	A
V_{SD}	Diode forward voltage	$I_F = 0.5$ A; $V_{GS} = 0$ V	-	0.74	1	V
t_{rr}	Reverse recovery time	$I_F = 0.5$ A; $-dI_F/dt = 100$ A/μs;	-	27	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0$ V; $V_R = 16$ V	-	19	-	nC