AKM

AK8428

Advanced video halftone processor

Features

☐Bi-level Image processing

Error diffusion

- 12 bit arithemetic processing internally

4×4, 8×8 dithering

- 3 types fixed dithering pattern included:Bayer, Uzumaki, Amiten
- Interface with the external ROM/PLD for other patterns
- Dithering offset:8 types, dithering amplitude:4 types programable

2 dimension distinction character part from photograph part

- Discrimination parameter programable

2 dimension MTF compensation

- For distinguished character part only

☐Enlargement/reduction

- Enlargement up to ×2, reduction up to 1/100 with 1% resolution for main scan
- Bi-level image processing execution/stop control for sub-scan
- Effective for not only bi-level processed image data but also multiple bits image data

☐Processing speed and clock rate

- ×8 main clock of data rate(5M pix/s max.)
  (ex.)40 MHz clock for 5M pix/s image processing
- Maximum clock rate 40MHz

☐Sensor clocks generation (programable)

☐AK8406 clocks generation

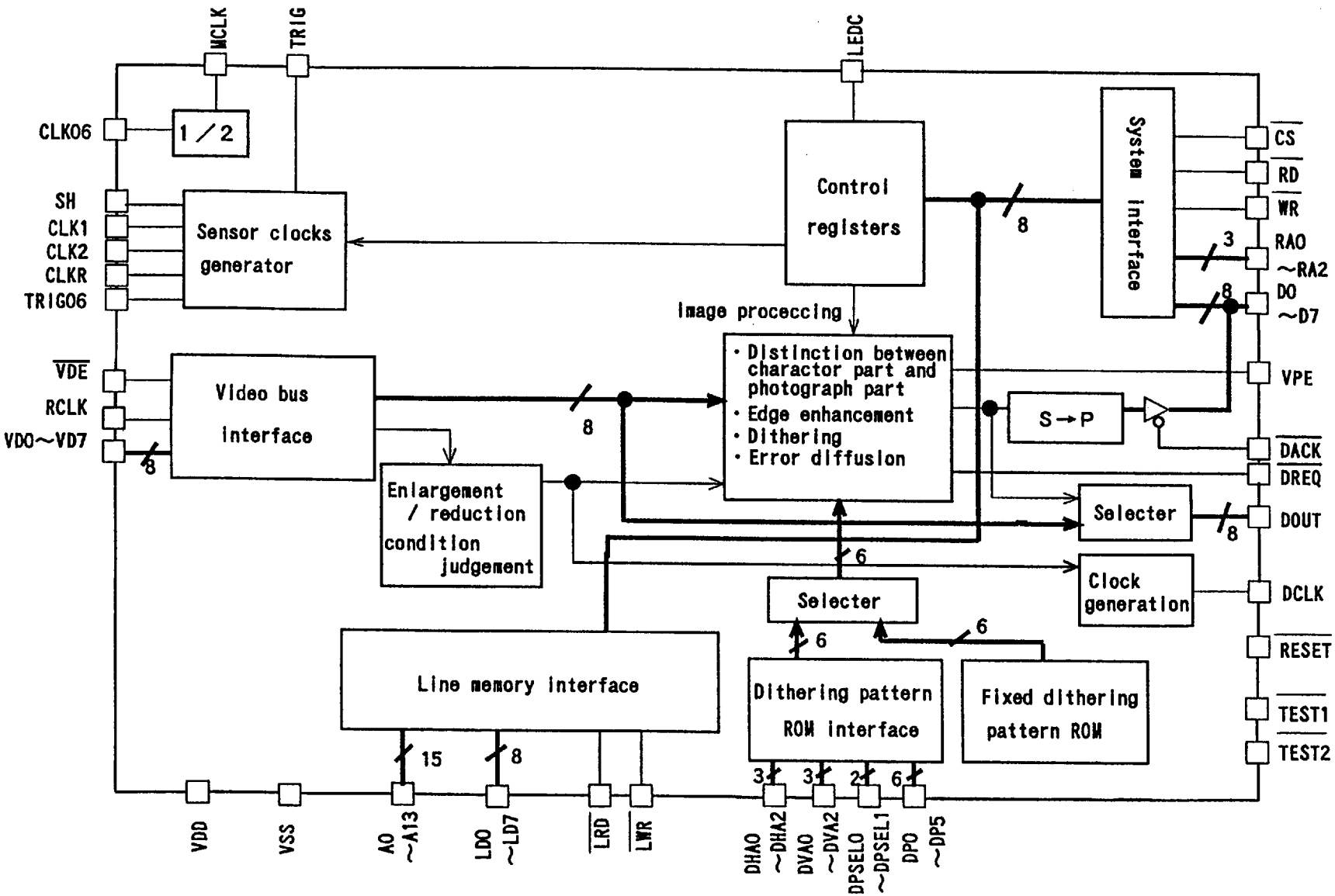
☐Sequential access to the line memory for image processing use possible

☐Parallel/sequencial video data outputs

- Parallel outputs(DMA transfer) and sequencial outputs for bi-level data
- Sequential outputs(8 bit) for multiple bits data

☐Package 100 pin QFP

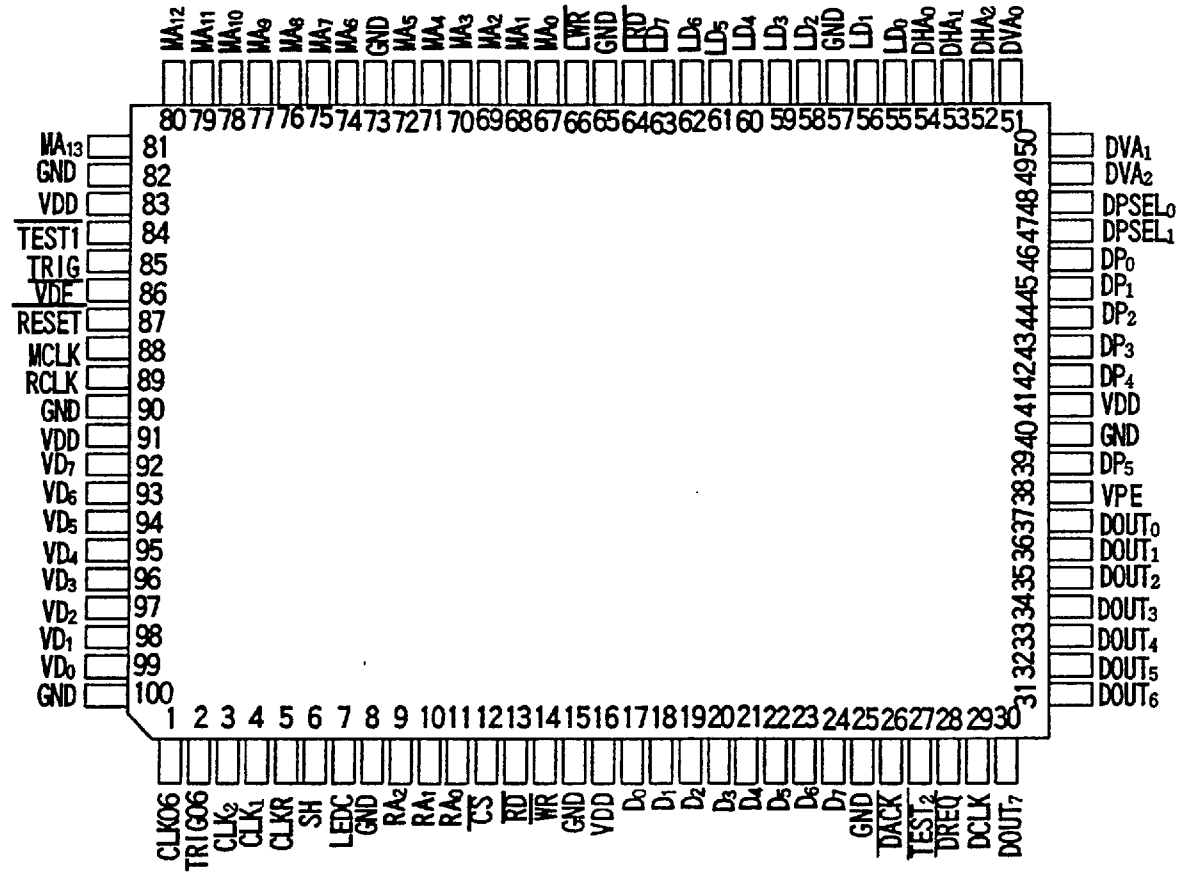
ASAHI KASEI®


MCLK
TRIG
LEDC
CLKO6
1/2
SH
CLK1
CLK2
CLKR
TRIGO6
Sensor clocks generator
Control registers
8
System interface
CS
RD
WR
3
RAO ~RA2
8
DO ~D7
Image proceccing
VDE
RCLK
VDO~VD7
8
Video bus interface
8
・Distinction between charactor part and photograph part
・Edge enhancement
・Dithering
・Error diffusion
VPE
S→P
DACK
DREQ
Enlargement / reduction condition judgement
Selecter
8
DOUT
6
Clock generation
DCLK
Selecter
6
6
RESET
Line memory interface
Dithering pattern ROM interface
Fixed dithering pattern ROM
TEST1
TEST2
15
8
3
3
2
6
VDD
VSS
AO ~A13
LDO ~LD7
LRD
LWR
DHAO ~DHA2
DVAO ~DVA2
DPSELO ~DPSEL1
DPO ~DP5

General description

(1)AK8428 is a hi-performance bi-level image processing LSI for AK8406.
(2)AK8428 has many bi-level image processing functions, that is, 256 gray shades ED, 64 gray shades dithering, 2 dimension character/photograph part distinction, 2 dimension MTF compensation, image enlargement/reduction.
(3)Image enlargement/reduction function ia effective for not only bi-level image data but also multiple bits(8 bit) data.
(4)AK8428 generates sensor clocks, ak8406 clocks(MCLK, TRIG).

Pinouts



Pin description

NO	Name	I/O	Function
			Power supply pins
16, 41, 83 91	VDD	-	+5 V
8, 15, 25 40, 57, 65 73, 82, 90 100	VSS	-	Ground
			Clocks and test use pins
88	MCLK	I	Master clock input, whose freq must be multiplied by 4 of data rate(40 MHz max).
84 27	(TEST1) (TEST2)	I	Test pins. Pull up to VDD normally.
85	TRIG	I	Line start signal.
			Sensor clocks
4, 3	CLK1, CLK2	O	2 phase clocks for the image sensor.
5	CLKR	O	Reset clock for the image sensor.
6	SH	O	SH clock for the image sensor.
			AK8406 clocks
1	CLK06	O	Master clock for AK AK8406, which is one devided by 2 of MCLK.
2	TRIG06	O	Line start signal for AK8406. Connect with AK8406 TRIG input.
			Video input bus interface
86	VDE	I	Input signal, which indicates data valid period. AK8428 latches the data by RCLK when this input is 'L' (data valid). Connect with AK8406 $\overline{SOE}$ pin.
99~92	VD0~VD7	I	8 bit image data inputs. Connect with AK8406 VD0 ~VD7 outputs.
89	RCLK	I	Clock input which latches VD0~VD7. With rising edge of this clock, VD0~VD7 are latched.

NO	Name	I/O	Function
Micro computer interface			
12	$\overline{CS}$	I	Chip select signal.
13	$\overline{RD}$	I	Read signal.
14	$\overline{WR}$	I	Write signal.
11~9	RA0~RA2	I	Address inputs for selecting internal registers.
87	$\overline{RESET}$	I	Reset signal. Some registers are reset by this input.
17~24	D0~D7	I/O (3state)	System data bus.
28	$\overline{DREQ}$	O	DMA request output.
26	$\overline{DACK}$	I	DMA acknowledge input.
Line memory interface			
67~72 74~80	A0~A12	O	Address outputs. A sensor whose pixels count is 8184 can be used.
81	A13	O	Bank select signal of the line memory.
55,56 58~63	LD0~LD7	I/O (3state)	Data bus of the line memory.
64	$\overline{LRD}$	O	Read signal for the line momory.
66	$\overline{LWR}$	O	Write signal for the line memory.
Dithering pattern use ROM/PLD interface			
54~52	DHA0~DHA2	O	Horizontal addresses for dithering pattern.
51~49	DVA0~DVA2	O	Vertical addresses for dithering pattern.
48~47	DPSEL0~ DPSEL1	O	External dithering pattern select outputs.
46~42	DP0~DP5	I	External dithering pattern inputs.
Image data output bus interface			
29	DCLK	O	Clock for video data outputs. Image data output synchronised with the falling edge of this clock
37~30	DOUT0~DOUT7	O	Image data sequential outputs. Only DOUT0 is valid at bi-level processing.
Other pins			
7	LEDC	O	General output port which can be used LED light control and so on.
38	VPE	I	Video processing enable, which controls video processing for the next line.

Functional description

1. AK8406 interface and sensor clocks generation

AK8428 generates AK8406 master clock(CLK06), that is a half rate clock of MCLK, AK8406 line start signal(TRIG06), sensor timing clocks(CLK1, CLK2, CLKR, SH) by master clock(MCLK) and line start input(TRIG).
These clocks are phase synchronized by every TRIG input.
Timing adjustment for the delay of the pre-amplifier and so on can be done by putting forward CLK1, CLK2 with 1/MCLK unit. The timing of CLKR can be also programmed.
MCLK must be ×8 of the sensor data rate.

2. Image data input interface with AK8406

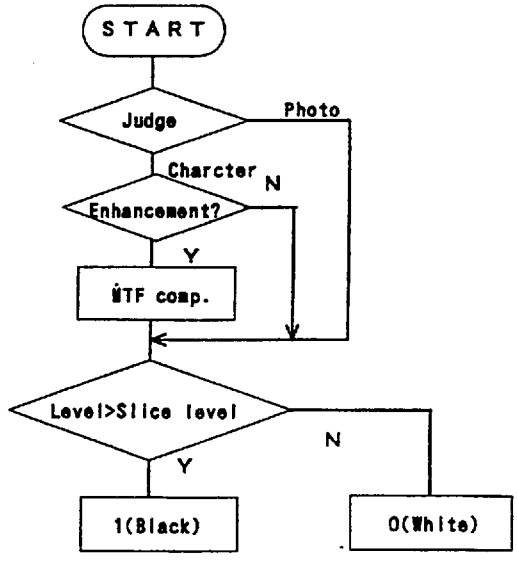
AK8406 manages pre-dummy pixels count and sensor pixels count. AK8428 latches AK8406 8 bit image data(VD0~VD7) by the rising edge of the RCLK during $\overline{VDE}$=L, and does bi-level image processing. AK8428 recognizes the line-end by TCLK disappearing automatic-ally.
AK8406 TCLK can be used as the RCLK, and AK8406 $\overline{SOE}$ as $\overline{VDE}$.

3. Bi-level image processing

3 – 1. Image processing mode

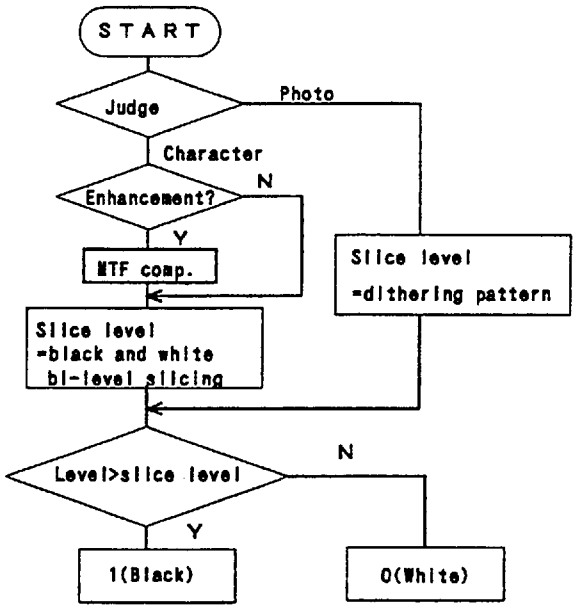
AK8428 has 4 types of bi-level image processing modes. The each processing flow is as the following diagram.

(A)Black and white mode
As the result of distiction character/photograph part, the character part is bi-level sliced after MTF compensation, which is controlled by another register, and the photograph part is bi-level sliced without MTF compensation.



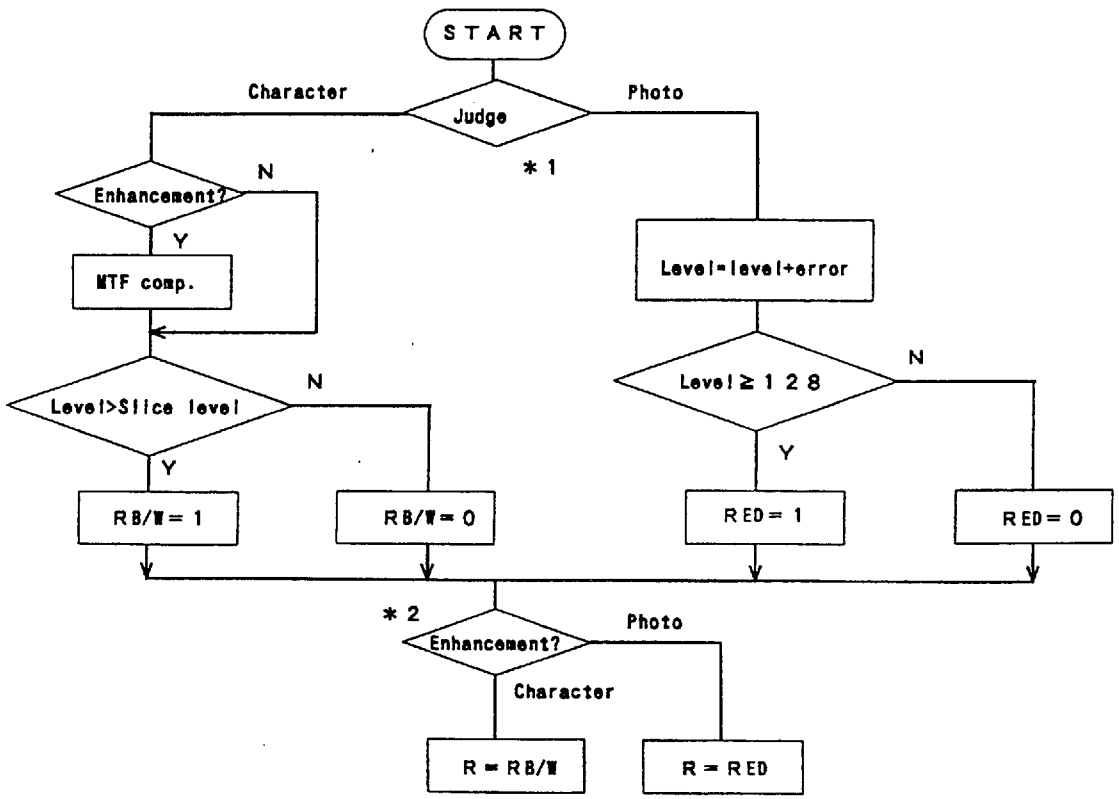
(B)Dithering mode

As the result of distiction character/photograph part, the character part is bi-level sliced after MTF compensation, which is controlled by another register, and the photograph part is image processed by dither.



(C)Error diffusion A mode

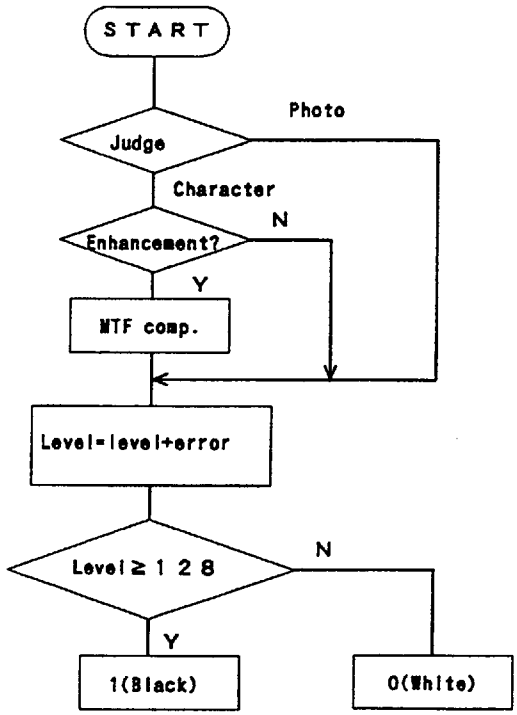
As the result of distiction character/photograph part, the character part is bi-level sliced after MTF compensation, which is controlled by another register, and the photograph part is image processed by error diffusion method.



(NOTE)*1 and *2 are the same judgement

(D)Error diffusion B mode

As the result of distiction character/photograph part, after MTF compensation of character part, which is controlled by another register, both parts are image processed by the error diffusion method.



3 − 2. Distinction character/photograph part

AK8428 distinguishes the character/photograph part by level difference with the surrounding pixels. The judgement threshold can be set by the register.

3 − 3. MTF compensation

AK8428 does MTF compensation by modified Laplacian filter.

3 − 4 . Dithering

Ak8428 generates the actual slicing level by operating arithmetic operand(b) to the dither pattern(a).

(a) Dither pattern

AK8428 has 6 dithering pattern, that is, 3 patterns for 4×4 matrix and 3 patterns for 8×8 matrix. AK8428 has the interface with external ROM/PLD for other patterns.

0	32	8	40
48	16	56	24
12	44	4	36
60	28	52	20

4 × 4 Bayer

0	32	8	40	2	34	10	42
48	16	56	24	50	18	58	26
12	44	4	36	14	46	6	38
60	28	52	20	62	30	54	22
3	35	11	43	1	33	9	41
51	19	59	27	49	17	57	25
15	47	7	39	13	45	5	37
63	31	55	23	61	29	53	21

8 × 8 Bayer

24	28	32	36
20	0	4	40
16	12	8	44
60	56	52	48

4 × 4 Uzumaki

24	28	32	36	26	30	34	38
20	0	4	40	22	2	6	42
16	12	8	44	18	14	10	46
60	56	52	48	62	58	54	50
27	31	35	39	25	29	33	37
23	3	7	43	21	1	5	41
19	15	11	47	17	13	9	45
63	59	55	51	61	57	53	49

8 × 8 Uzumaki

0	8	56	48
32	40	20	28
60	52	4	12
16	24	36	44

4 × 4 Amiten

0	8	56	48	2	10	58	50
32	40	20	28	34	42	22	30
60	52	4	12	62	54	6	14
16	24	36	44	18	26	38	46
3	11	59	51	1	9	57	49
35	43	23	31	33	41	21	29
63	55	7	15	61	53	5	13
19	27	39	47	17	25	37	45

8 × 8 Amiten

(Interface signals with external ROM/PLD)

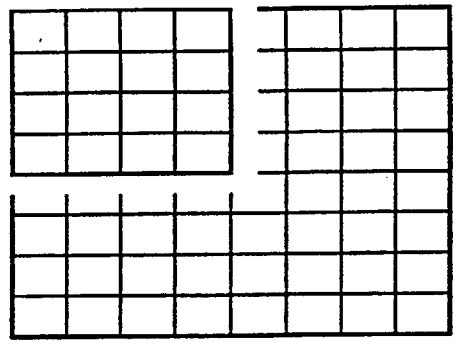
DHA0~DHA2	Horizontal addresses outputs
DVA0~DVA2	Vertical addresses outputs
DP0~DP5	Pattern data inputs
DPSEL0~DPSEL1	Pattern select outputs

When using 4×4 pattern, arrange the pattern as the pattern changes with the each lower 2 bits of the horizontal addresses and vertical addresses.

(b) Slice level generation

AK8428 generates actual 8 bit dithering slice level by operating the following equation to the 6 bit dithering pattern.

$$\{ A \times (\quad - 32) + 128 \} + B$$



A is 4 types of the dithering amplitude parameter(1, 2, 3, 4).
B is 8 types of the dithering offset parameter(-32, -16, 0, 16, 32, 48, 64, 80), whose reference level is 128.
The products of the arithmatic operation is limited to 0 if it is less than 0 , and it is limited to 254 if it is more than 254.

Slice level generation for the black and white type bi-level processing is 6 bit setting data to 8 bit actual slice level conversion according to the follo -wing equation.

Actual slice level= 4 × set parameter + 3

In the black/white and dithering mode, when level>actual slice level, the results is black(1), when level≦actual slice level, the result is white(0).

3 – 5 . Error diffusion

AK8428 diffuses the fixed coefficient multiplied 8 bit error data with sign(-127～127) by bi-level processing to the surrounding pixels. AK8428 does 12 bits operation for minimizing the arithmetic operation error.

3 – 6 . Enlargement/reduction

AK8428 can reduce the image with 1%～99% reduction ratio, and enlage with 101%～200% enlargement ratio by 1% unit.
Enlagement/reduction function is effective for multipul bits data also.

4. Output video data format

4 – 1. Sequencial data

AK8428 outputs multiple bits data through VD data bus(VD0~VD7)or bi-level data through VD0 with DCLK. DCLK is thinned out at reduction mode, and inserted at enlargem -ent mode.

4 – 2. Parallel data(DMA interface)

The bi-level processing image data by AK8428 can be read through the system data bus(D0~D7) after serial to parallel conversion.
According to the AK8428 DMA reques($\overline{DREQ}$), set the $\overline{DACK}$ to the "L" state read out the image data by DMA controller .

4 – 3. DCLK/$\overline{DREQ}$ clock count

DCLK, $\overline{DREQ}$ clock count is as following equations.

No enlargement and reduction case

N : pixel counts (Multiple of 8)

$$n_{DCLK} = N$$
$$n_{DREQ} = N / 8 = n$$

Enlargement and reduction case

N : pixel counts (Multiple of 8)
k : enlargement/reduction ratio
[M] : minimum integer not less than M

$$n_{DCLK} = [N \times k]$$
$$n_{DREQ} = [[N \times k] / 8]$$

(EX 1) N = 1728, k = 0.71

$$n_{DCLK} = [1728 \times 0.71] = [1266.88] = 1267$$
$$n_{DREQ} = [[1728 \times 0.71] / 8] = [[1266.88] / 8]$$
$$= [1267 / 8] = [158.375] = 159$$

(EX 2) N = 1728, k = 1.15

$$n_{DCLK} = [1728 \times 1.15] = [1987.2] = 1988$$
$$n_{DREQ} = [[1728 \times 1.15] / 8] = [[1987.2] / 8]$$
$$= [1988 / 8] = [248.5] = 249$$

AK8428 fill with 0 to let enlarged or reduced pixel count to be a multiple of 8 in the parallel(DMA) interface.

5. Operation control

5 – 1. Shading data(black/white/peak) detect modes

AK8428 generates the clocks(CLK1, CLK2, CLKR, SH) for the image sensor, and clocks (CLK06, TRIG06) for AK8406.

5 – 2. Document read mode

At the first line of a page, set the VPE bit or VPE pin to the enable state, and the PAGE START bit, which indicates the first line of the page, to the enable state.
By the first TRIG after the command set, image processing starts. At the first line end, the PAGE START bit is automatically reset.
When thinning out lines or stopping paper feed, VPE bit or VPE pin must be set to the disable state for keeping the continuity of image processing(dithering or error diffusion). By the first TRIG after the command set, the command is accepted.
During the image processing, DCLK, $\overline{\text{DREQ}}$, the bi-level image processed data output with 1 line delayed. Multiple bits data and DCLK are output with no delay.
Note that, because the image processing control is done by VPE pin or VPE bit, unused one(VPE pin or VPE bit) must be "L" state.

5 – 3. Line memory access mode

The line memory for the image processing use can be accessed through AK8428. When using in this mode, VPE bit or VPE pin must be the disable state, and LMAE bit must be changed 0→1 for initializing the address counter.
After that line memory can be accessed sequentially by accessing R7 register. Selec -ting the bank(original data bank/error data bank) can be done by the LINE MEMORY BANK SELECT bit.

Registers

RA0~RA2 (HEX)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	W	X					line memory access enable	page start	video process-ing enable
1	W	ditha pattern int/ext select	bi-level image processing mode select		bi-/mul-tiple level select	general output control (LEDC)	CLK1 select		CLKR select
2	W	ditha pattern control							
		amplitude select		offset select			matrix select	pattern select	
3	W	enlargement/reduction ratio							
4	W	enlarge-ment/ reduct-ion enable	line memory bank select	judgement thereshold for black point (protect tiny line thinning out at reduction mode)					
5	W	MTF enhance-ment enable	parameter for photograph/character part descrimination						
6	W	X		bi-level slice level (black and white)					
7	R/W	line memory access window							

DMA register	R	VD_{N-7}	VD_{N-6}	VD_{N-5}	VD_{N-4}	VD_{N-3}	VD_{N-2}	VD_{N-1}	VD_N

* 1 : □
  indicates the registers which are reset by $\overline{RESET}$.
* 2 : ▨
  indicates the registers whose command is effective by the first TRIG after the command set.

* 3 : DMA register can be read by $\overline{DACK}$.

1. R 0 register

(1) D 0 : video processing enable
0 : stop
1 : enable

(2) D 1 : page start

0 : normal
1 : page start

(3) D 2 : line memory access enable

0 : disable
1 : enable

2. R1 register

(1) D0/D1~D2 : CLKR/CLK1 timing select

D0	CLKR timing	D2	D1	CLK1 timing
0	A	0	0	A
1	B	0	1	B
		1	0	C
		1	1	D

Refer to the timing diagram as for A, B, C, D states of CLK1, CLK2, and A, B states of of CLKR.

(2) D3 : LEDC port control

0 : LEDC = 0
1 : LEDC = 1

(3) D4 : bi-/multiple level

0 : bi-level
1 : multiple level

(4) D5 ~ D6 : bi- level image processing mode

D6	D5	
0	0	black and white
0	1	dithering
1	0	error diffusion A mode
1	1	error diffusion B mode

(5) D7 : ditering pattern internal/external select

0 : internal pattern(3 types)
1 : external pattern(4 types)

3. R2 register

(1) D0 ~ D1 : dither pattern select

D1	D0	internal	external
0	0	Bayer	DPSEL1/DPSEL0=0/0
0	1	Uzumaki	DPSEL1/DPSEL0=0/1
1	0	Amiten	DPSEL1/DPSEL0=1/0
1	1	X	DPSEL1/DPSEL0=1/1

(2) D2 : dither matrix select

0 : 8×8
1 : 4×4

(3) D3 ~ D5 : dither offset select

D5	D4	D3	offset
0	0	0	−32
0	0	1	−16
0	1	0	0
0	1	1	16
1	0	0	32
1	0	1	48
1	1	0	64
1	1	1	80

(4) D6 ~ D7 : dither amplitude select

D7	D6	amplitude
0	0	1
0	1	2
1	0	3
1	1	4

4. R3 register

(1) D0～D7 : enlargement/reduction ratio(1/100～200/100)

Set a numerator.

5. R4 register

(1) D0～D5 : judgement threshold for protecting tiny black line thinning out

When N(0～63) is the setting parameter, actual threshold N_R is as the following equation.

$N_R = 4 \times N$ (N = 1～63)
N = 0 disable

(2) D6 : line memory bank select

D6	line memory bank	A13
0	original data bank	0
1	error data bank	1

(3) D7 : enlargement/reduction enable

0 : disable
1 : enable

6. R5 register

(1) D0～D6 : distinction threshold of photo/character part

When actual level differences with surrounding pixels is more than or equal with the setting parameter, which part is judged as the character part.

(2) D7 : MTF compensation enable

0 : disable
1 : enable

7. R6 register

(1) D0～D5 : slice level(black/ white mode)

When N(0～63) is the setting parameter, actual slice level N_S is as the following equation.

$N_S = 4 \times N + 3$ (N = 0～63)

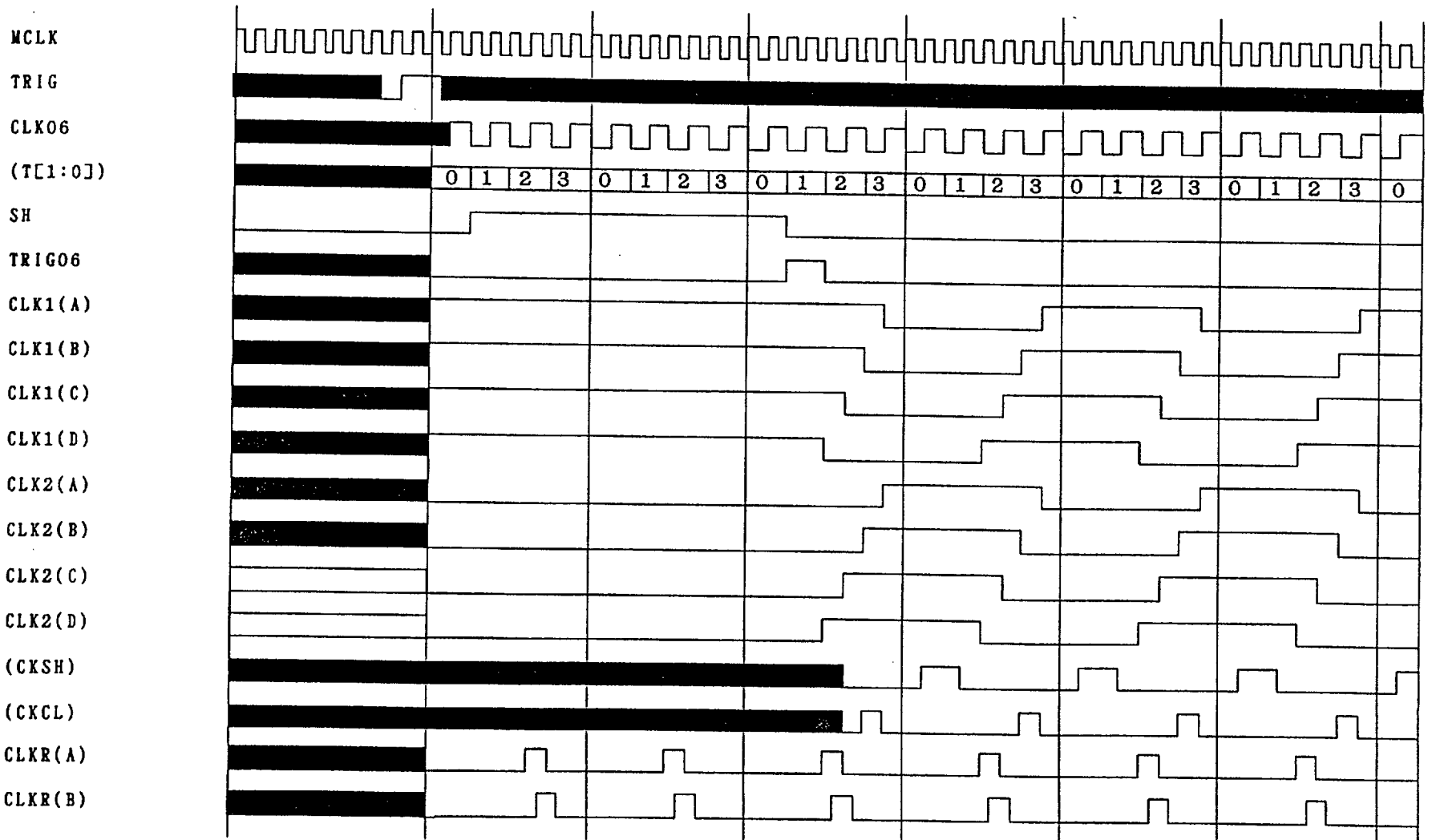
8. R7 register : line memory access register

When accessing to the line memory, use this register as the window register.

9. DMA register

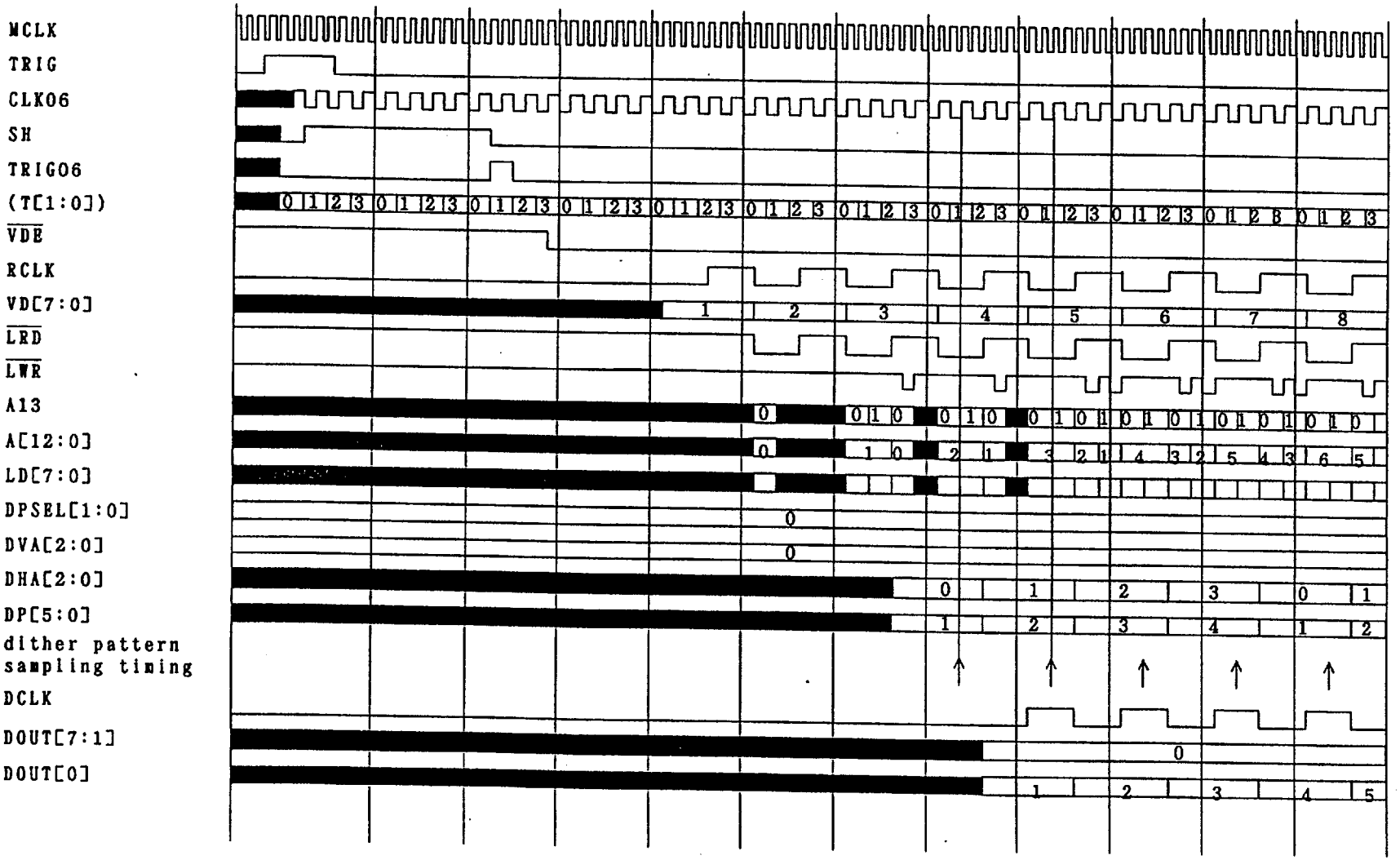
At the bi-level processing mode, image processed data can be read through this register.

1. TRIG、CLK06、SH、TRIG06、CLK1、CLK2、CLKR

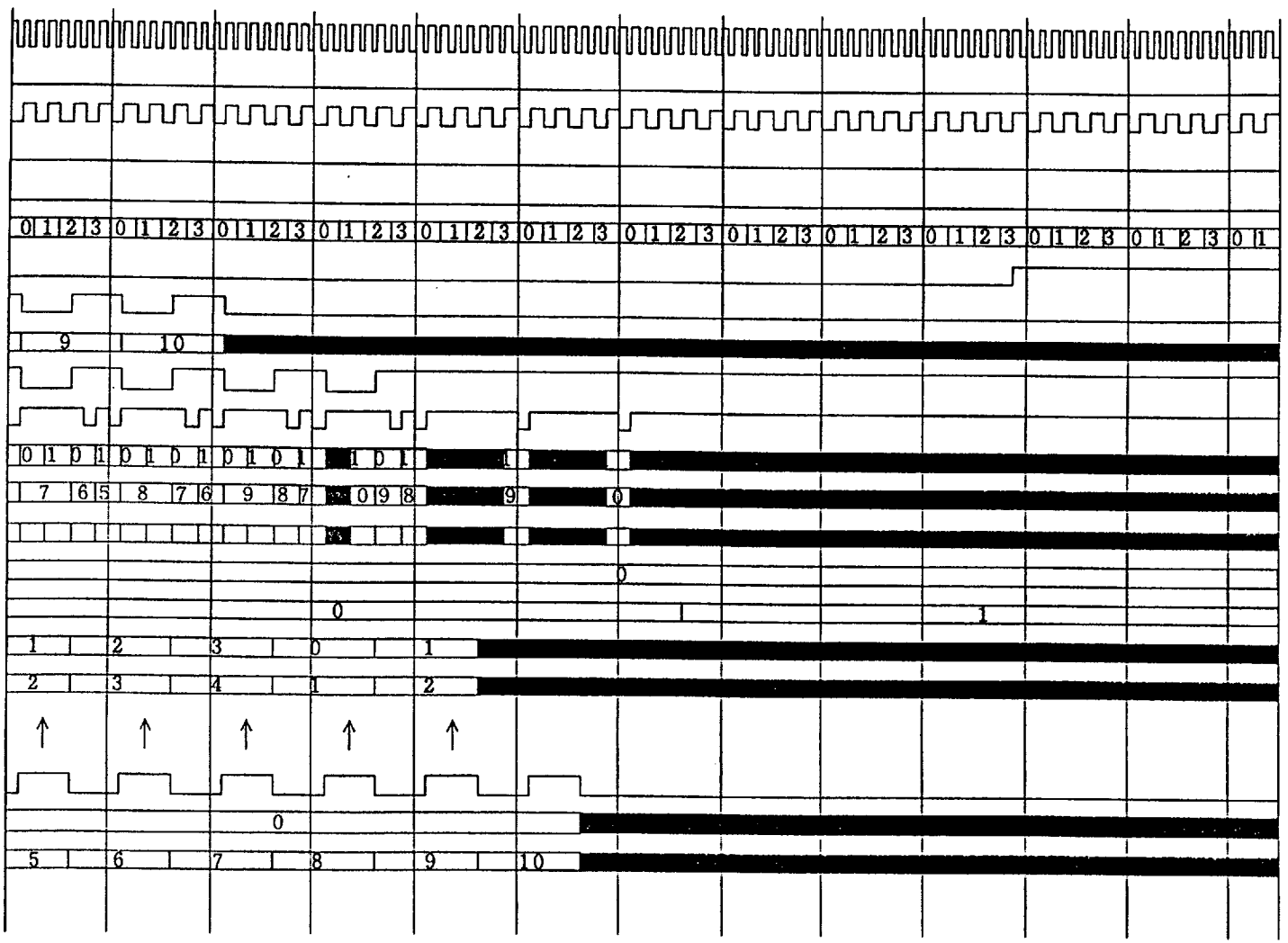


(注) T [1 : 0] : internal signals

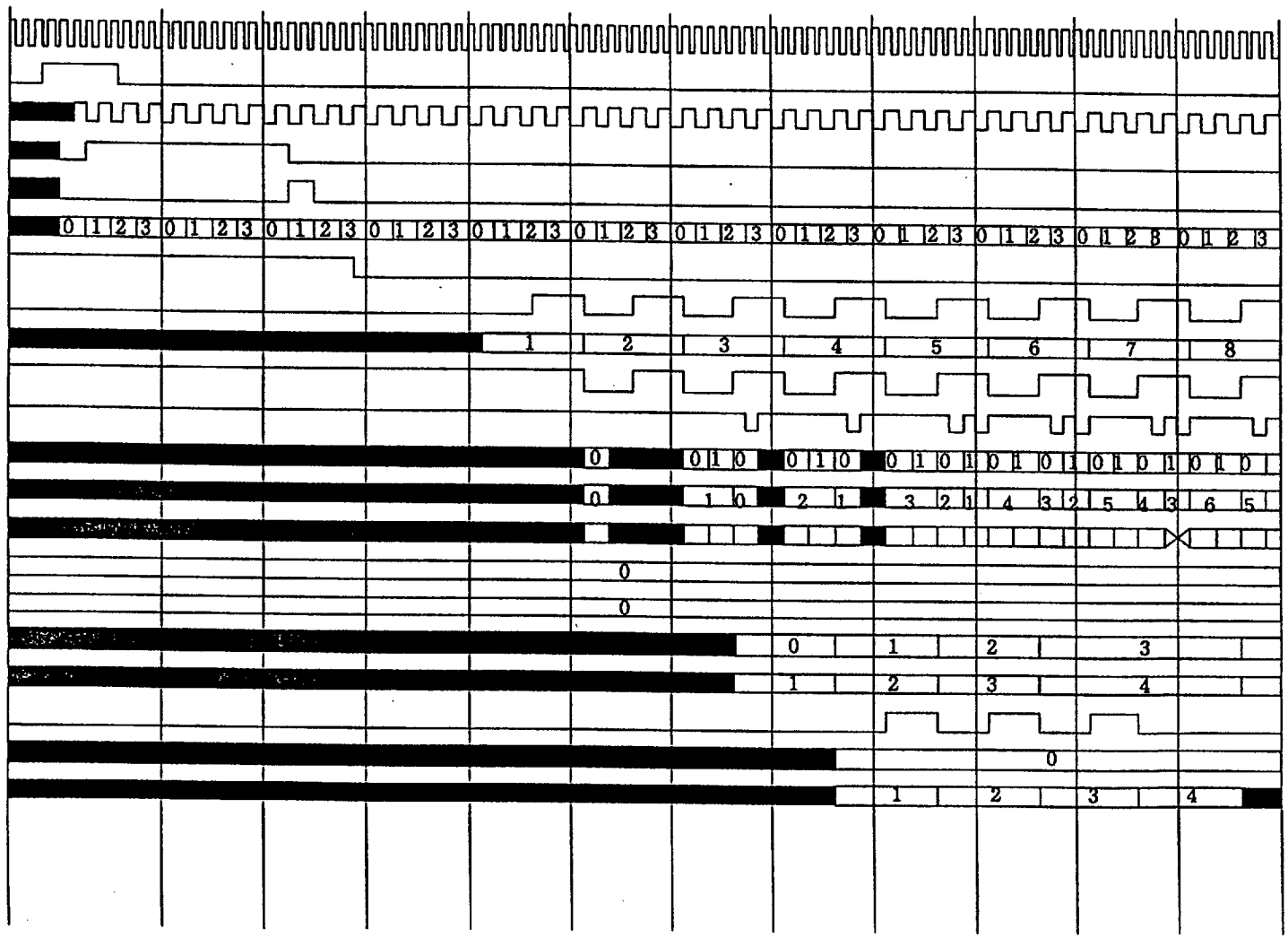
2－1．Bi-level image processing(no enlargement/reduction)



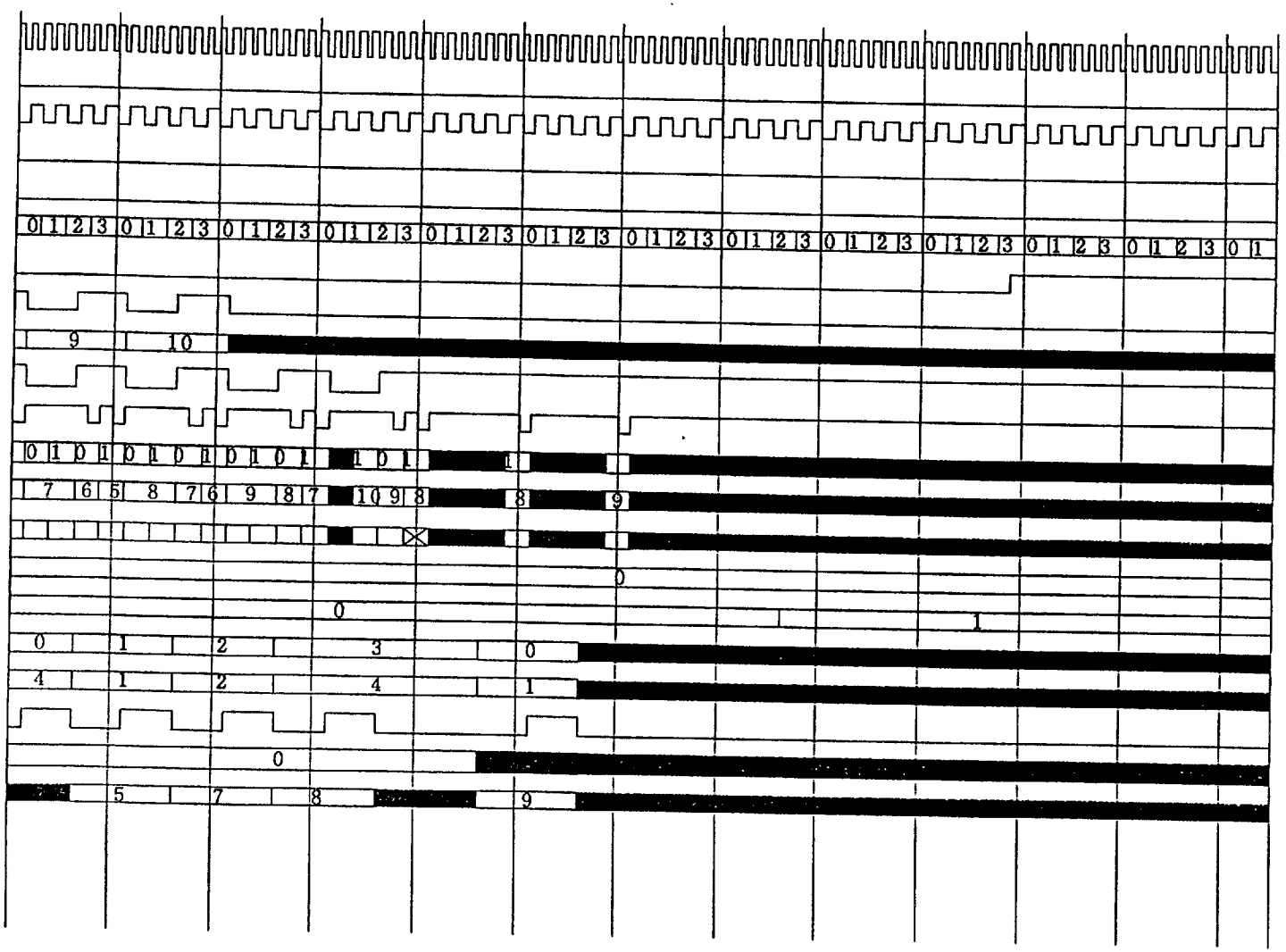
2－2． Bi-level image processing(No enlargement/reduction)…continued



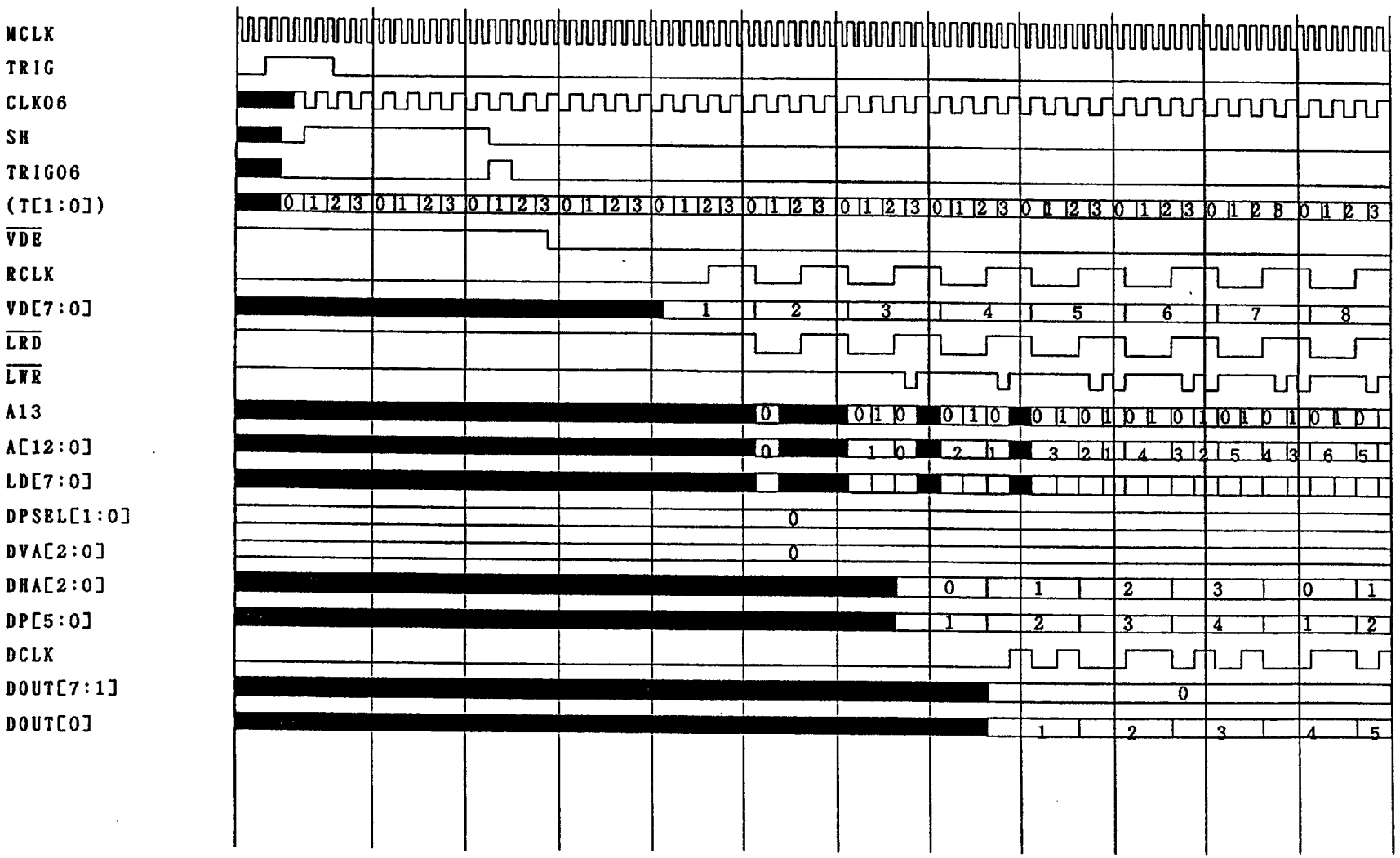
3 – 1 . Bi-level image processing(Reduction: 80%)



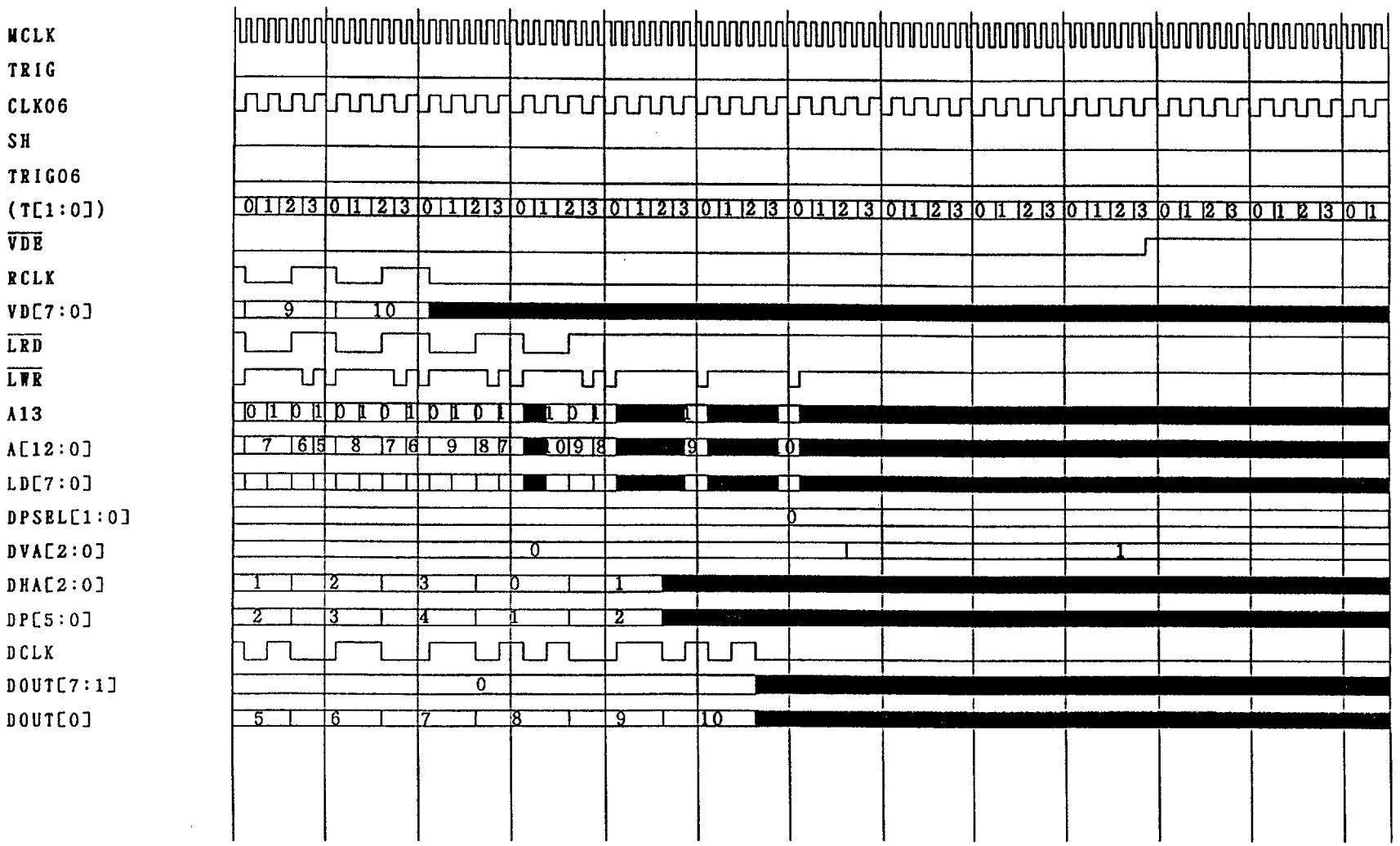
3 – 2. Bi-level image processing(Reduction: 80%)···continued



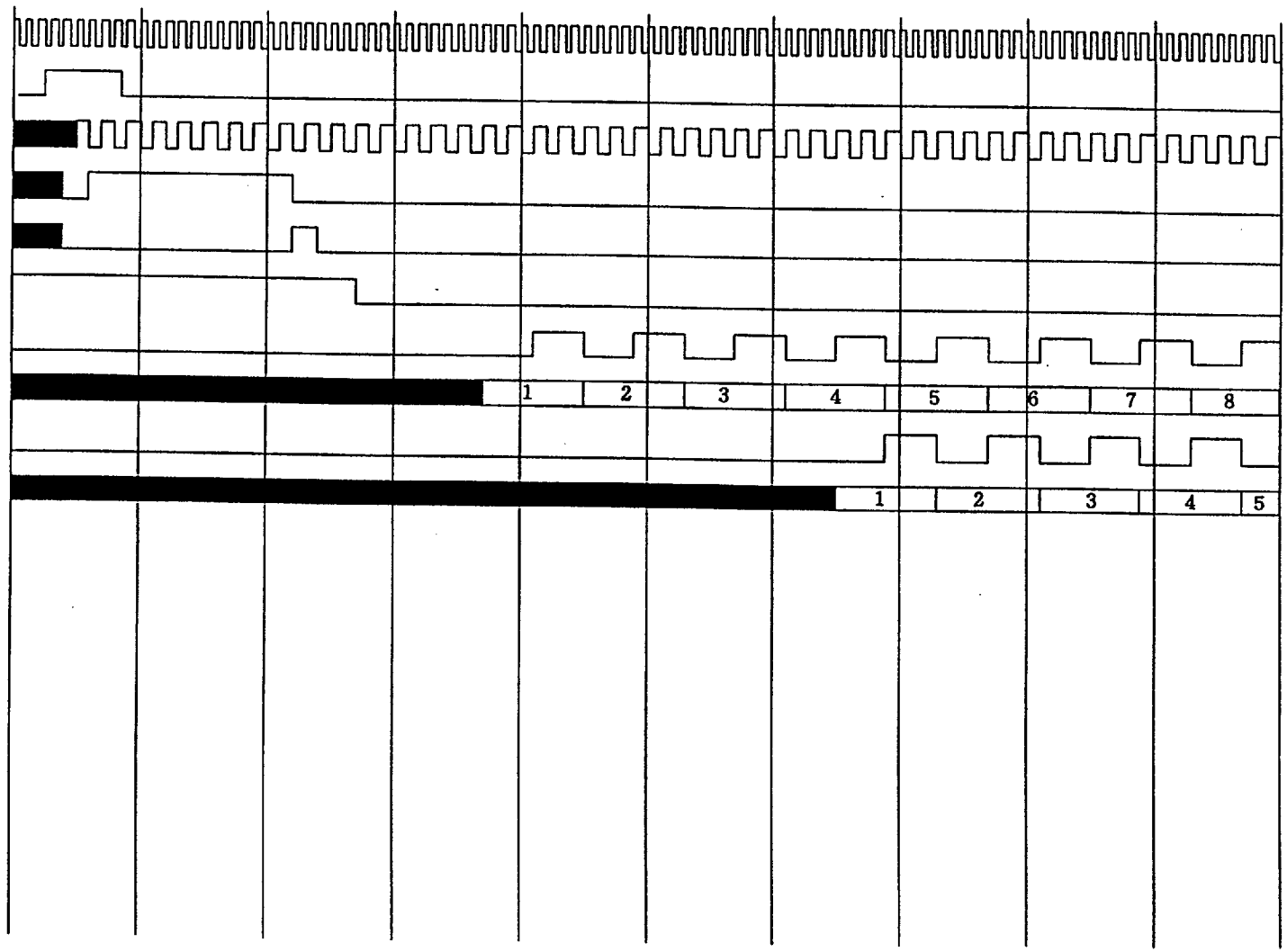
4－1． Bi-level image processing(Enlargement:141%)



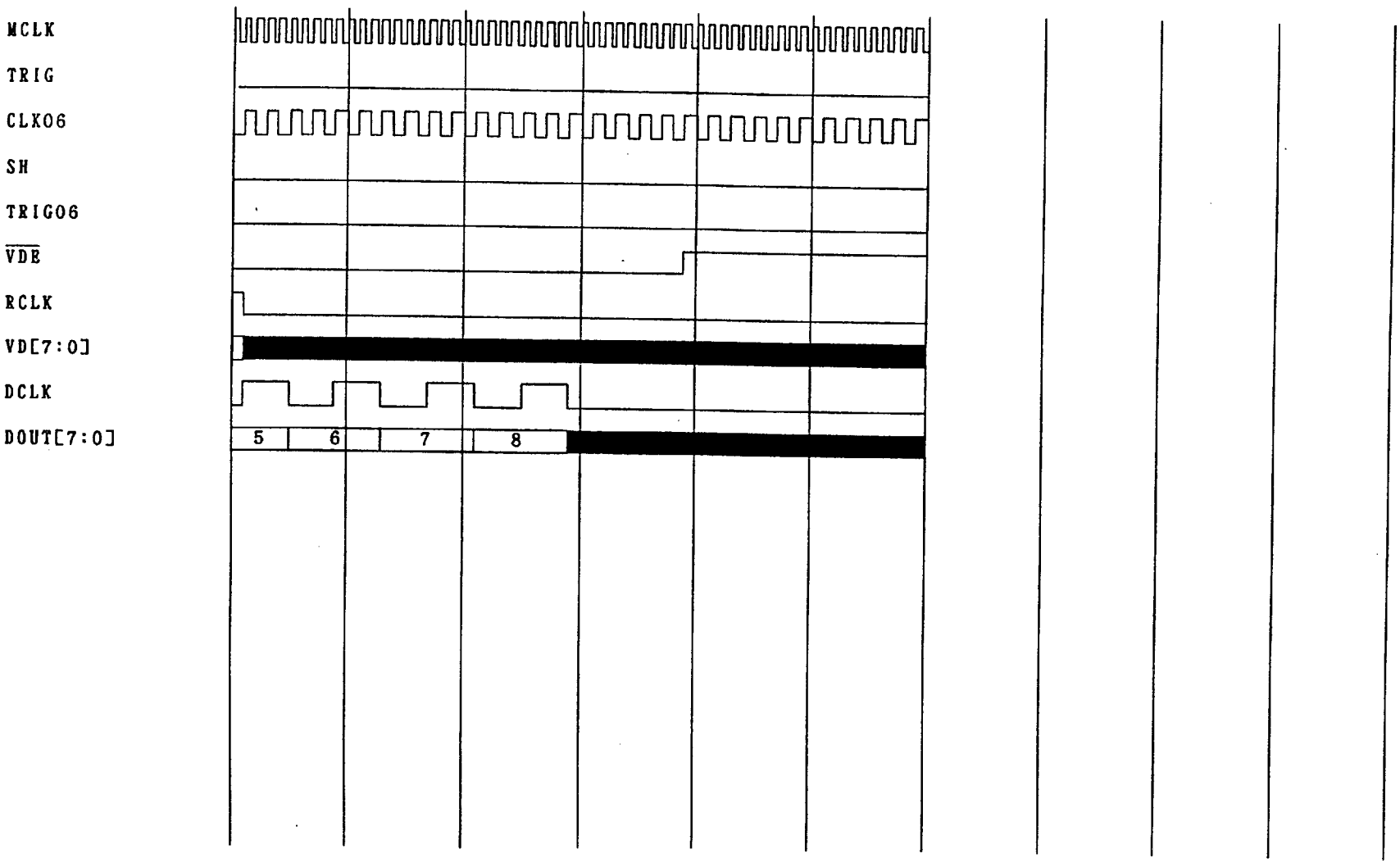
4－2． Bi-level image processing(Enlargement:141%)…continued



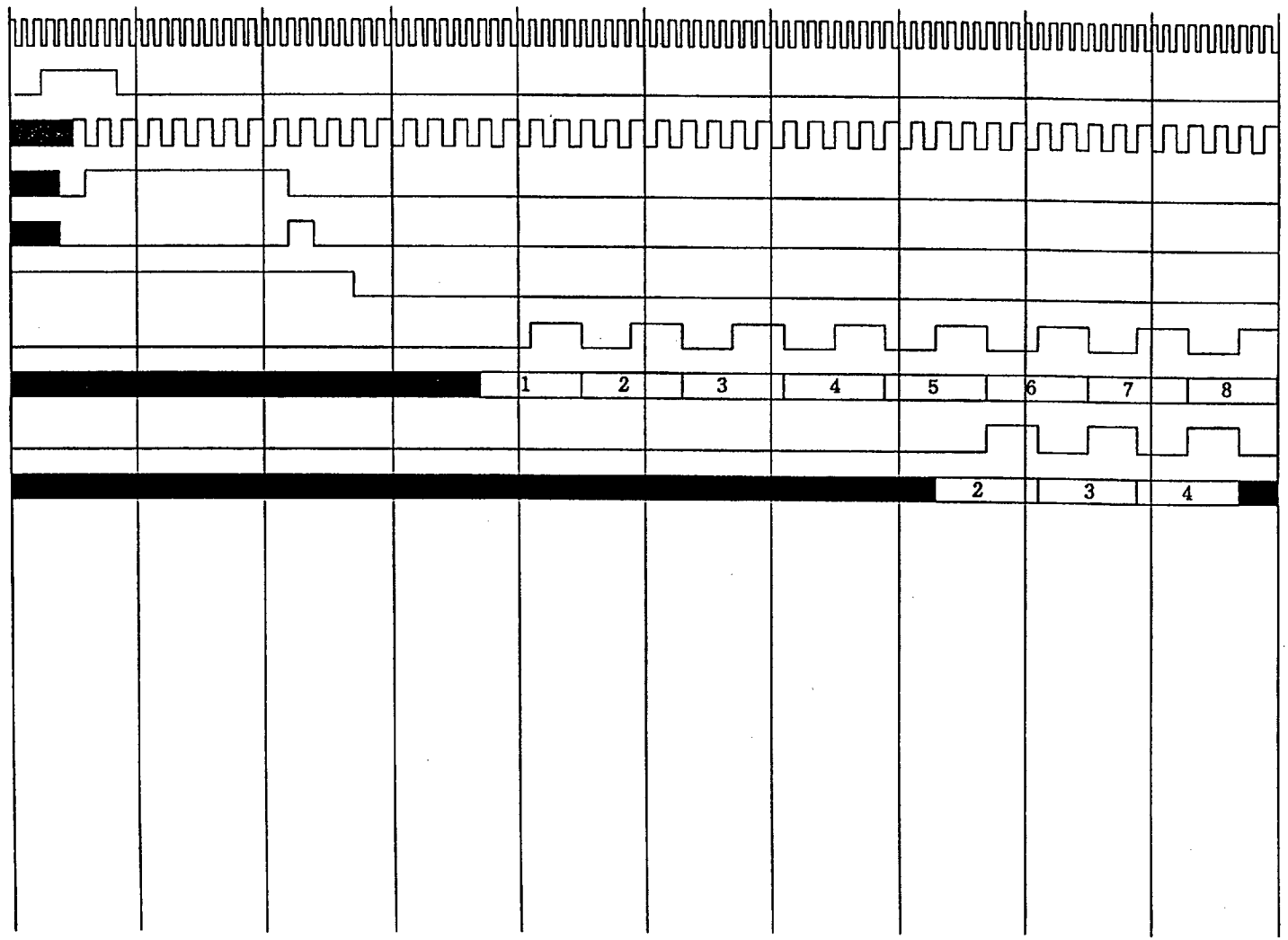
5－1．　Multiple level mode(No reduction/enlargement)



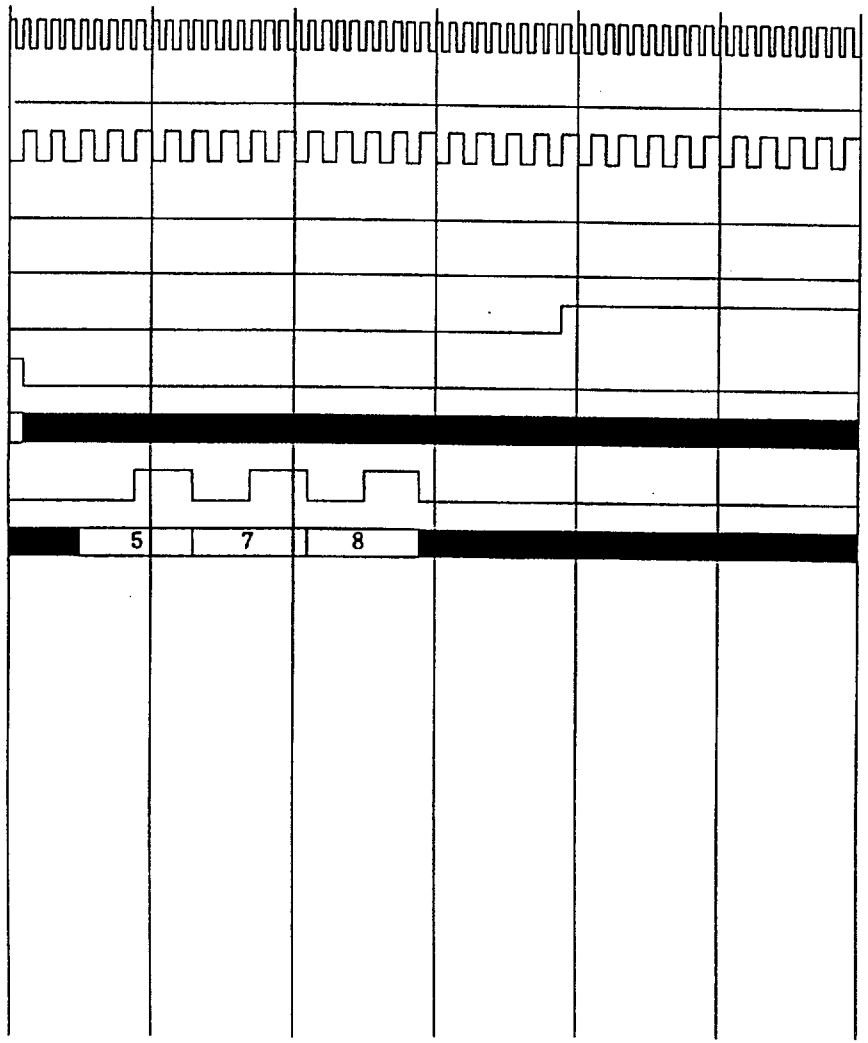
5 – 2. Multiple level mode(No reduction/enlargement)···continued



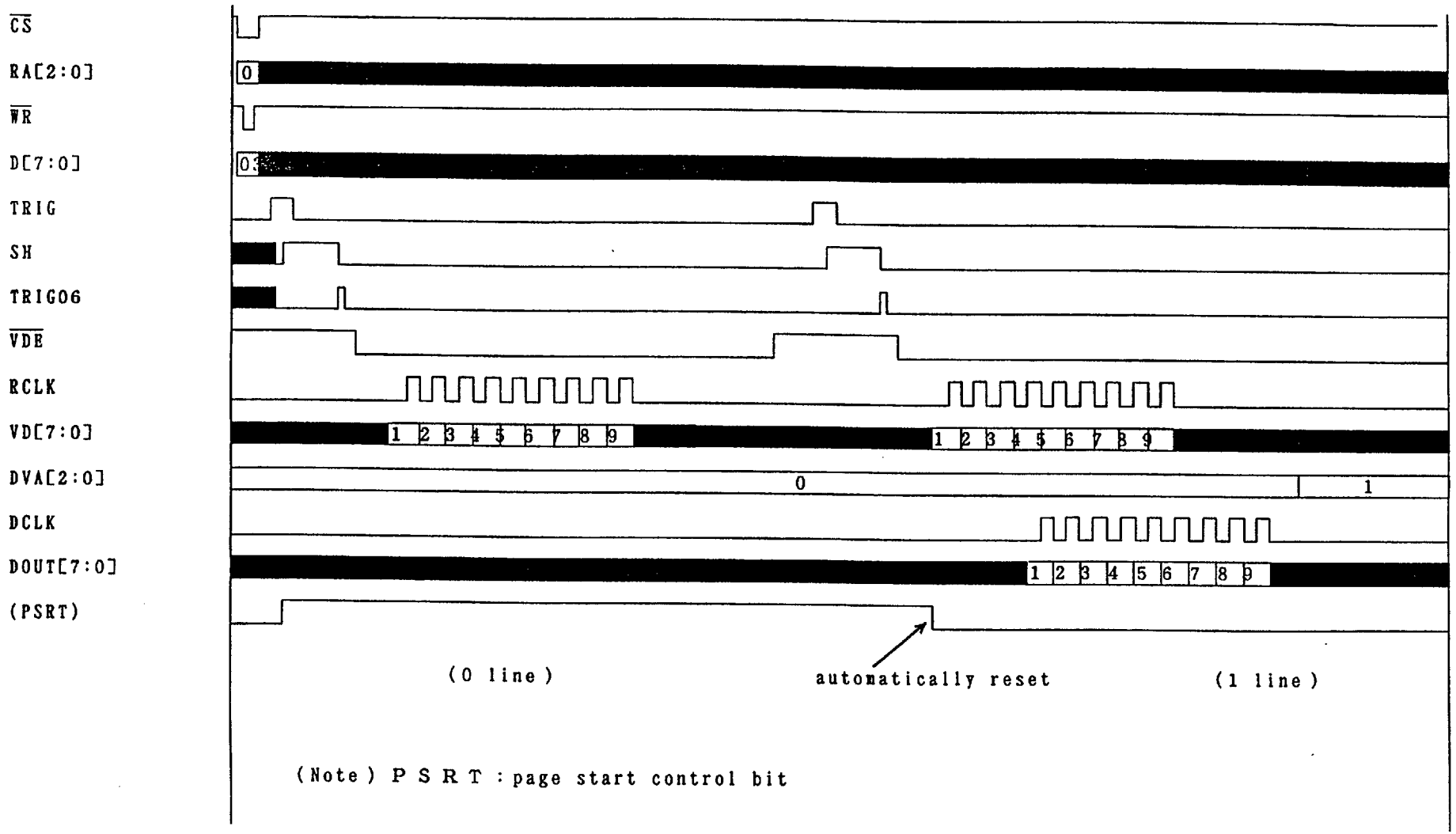
6-1. Multiple level mode(Reduction: 80%)



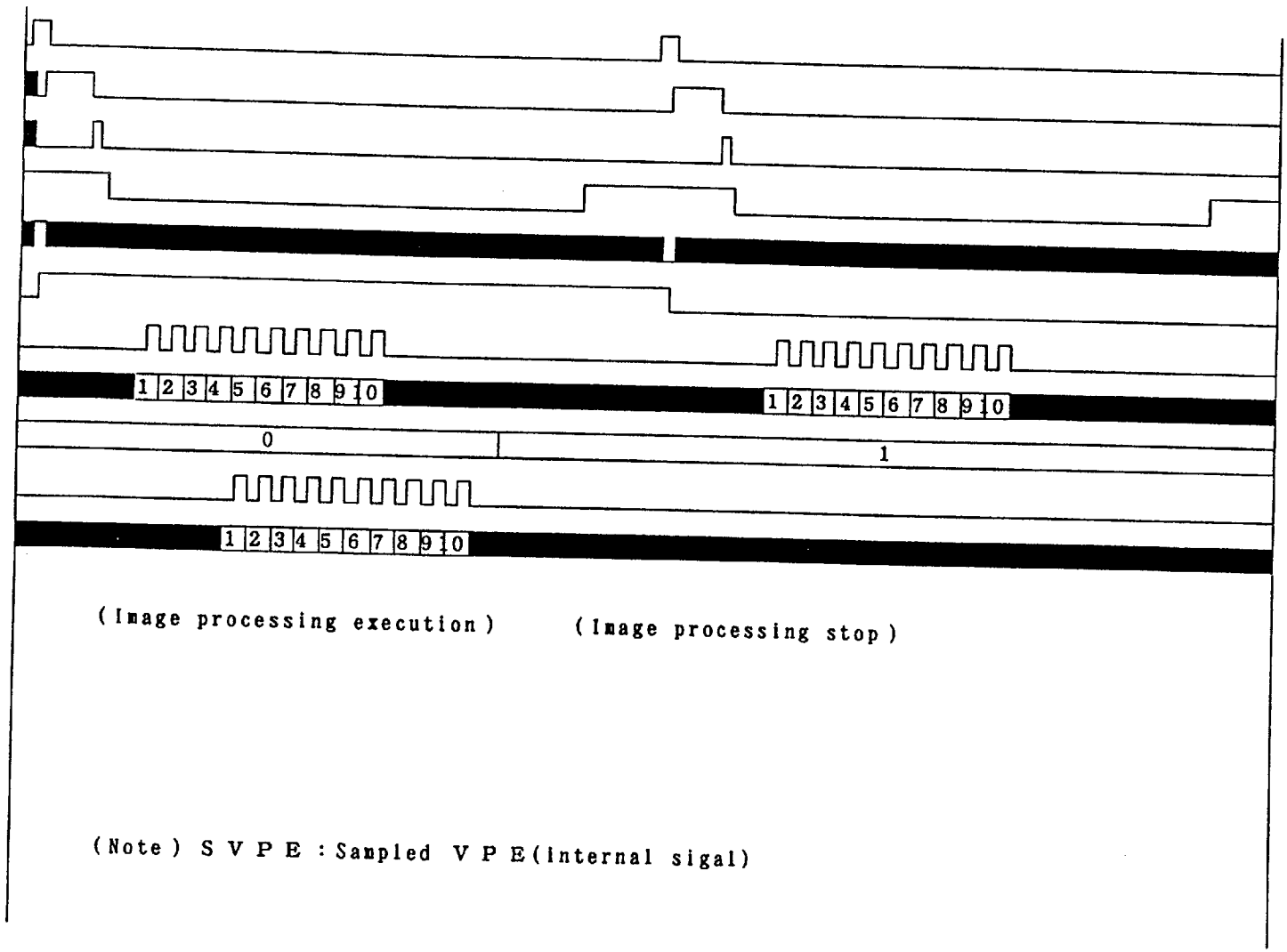
6 − 2 . Multiple level mode(Reduction: 80%)···continued



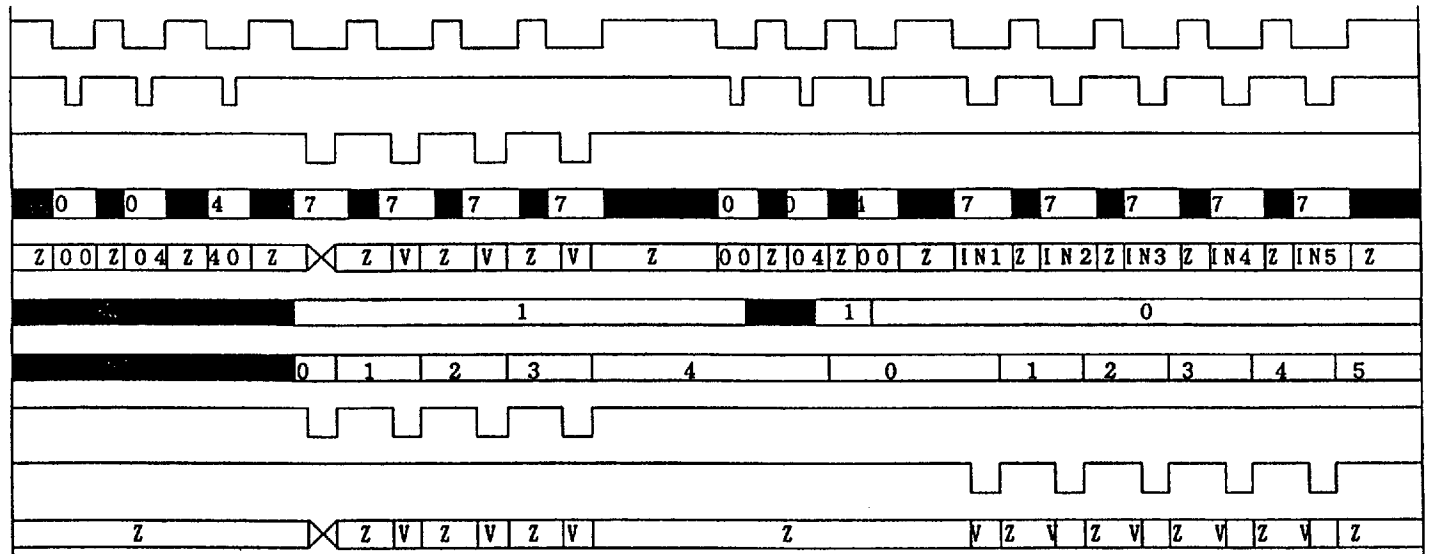
7. Page start control bit



8. VPE control pin

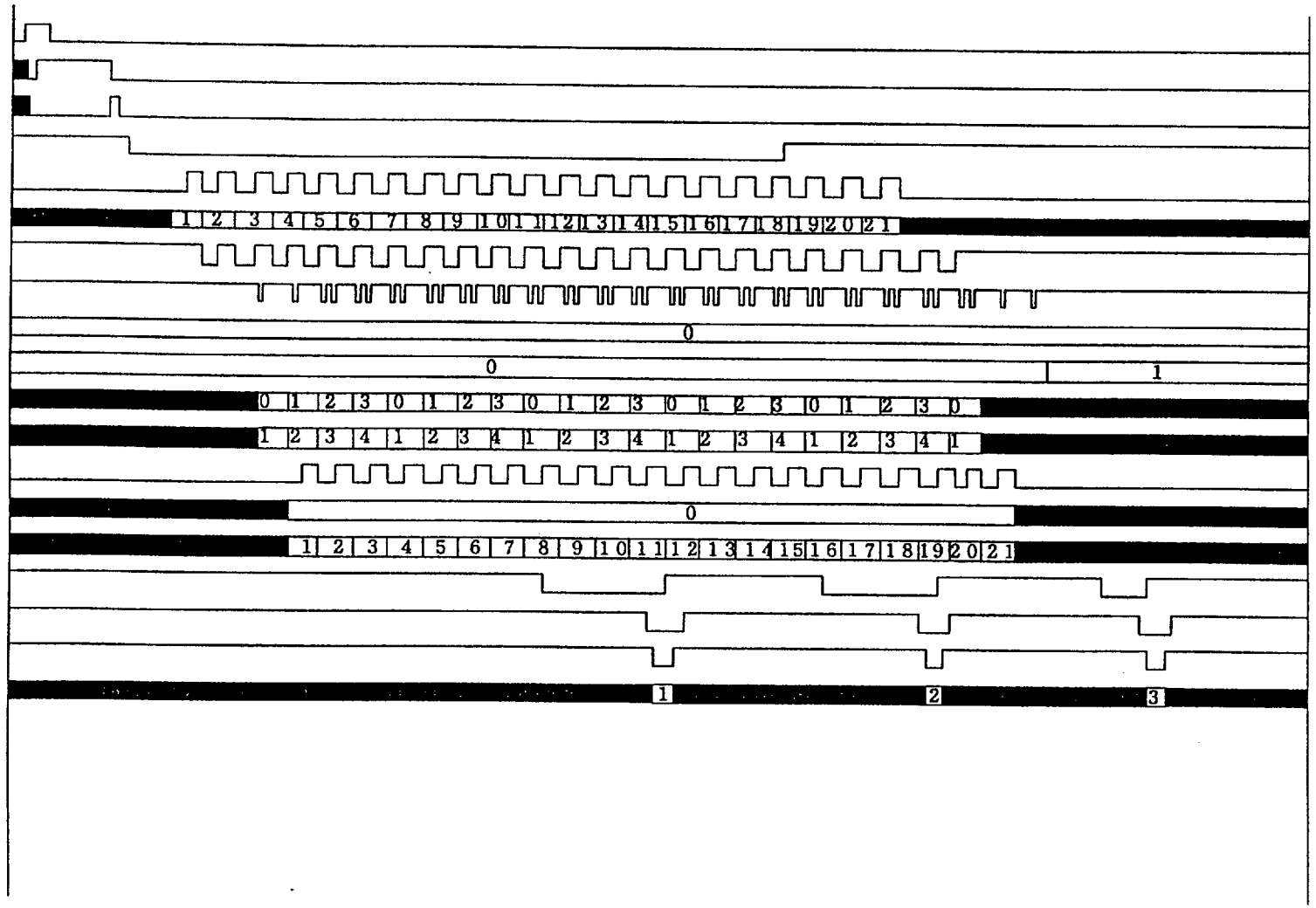


9. Line memory access



(Note) When accessing to the error data bank、pixel count+1 turns of R／W is necessary.
1st data is invalid,the 2nd data and succeeding one are valid.

10. DMA operation



Absolute maximum rating

Symbol	Parameters	Min.	Max.	Unit
VDD	Supply voltage	-0.3	6.7	V
VIN	Input voltage	-0.3	VDD+0.3	V
VOUT	Output voltage	-0.3	VDD+0.3	V
TSTG	Storage temperature	-55	125	℃
TLEAD	Soldering temperature(10 sec)		260	℃
TOPER	Operating temperature	0	70	℃

(All voltages are defined to Vss=0V)

〔Note 1〕 Parmanent damage may occur if Absolute maximum ratings are exeeded. Normal operation should be under the conditions of Electrical charact -eristics. If these conditions are exeeded, it may cause the LSI to malf -unction or affect the reliability of LSI.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Unit
VDD	Supply voltage	4.75	5	5.25	V
TA	Operating temperature	0		70	℃
IDD	Operating supply current(Note)			100	mA

(Note) Vdd=5V, No load

Electrical Specifications

■ DC characteristics

(Unless otherwize specified, Vdd=5V±5%, Ta=0～70℃)

Parameters	Symbol	pins	min.	typ.	max.	Unit	Cond.
Supply current	I_{DD}				100	mA	
HIGH level input voltage	V_{IH1}	MCLK, RCLK, VD7～VD0, VDEN, (TEST1N), (TEST2N)	0.7VDD	–	–	V	
	V_{IH2}	Other inpu-t pins	2.2	–	–	V	
LOW level input voltage	V_{IL1}	Same as V_{IH1}	–	–	0.3VDD	V	
	V_{IL2}	Same as V_{IH2}	–	–	0.8	V	
HIGH level output voltage	V_{OH}		3.5	–	–	V	V_{OH}=-2mA
LOW level output voltage	V_{OL}		–	–	0.5	V	V_{OL}= 8mA
Pull-up current	I_{PU}	DP5～DP0, (TEST1N), (TEST2N)	80	–	550	μA	V_{IN}=VSS
Pull-down current	I_{PD}	VPE	80	–	550	μA	V_{IN}=VDD
Leakage current	I_{LI}	Pins exept DP5～DP0, VPE, (TEST1N), (TEST2N)	-1		1	μA	

(Note) Measured at input/output levels are constant condition.

■ A C characteristics

No	Parameters	Pins	min.	typ.	max.	Unit	Cond.
1	MCLK cycle time(T) (Note 1)	MCLK	31			nS	
2	MCLK HIGH level width	MCLK	30%		70%	T	
3	MCLK LOW level width	MCLK	30%		70%	T	
4	CLK06 cycle time	CLK06		2		T	
5	CLK06 HIGH level width	CLK06		1		T	
6	CLK06 LOW level width	CLK06		1		T	
7	$\overline{CS}$ active setup time (to $\overline{WR}\downarrow$ or $\overline{RD}\downarrow$)	$\overline{CS}$	10			nS	
8	$\overline{CS}$ active hold time (to $\overline{WR}\uparrow$ or $\overline{RD}\uparrow$)	$\overline{CS}$	0			nS	
9	RA2～RA0 setup time (to $\overline{WR}\downarrow$)	RA2～RA0	10			nS	
10	RA2～RA0 hold time (to $\overline{WR}\uparrow$)	RA2～RA0	0			nS	
11	$\overline{WR}$ active pulsewidth	$\overline{WR}$	20			nS	
12	D7～D0 setup time (to $\overline{WR}\uparrow$)	D7～D0	20			nS	
13	D7～D0 hold time (to $\overline{WR}\uparrow$)	D7～D0	0			nS	
14	LEDC delay time(to $\overline{WR}\uparrow$)	LEDC			45	nS	C_L=50pF
15	LEDC delay time(to D3)	LEDC			35	nS	C_L=50pF
16	$\overline{LWR}$ delay time(to $\overline{WR}$)	$\overline{LWR}$			30	nS	C_L=20pF
17	LD7～LD0 delay time (to $\overline{WR}\downarrow$)	LD7～LD0			40	nS	C_L=20pF
18	LD7～LD0 delay time (to D7～D0)	LD7～LD0			30	nS	C_L=20pF
19	LD7～LD0 floating delay time (to $\overline{LWR}\uparrow$)	LD7～LD0	0			nS	
20	A13～A0 hold time (to $\overline{LWR}\uparrow$ or $\overline{LRD}\uparrow$)	A13～A0	0			nS	C_L=20pF

No.	Parameters	Pins	min.	typ.	max.	Unit	Cond.
21	D7～D0 delay time (to $\overline{RD}$↓)	D7～D0	0		40	nS	C_L=50pF
22	D7～D0 delay time (to LD7～LD0)	D7～D0			30	nS	C_L=50pF
23	D7～D0 floating delay time (to $\overline{RD}$↑)	D7～D0	0			nS	
24	$\overline{LRD}$ delay time (to $\overline{RD}$)	$\overline{LRD}$			25	nS	C_L=20pF
25	LD7～LD0 hold time (to $\overline{LRD}$↑)	LD7～LD0	0			nS	
26	A13～A0 setup time (to $\overline{LWR}$↓)	A13～A0	T-15			nS	C_L=20pF
27	A13～A0 hold time (to $\overline{LWR}$↑)	A13～A0	0			nS	
28	$\overline{LWR}$ active pulsewidth	$\overline{LWR}$	1			T	
29	LD7～LD0 setup time (to $\overline{LWR}$↓)	LD7～LD0	1			T	
30	LD7～LD0 hold time (to $\overline{LWR}$↑)	LD7～LD0	0			nS	
31	LD7～LD0 acceptable delay time(to A13～A0)	LD7～LD0			2T-30	nS	C_L=20pF (Note 2)
32	LD7～LD0 acceptable delay time (to $\overline{LRD}$↑)	LD7～LD0			2T-30	nS	C_L=20pF (Note 2)
33	A13～A0 hold time (to $\overline{LRD}$↑)	A13～A0	0			nS	
34	DP5～DP0 acceptable delay time (to DHA2～DHA0)(Note 3)	DP5～DP0			6T-75	nS	DHA2～DHA0 C_L=20pF
35	DCLK delay time (to MCLK↑)	DCLK			60	nS	C_L=50pF
36	DCLK LOW level width	DCLK		4		T	
37	DCLK HIGH level width	DCLK		4		T	
38	DOUT7～DOUT0 delay time (to MCLK↑)	DOUT7 ～DOUT0			60	nS	C_L=50pF

No.	Parameters	Pins	min.	typ.	max.	Unit	Cond.
39	DCLK delay time(Enlargem -ent) (to MCLK↑)	DCLK			60	nS	C_L=50pF
40	DCLK LOW level width (Enlargement)	DCLK		2		T	
41	DCLK HIGH level width (Enlargement)	DCLK		2		T	
42	$\overline{DREQ}$↓ delay time (to MCLK↑)	$\overline{DREQ}$			65	nS	C_L=50pF
43	$\overline{DREQ}$↑ delay time (to $\overline{RD}$↓)	$\overline{DREQ}$			40	nS	C_L=50pF
44	$\overline{DACK}$↑ setup time (to $\overline{RD}$↓)	$\overline{DACK}$	0			nS	
45	$\overline{DACK}$↑ hold time (to $\overline{RD}$↑)	$\overline{DACK}$	0			nS	
46	D7～D0 delay time (to $\overline{RD}$↓)	D7～D0	0		45	nS	C_L=50pF
47	D7～D0 floating delay time (to $\overline{RD}$↑)	D7～D0	0			nS	
48	TRIG setup time (to MCLK↑)	TRIG	10			nS	
49	TRIG hold time (to MCLK↓)	TRIG	4			nS	
50	TRIG active pulsewidth	TRIG	2			T	
51	CLK06 delay time (to MCLK↑)	CLK06	0		40	nS	C_L=50pF
52	VPE setup time (to SH↑)	VPE	30			nS	SH C_L=50pF
53	VPE hold time (to SH↑)	VPE	0			nS	
54	SH delay time(to MCLK↑)	SH			40	nS	C_L=50pF
55	SH active pulsewidth	SH		16		T	
56	TRIG06 delay time (to MCLK↑)	TRIG06			40	nS	C_L=50pF
57	TRIG06 active pulsewidth	TRIG06		2		T	

No.	Parameters	Pins	min.	typ.	max.	Unit	Cond.
58	CLK1 delay time (to MCLK↑)	CLK1			40	nS	C_L=50pF
59	CLK1 LOW level width	CLK1		8		T	
60	CLK1 HIGH level width	CLK1		8		T	
61	CLK2 delay time (to MCLK↑)	CLK2			40	nS	C_L=50pF
62	CLK2 HIGH level width	CLK2		8		T	
63	CLK2 LOW level width	CLK2		8		T	
64	CLKR(A) delay time (to MCLK↑)	CLKR			35	nS	C_L=50pF (Note 4)
65	CLKR HIGH level width	CLKR		1		T	
66	CLKR LOW level width	CLKR		7		T	
67	CLKR(B) delay time (to MCLK↑)	CLKR			40	nS	C_L=50pF (Note 4)

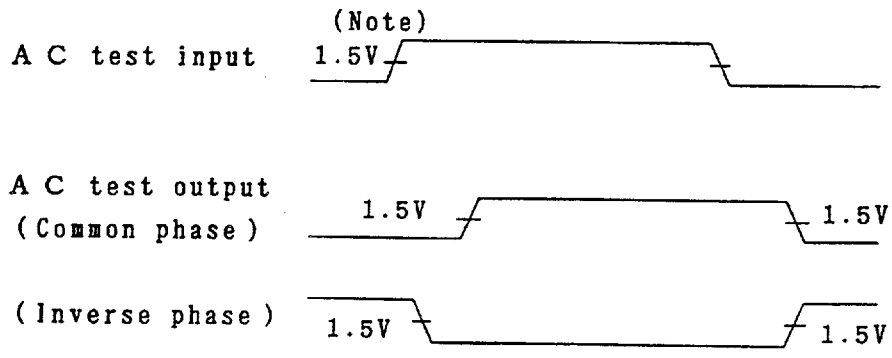
(Note 1) MCLK cycle time is defined as T.

(Note 2) SRAM for the line memory.

(Note 3) ROM, PLD for dither pattern.

(Note 4) As for CLKR(A), CLKR(B), refer to "Registers"

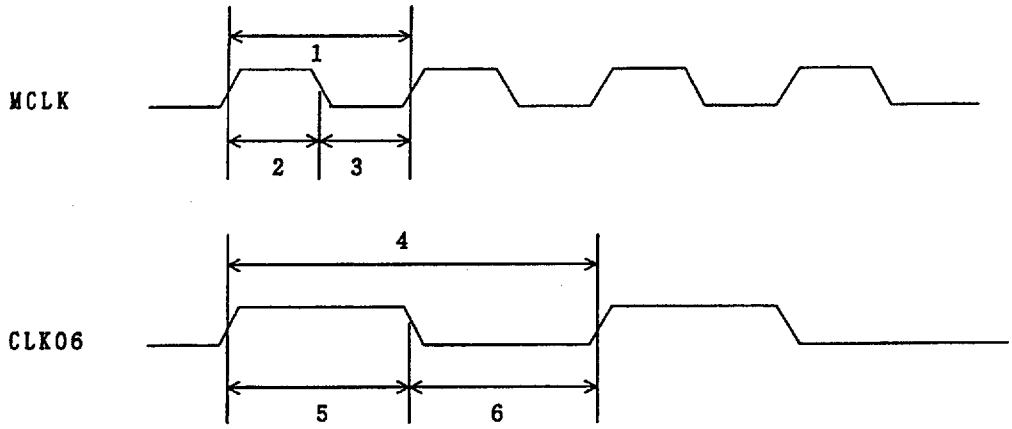
- Measurement conditions



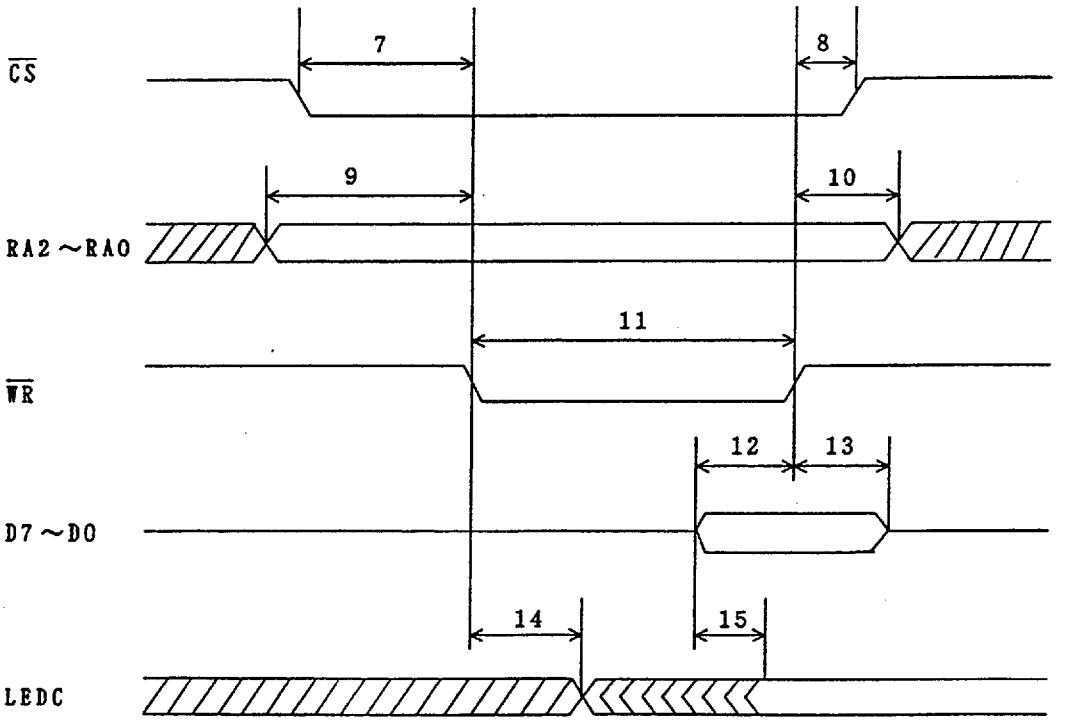
(Note) VDD/2 (In case of CMOS level input)

■ Timing specifications

1. Clocks

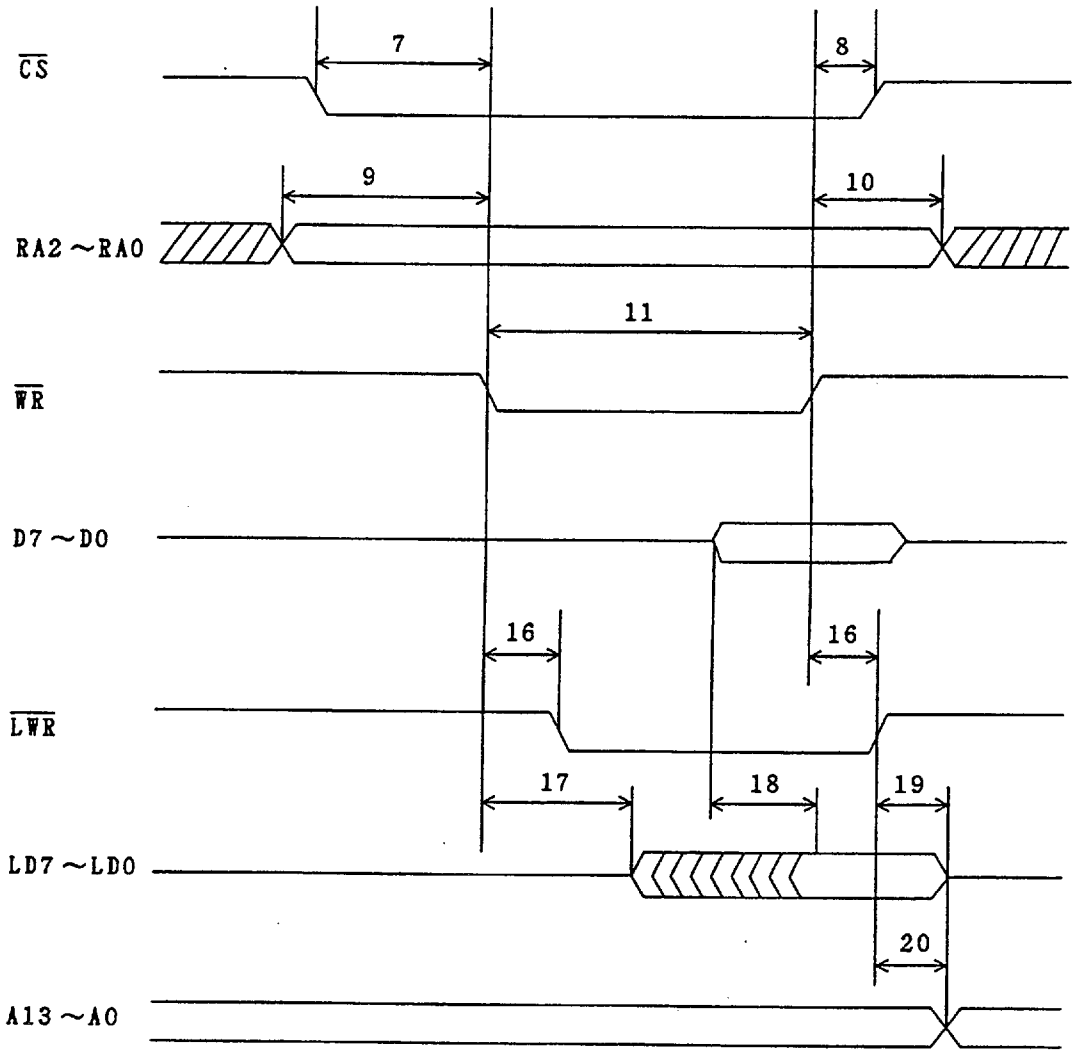


2. CPU interface relateted

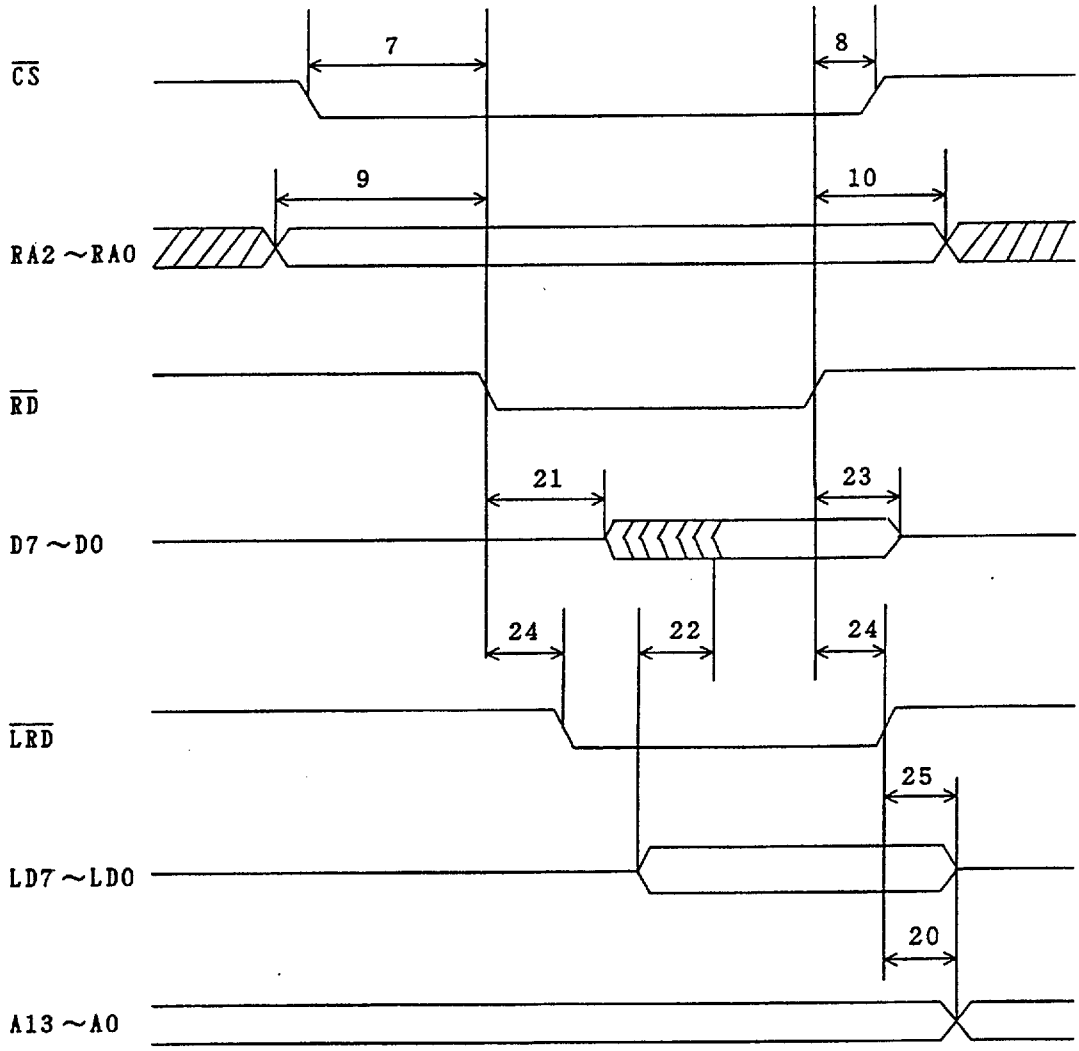


3. Line memory interface related

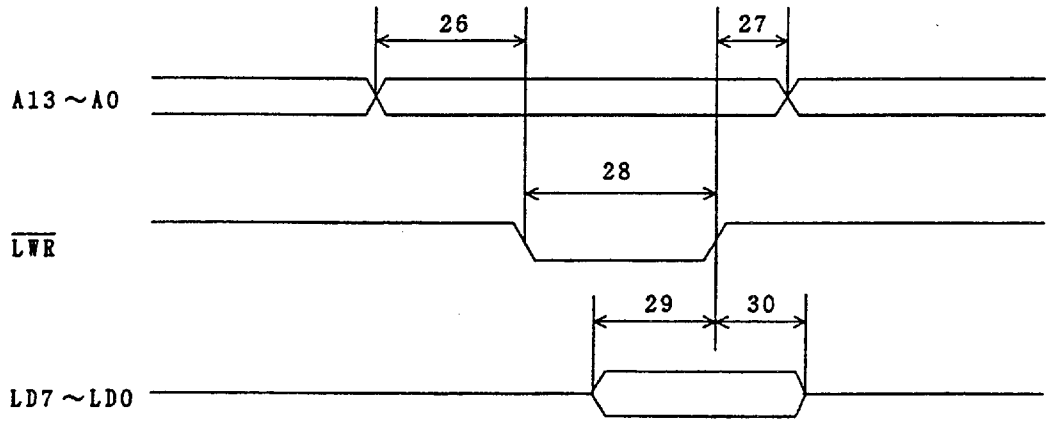
3-1. Line memory access(write)



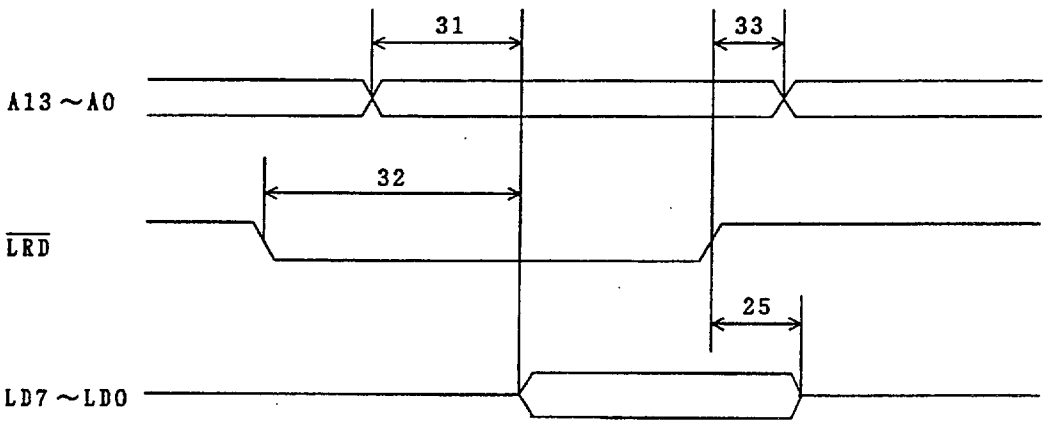
3-2. Line memory access(read)



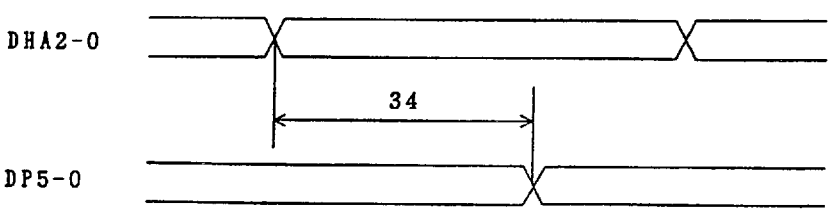
3-3. Bi-level image processing mode(line memory write)



3-4. Bi-level image processing mode(line memory read)

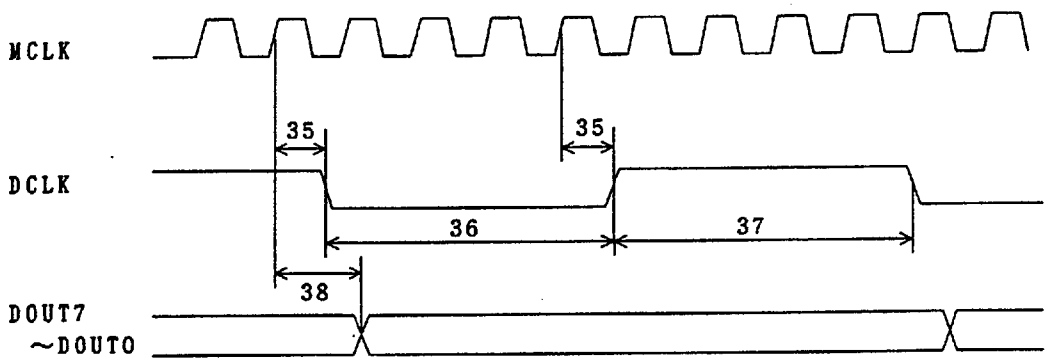


4. ROM or PLD(for dither pattern) interface related

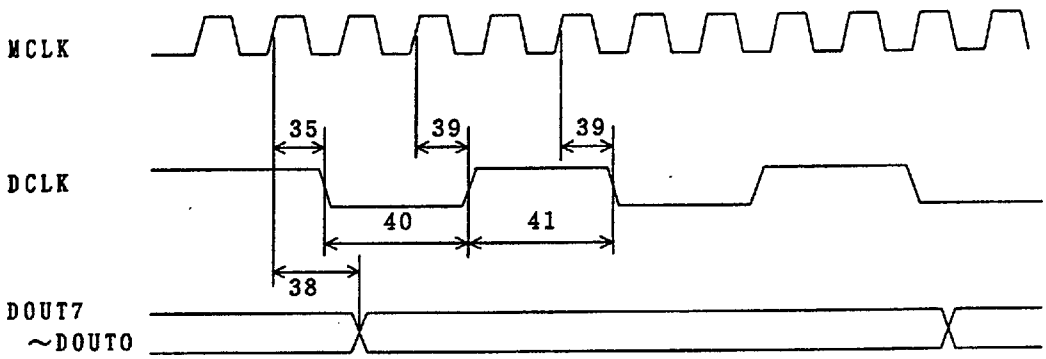


5. Serial output interface

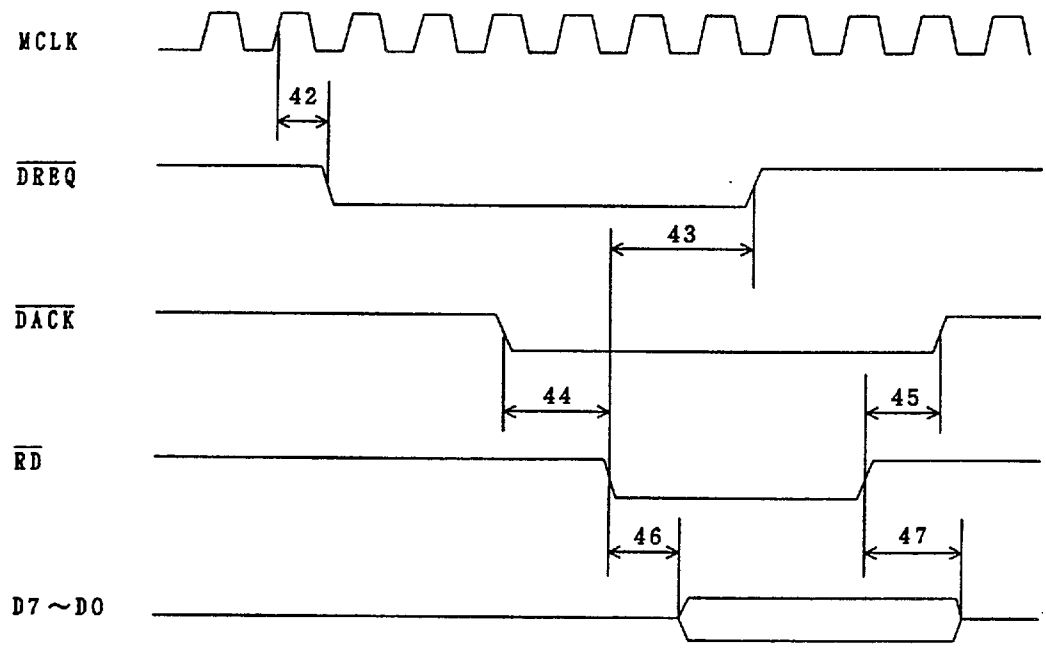
5-1. No enlargement/reduction



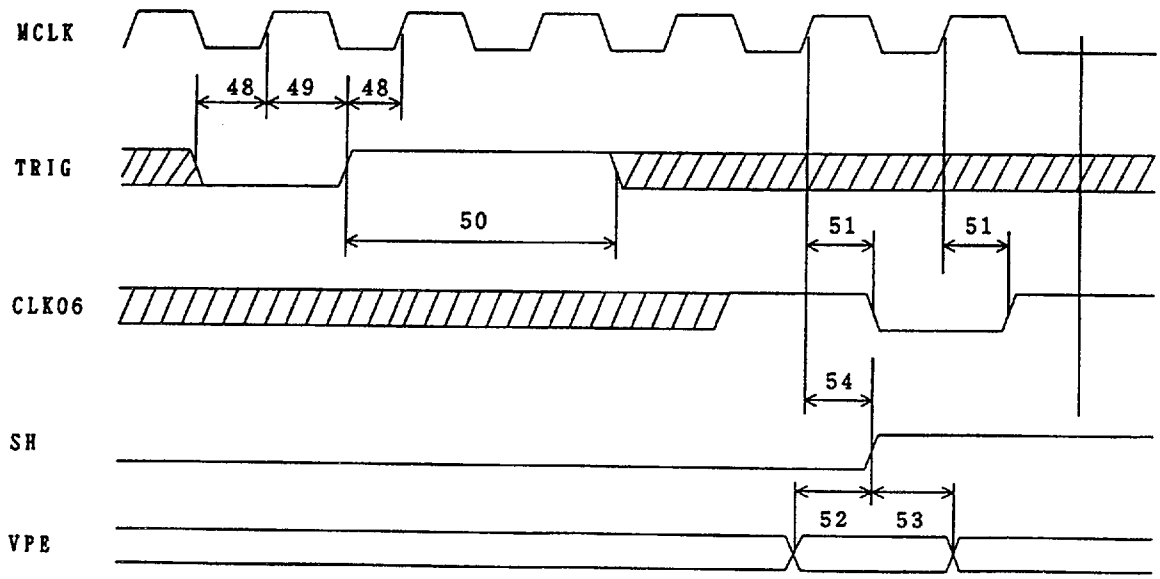
5-2. Enlargement



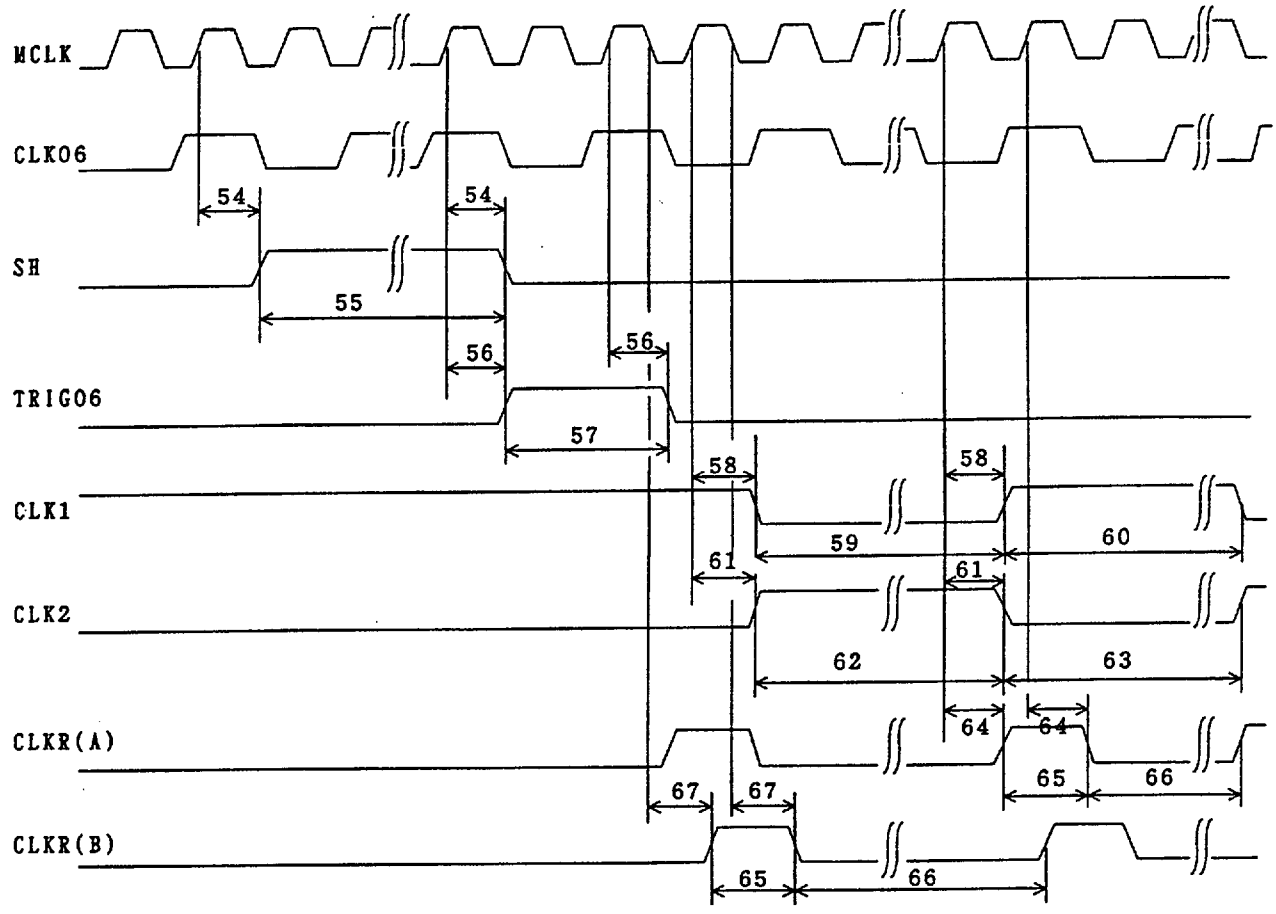
6. DMA interface



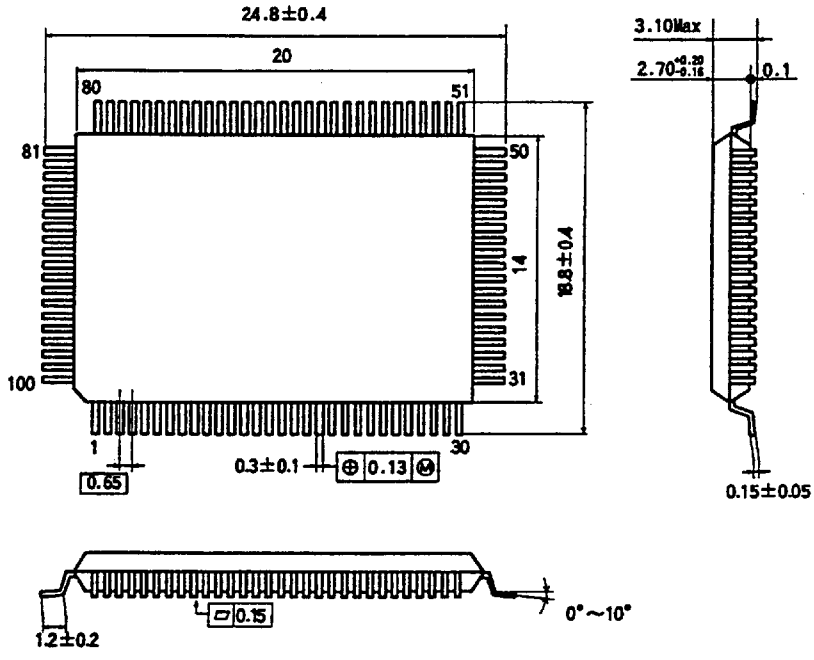
7. TRIG, VPE and CLK06



8. S H, T R I G 0 6, C C D related timing



Package


24.8±0.4
20
80
51
81
50
14
18.8±0.4
100
31
1
30
0.65
0.3±0.1
0.13
M
3.10Max
2.70
0.1
0.15±0.05
0.15
1.2±0.2
0°~10°

Products and product specifications mentioned in this data sheet are subject to change without notice due to product improvements. Please understand that ASAHI KASEI MICROSYSTEMS Co., Ltd. (AKM) shall not be held liable for the results of using this product under conditions other than those specified in this data sheet.
Also, please note that this company shall not be held liable for infringement of patent rights, industrial ownership or other rights of any third party regarding the use of information or drawings included in this data sheet.
Furthermore, in the case that the product described in this data sheet is specified as a strategic product under the provisions of the foreign exchange and foreign trade control laws of Japan (including services), it is necessary to obtain an export permit in accordance with the specified laws in the event of import.

AKM

ASAHI KASEI MICROSYSTEMS CO., LTD.

2001 GATEWAY PLACE
SUITE 195 EAST
SAN JOSE, CALIFORNIA 95110 USA
TELEPHONE (408) 436-8580
FACSIMILE (408) 436-7591

TS BUILDING
24-10 YOYOGI 1-CHOME
SHIBUYA-KU, TOKYO, 151, JAPAN
TELEPHONE (03) 3320-2067
FACSIMILE (03) 3320-2072