CLF11 Series Compact Linear Flash Memory Card 8, 16 and 32 MB (Intel Strata Flash)

GENERAL DESCRIPTION

The CLF11 Series Compact Flash memory cards offer a low cost linear Flash solid state storage solution for code and data storage, high performance disk emulation, mobile PC and embedded applications.

CLF11 series cards offer memory capacities from 8MB to 32MB, with 256kB (2x128kB) block erase size.

It is based on Intel MLC, Strata Flash memories. Cards are based on the J3 families of memory components: built with: 28F128J3, 28F640J3, 28F320J3

These flash devices support the Common Flash Interface (CFI) programming algorithm, a standard that allows system level software to evaluate the flash configuration, electrical characteristic, programming parameters and supported functions. CFI is intended to support future upgrades with universal programming algorithms, so there is no longer a need for continued programming software modification and updates. Systems should be able to recognize and support all devices to allow universal expansion/upgrade path.

The symmetrically blocked architecture and single supply (universal 3.3V or 5V for CLF11 cards) operation provides a cost effective, high performance, nonvolatile storage solution. The Compact Flash Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

The CLF11 series is designed as a simple x16 linear array of Flash devices. Two Flash devices provide the lower and upper bytes for the 16 bit access. (See Functional Truth Table on page 5)

WEDC's standard cards are shipped with blank housings . Please contact WEDC sales representative for further information on Custom artwork.

FEATURES

- Small Form Factor: CF compatible
  - 36.4 x 42.8 x 3.3 mm
- Low cost Linear Flash Card
- Single Supply Operation
  - 5V or 3.3V (Note 1)
- Fast Read Performance
  - 200ns Maximum Access Time
- Based on MLC J3 Strata Flash Components
- Common Flash Interface (CFI) compliant
- Erase sector size: 2x 128kB
- High Performance Random Writes
  - 6µs Typical per Byte Write Time, using 32Byte Write buffer
- Automated Write and Erase Algorithms
- High Write/Erase Endurance:
  100,000 Write/Erase Cycles
- Low Power Consumption
  - 150µA Standby Current
  - 75mA Max Byte Write Current

Note 1:
CLF11 supports wide, universal operating voltage: 3V to 5V.

That means the card will work in 3.3V systems as well as in 5V systems. This feature may allow easy exchange of data between multiple and different systems and provide easy upgrade / expansion path.

CLF BLOCK DIAGRAM

MANUFACTURER AND DEVICE ID CODES

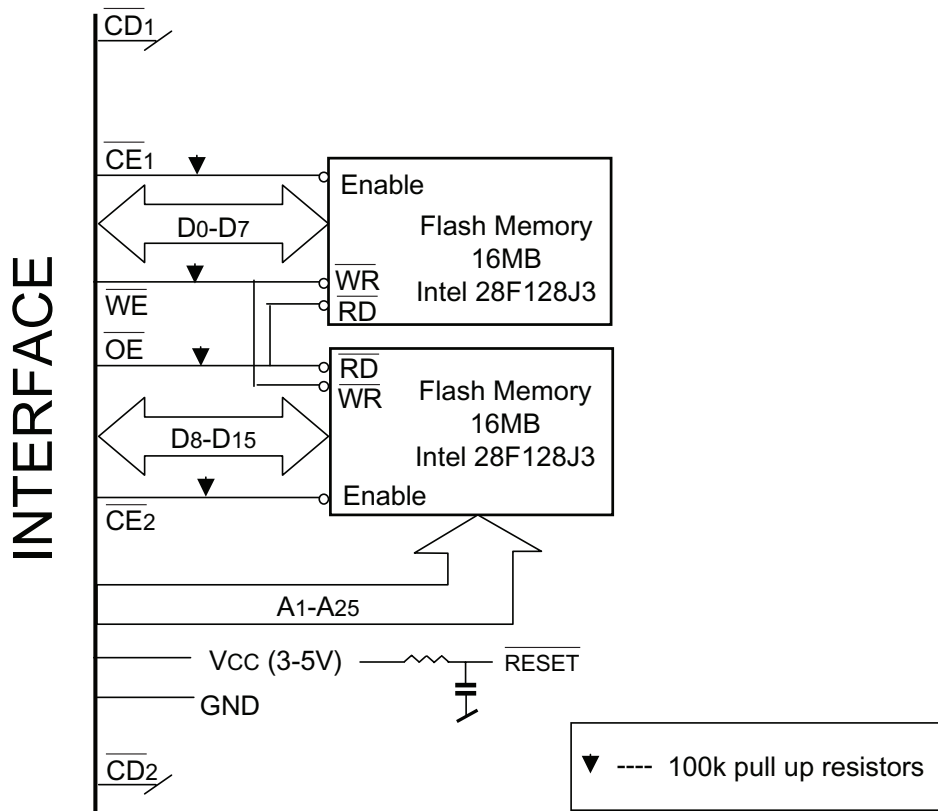| Device	Manuf ID	Device ID
Int 28F128J3	89h	18h
Int 28F640J3	89h	17h
Int 28F320J3	89h	16h

FIG 1. BLOCK DIAGRAM FOR 32MB CARD

Notes:
1. A25..23 pulled down by 100kW resistors
2. Open for FVF0x; GND for FVF1x (3.3V operation)

Other configurations available: 8MB, 16MB, 16 bit only access, etc.
Please contact sales department for more information

For information regarding modes of operation, commands, and programming details for the memory components, please consult the Intel StrataFlash J3 data sheet.

http://developer.intel.com/design/flcomp/datashts/290667.htm

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register, and, when $V_{PEN} = V_{PENH}$, block erasure, program, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Block Lock-Bit commands require the command and block within the device to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when the device is enabled and $\overline{WE}$ is active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or the first edge of $\overline{CE}_1$ or $\overline{CE}_2$ that disables the card. Standard microprocessor write timings are used.

PINOUT

Pin	Signal name	I/O	Function	Active		Pin	Signal name	I/O	Function	Active
1	GND		Ground			26	$\overline{CD}_1$	O	Card Detect 1	LOW
2	DQ_3	I/O	Data bit 3			27	DQ_{11}	I/O	Data bit 11	
3	DQ_4	I/O	Data bit 4			28	DQ_{12}	I/O	Data bit 12	
4	DQ_5	I/O	Data bit 5			29	DQ_{13}	I/O	Data bit 13	
5	DQ_6	I/O	Data bit 6			30	DQ_{14}	I/O	Data bit 14	
6	DQ_7	I/O	Data bit 7			31	DQ_{15}	I	Data bit 15	
7	$\overline{CE}_1$	I	Card enable 1	LOW		32	$\overline{CE}_2$	I	Card enable 2	LOW
8	A_{11}	I	Address bit 10			33	A_{22}	I	Address bit 22	
9	$\overline{OE}$	I	Output enable	LOW		34	A_{21}	I	Address bit 21	
10	A_{10}	I	Address bit 11			35	A_{20}	I	Address bit 20	
11	A_9	I	Address bit 9			36	$\overline{WE}$	I	Write Enable	LOW
12	A_8	I	Address bit 8			37	A_{24}	I	Address bit 24	
13	V_{CC}		Supply Voltage			38	V_{CC}		Supply Voltage	
14	A_7	I	Address bit 7			39	A_{19}	I	Address bit 19	
15	A_6	I	Address bit 6			40	A_{18}	I	Address bit 18	
16	A_5	I	Address bit 5			41	A_{23}	I	Address bit 23	
17	A_4	I	Address bit 4			42	A_{17}	I	Address bit 17	
18	A_3	I	Address bit 3			43	A_{16}	I	Address bit 16	
19	A_2	I	Address bit 2			44	A_{15}	I	Address bit 15	
20	A_1	I	Address bit 1			45	A_{14}	I	Address bit 14	
21	DQ_0	I/O	Data bit 0			46	A_{13}	I	Address bit 13	
22	DQ_1	I/O	Data bit 1			47	DQ_8	I/O	Data bit 8	
23	DQ_2	I/O	Data bit 2			48	DQ_9	I/O	Data bit 9	
24	A_{12}	I	Address bit 12			49	DQ_{10}	O	Data bit 10	
25	$\overline{CD}_2$	O	Card Detect 2	LOW		50	GND		Ground	LOW

Notes:
16 bit operation; using 2 independent Low and High byte enables: single byte access ability

MECHANICAL
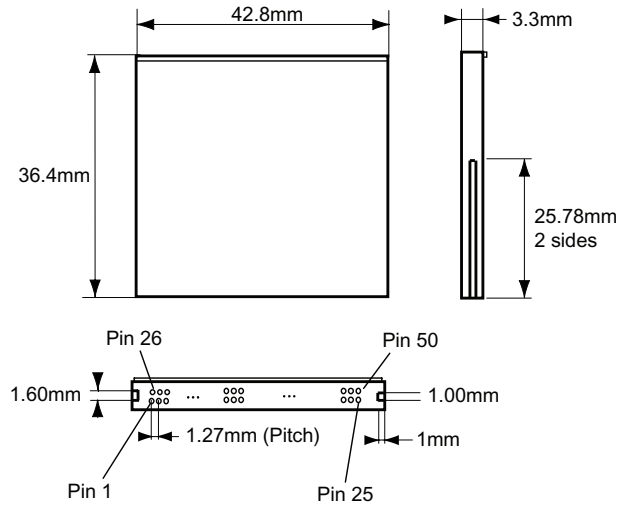
CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A_1 - A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64MB of memory on the card
DQ_0 - DQ_{15}	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 THROUGH DQ_{15} constitute the bi-directional databus. DQ_0 - DQ_7 constitute the lower (even) byte and DQ_8 - DQ_{15} the upper (odd) byte. DQ_{15} is the MSB.
$\overline{CE}_1$	INPUT	**CARD ENABLE 1:** $\overline{CE}_1$ enables card accesses (See below the Functional Truth Table).
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Active low signal enabling read data from the memory card.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
CD_1, CD_2	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
V_{CC}		**CARD POWER SUPPLY:** (5.0V for FVF0x or 3V to 5V for FVF1x)
GND		**GROUND:**

FUNCTIONAL TRUTH TABLE

Function Mode	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{OE}$	$\overline{WE}$	D_{15}-D_8	D_7-D_0
Standby Mode	H	H	X	X	High-Z	High-Z
Output Desible	L	L	H	H	High-Z	High-Z
Read Function LOW Byte Access (8 bits)	H	L	L	H	High-Z	**Even-Byte Out**
Read Function HIGH Byte Access (8 bits)	L	H	L	H	**Odd-Byte Out**	High-Z
Read Function Word Access (16 bits)	L	L	L	H	**Odd-Byte Out**	**Even-Byte Out**
WRITE function LOW Byte Access (8 bits)	H	L	H	L	XX	**Even-Byte In**
WRITE function HIGH Byte Access (8 bits)	L	H	H	L	**Odd-Byte In**	XX
WRITE function Word Access (16 bits)	L	L	H	L	**Odd-Byte In**	**Even-Byte In**

COMMAND DEFINITIONS TABLE
(THE COMMAND DEFINITIONS FOR STRATA FLASH MEMORY)

Command Code Sequence	Bus Cyc.	1st Bus Cycle			2nd Bus Cycle		
		Bus Opr	Addr	Data	Bus Opr	Addr	Data
Read Array	1	WR	X	FFh			
Read Identifier Codes	2	WR	X	90h	RD	IA	ID
Read Status Register	2	WR	X	70h	RD	X	SRD
Clear Status Register	1	WR	X	50h			
Block Erase	2	WR	BA	20h	WR	BA	D0h
Word/Byte Write	2	WR	WA	40h or 10h	WR	WA	WD
Erase/Write Suspend	1	WR	X	B0h			
Erase/Write Resume	1	WR	X	D0h			

ABSOLUTE MAXIMUM RATINGS [1]

Operating Temperature TA (ambient)	
Commercial	0°C to +70 °C
Industrial	-40°C to +85 °C
Storage Temperature	55°C to +110 °C
Voltage on any pin relative to Vss	-0.5V to Vcc+0.5V

Notes:

1. Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS
VCC SUPPLY VOLTAGE 3V - 5V

Symbol	Parameter	Notes	Typ	Max	Units	Test Conditions
I_{CCR}	Vcc Read Current 16 bit mode	Vcc = 3.3V Vcc = 5.0V	35 45	55 65	mA	Vcc = Vcc MAX tcycle = 200ns
I_{CCW}	Vcc Program Current	Vcc = 3.3V Vcc = 5.0V	35 40	60 70	mA	1 device active
I_{CCE}	Vcc Erase Current	Vcc = 3.3V Vcc = 5.0V	35 40	70 80	mA	1 device active
I_{CCSL}	Vcc Sleep Current	Per 2 devices	160	250	µA	Vcc = 3.3V Control Signals = Vcc Reset = V_{IH} (active)
I_{CCS}	Vcc Standby Current	Per 2 devices TTL inputs		300	µA	Vcc = 3.3V Control Signals = V_{IH} Reset = V_{IL} (not active)

Notes:
CMOS Test Conditions: V_{IL} = Vss ± 0.2V, V_{IH} = Vcc ± 0.2V

V_{CC} SUPPLY VOLTAGE 3V - 5V

V_{CC} SUPPLY VOLTAGE 3V - 5V

| Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{IL}	Input Leakage Current	1, 2		±20	µA	$V_{CC} = V_{CC}MAX$ $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1		±20	µA	$V_{CC} = V_{CC}MAX$ $V_{OUT} = V_{CC}$ or V_{SS}
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	1	2.4	3.2	V	I_{OH} = -2.0mA
V_{LKO}	Vcc Erase/Program Lockout Voltage		1	2.0	V	

Notes:
1. Values are the same for all card densities.
2. Exceptions: Leakage currents on $\overline{CE_1}$, $\overline{OE}$ and $\overline{WE}$ will be < 500 µA when V_{IN} = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when $V_{IN}=V_{CC}$ due to internal pull-down resistor.

AC CHARACTERISTICS
READ TIMING PARAMETERS [1]

SYMBOL(PCMCIA)	Parameter	200ns		Unit
		Min	Max	
$t_C(R)$	Read Cycle Time	200		ns
$t_a(A)$	Address Access Time		200	ns
$t_a(CE)$	Card Enable Access Time		200	ns
$t_a(OE)$	Output Enable Access Time		100	ns
$t_{su}(A)$	Address Setup Time		20	ns
$t_{su}(CE)$	Card Enable Setup Time		0	ns
$t_h(A)$	Address Hold Time		20	ns
$t_h(CE)$	Card Enable Hold Time		20	ns
$t_v(A)$	Output Hold from Address Change		0	ns
$t_{dis}(CE)$	Output Disable Time from $\overline{CE}$		90	ns
$t_{dis}(OE)$	Output Disable Time from $\overline{OE}$		90	ns
$t_{en}(CE)$	Output Enable Time from $\overline{CE}$	5		ns
$t_{en}(CE)$	Output Enable Time from $\overline{OE}$	5		ns
$t_{rec}(RST)$	Power Down recovery to Output Delay. Vcc = 5V		500	ns

READ TIMING DIAGRAM
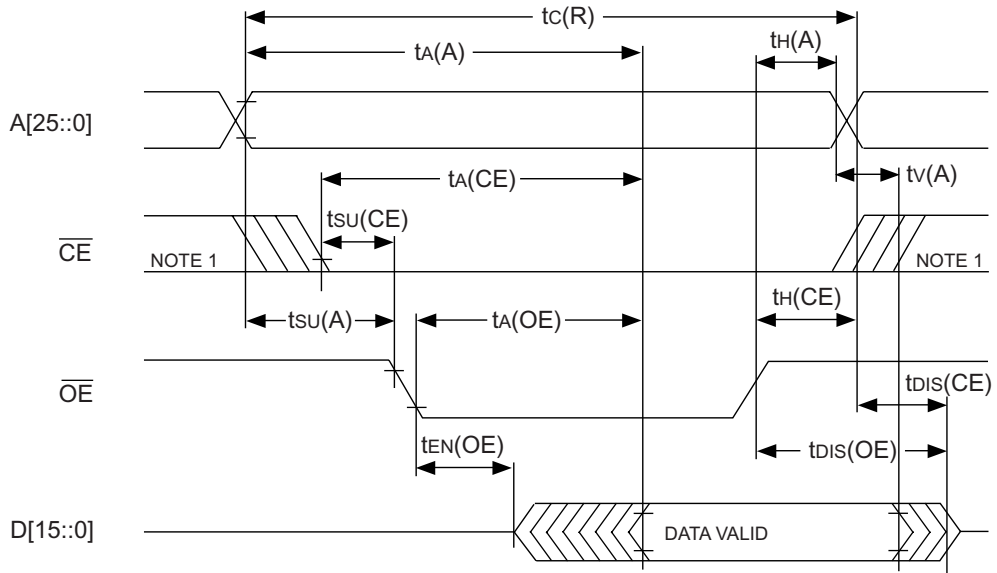
Note: *Signal may be high or low in this area.*

WRITE TIMING PARAMETERS

SYM (PCMCIA)	Parameter	200ns		Unit
		Min	**Max**	
tcW	Write Cycle Time	200		ns
tw(WE)	Write Pulse Width	120		ns
tsu(A)	Address Setup Time	20		ns
tsu(A-WEH)	Address Setup Time for $\overline{WE}$	140		ns
tsu(CE-WEH)	Card Enable Setup Time for $\overline{WE}$	140		ns
tsu(D-WEH)	Data Setup Time for $\overline{WE}$	60		ns
tH(D)	Data Hold Time	30		ns
tREC(WE)	Write Recover Time	30		ns
tDIS(WE)	Output Disable Time from $\overline{WE}$		90	ns
tDIS(OE)	Output Disable Time from $\overline{OE}$		90	ns
tEN(WE)	Output Enable Time from $\overline{WE}$	5		ns
tEN(OE)	Output Enable Time from $\overline{OE}$	5		ns
tsu(OE-WE)	Output Enable Setup from $\overline{WE}$	10		ns
tH(OE-WE)	Output Enable Hold from $\overline{WE}$	10		ns
tsu(CE)	Card Enable Setup Time from $\overline{OE}$	0		ns
tH(CE)	Card Enable Hold Time	20		ns

WRITE TIMING DIAGRAM
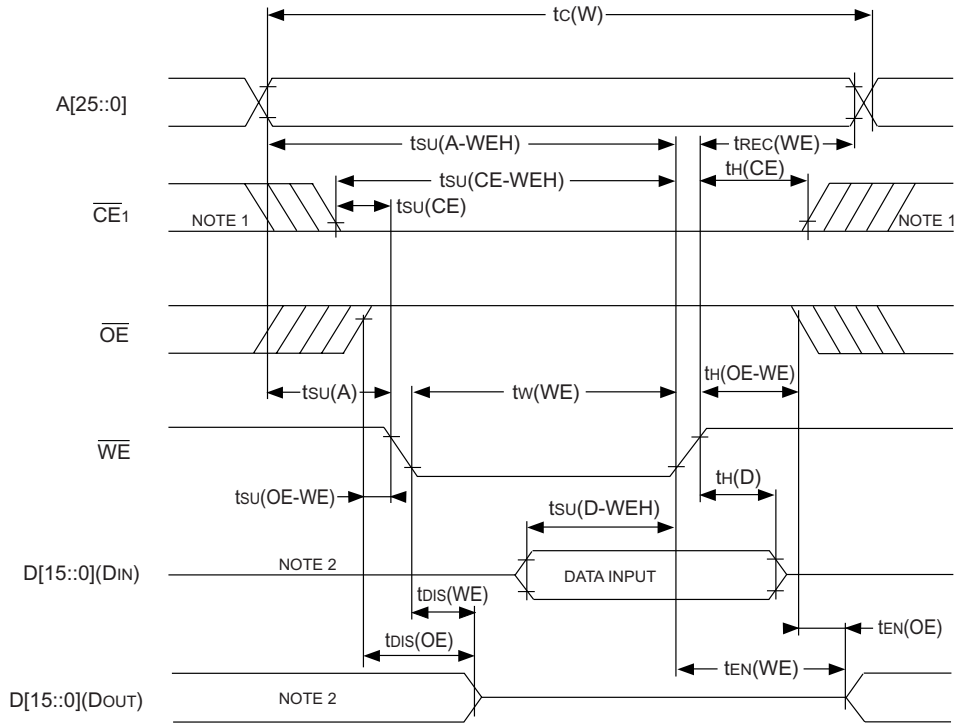
Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

DATA WRITE AND ERASE PERFORMANCE[1,2,3]
CLF11: V_{CC} = 3V-5V

Parameter	Notes	Min	Typ[1]	Max	Units
Write Buffer Byte program time(time to prog. 32Bytes/16Words)	- J3 device		200		µs
Byte Program time - Using Word/Byte prog command	- J3 device		180		µs
Block Program Time128kB written using Write to Buffer	- J3 device		0.8		sec
Block Erase Time	- J3 device		0.7		sec

Notes:
1. Typical: Nominal voltages and T_A = 25°C.
2. Excludes system overhead.
3. Valid for all speed options.

PRODUCT MARKING

```
                              EDI
                    WED  7P032CLF1101C20  C995  9915
```

COMPANY NAME

PART NUMBER

LOT CODE/TRACE NUMBER

DATE CODE

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

```
                              7  P  032  CLF11  01  C  20
```

CARD TECHNOLOGY
  7 FLASH
  8 SRAM

PC CARD
  P Standard PCMCIA/Compact Flash

CARD CAPACITY
  032 32MB

CARD FAMILY AND VERSION
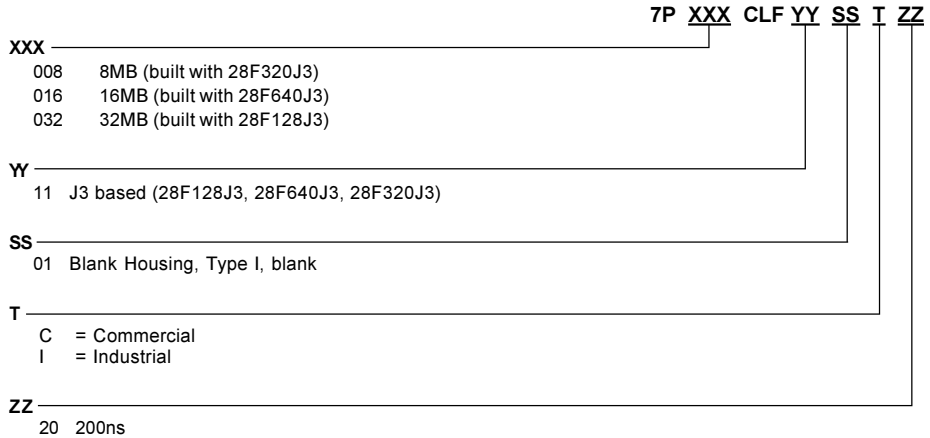 - See Card Family and Version Info. for details (next page)

PACKAGING OPTION
  01 Standard, Blank CF

TEMPERATURE RANGE
  C = Commercial   0°C to +70°C
  I = Industrial   -40°C to +85°C

CARD ACCESS TIME
  20 200ns

WHITE ELECTRONIC DESIGNS

ORDERING INFORMATION

                                        7P XXX CLF YY SS T ZZ

XXX
    008   8MB (built with 28F320J3)
    016   16MB (built with 28F640J3)
    032   32MB (built with 28F128J3)

YY
    11   J3 based (28F128J3, 28F640J3, 28F320J3)

SS
    01   Blank Housing, Type I, blank

T
    C   = Commercial
    I   = Industrial

ZZ
    20   200ns

PART NUMBER TABLE - COMMON OPTIONS

INTEL STRATA FLASH BASED CARDS

WEDC Part Number	Density	Speed	Flash Component
7P016CLF1101C20	8MB	200ns	28F320J3
7P032CLF1101C20	16MB	200ns	28F640J3
7P064CLF1101C20	32MB	200ns	28F128J3
7P016CLF1101I20	8MB	200ns	28F320J3
7P032CLF1101I20	16MB	200ns	28F640J3
7P064CLF1101I20	32MB	200ns	28F128J3

Notes:
1. Other options, including density, architecture and speed are available, please contact your WEDC sales representative with your request.

WHITE ELECTRONIC DESIGNS

Document Title

Compact Linear Flash Memory Card - CLF11 Series

Revision History

Rev level	Description	Date
rev 0	Initial release	February, 2001
rev 1	Add separate enable for LOW and HIGH bytes	February, 2001
rev 2	Final release	October, 2001
rev 3	Industrial temp. added	May, 2003