Description

The μPD9306 and μPD9306A hard-disk interface (HDI) chips are unique CMOS single-chip support devices intended for use with the μPD7261A hard-disk controller. The μPD9306/A includes a high-performance, digital phase-locked loop (DPLL), write precompensation logic, and μPD7261A CLK and R/W CLK generation. The μPD9306/A requires only two inexpensive passive delay lines and a crystal for the self-contained oscillator. It provides a simple but effective solution to the design of support circuitry for typical hard-disk controllers utilizing the ST-506 type interface. Due to its fast acquisition time, the μPD9306/A can actually provide increased storage by allowing for a size reduction in the sync field areas. The HDI also significantly reduces board area requirements and overall design time. The schematic examples included in this data sheet can be used to reduce the ST-506 interface design time to a few hours.

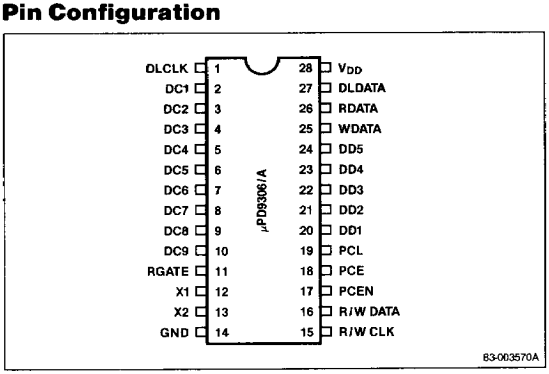
Features

- ☐ Unique digital phase-locked loop (no adjustments)
- ☐ Precompensation logic
- ☐ 5-MHz MFM data rate
- ☐ Internal crystal oscillator
- ☐ CMOS technology
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type
μPD9306C / μPD9306AC	28-pin plastic DIP

Pin Configuration



Pin Identification

No.	Symbol	Function
1	DLCLK	Delay line clock output
2–10	DC1–DC9	Delay clock inputs
11	RGATE	Read gate input
12	X1	Crystal clock input
13	X2	Crystal clock output
14	GND	Ground
15	R/W CLK	Read / write clock output
16	R/W DATA	Read / write data input / output
17	PCEN	Precompensation enable input
18	PCE	Precompensation early input
19	PCL	Precompensation late input
20–24	DD1–DD5	Delayed data inputs
25	WDATA	Write data output
26	RDATA	Read data input
27	DLDATA	Delay line data output
28	V_{DD}	+5 V power supply

6

Pin Functions

DC1–DC9 (Delayed Clock)

These nine inputs receive clock signals delayed relative to DLCLK. The delays for pins DC1–DC9 are 10 ns to 90 ns in 10 ns increments.

DD1–DD5 (Delayed Data)

These five inputs receive the input data signals, delayed relative to DLDATA. The delays for pins DD1–DD5 are 40, 60, 80, 90, and 100 ns respectively. As an option, DD1 and DD2 may be connected to the 30-ns and 70-ns taps, respectively, of delay line 1. Comparative performance data is shown in table 1.

DLDATA (Delay Line Data)

This output supplies the external delay line with processed read data from the disk or processed write data from the host.

DLCLK (Delay Line Clock)

This pin is used for the output clock of the on-chip oscillator and to supply clocks for both the delay line and the μPD7261A.

RGATE (Read Gate)

When this input is active, the digital phase-locked loop (DPLL) circuit generates a read/write clock that is synchronized to the phase of the read data from the disk.

R/W CLK (Read/Write Clock)

When RGATE is active, the DPLL selects one clock input from DLCLK or DC1–DC9. The clock input is synchronized with the read data at the R/W DATA pin and output via R/W CLK. When RGATE is inactive, the DPLL outputs the previously selected clock.

R/W DATA (Read/Write Data)

This pin outputs read data that has been synchronized with R/W CLK when RGATE is high. This pin inputs write data when RGATE is low.

RDATA (Read Data)

Input for read data from the hard-disk drive.

WDATA (Write Data)

Output for write data to the hard-disk drive. Precompensation is according to PCE, PCL, and PCEN states.

PCEN (Precompensation Enable)

Write precompensation is performed when this input signal is active.

PCE (Precompensation Early)

When PCE and PCEN are active, write data is advanced in phase from its nominal position and output on the WDATA pin. External delay lines determine the amount of time advance.

PCL (Precompensation Late)

When PCL and PCEN are active, write data is delayed in phase from its nominal position and output on the WDATA pin. External delay lines determine the amount of time delay.

X1, X2 (Crystal)

These two pins connect the crystal to the on-chip oscillator and clock generator.

V_{DD} (Power Supply)

+5 V power supply input.

GND (Ground)

Ground.

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.5 to +7.0 V (Note 1)
Input voltage, V_I	−0.5 to +7.0 V (Note 1)
Output current, I_O	10 mA
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Note:
(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +5.0\,V \pm 10\%$ unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH}	2.0		$V_{DD}+0.5$	V	9306 only
	V_{IH1}	2.0		$V_{DD}+0.5$	V	(Note 3)
	V_{IH2}	$0.7V_{DD}$		$V_{DD}+0.5$	V	(Note 4)
Input voltage low	V_{IL}	−0.5		+0.8	V	9306 only
	V_{IL1}	−0.5		+0.8	V	(Note 3)
	V_{IL2}	0		$0.3V_{DD}$	V	(Note 4)
Output voltage high	V_{OH1}	$V_{DD}-0.4$			V	$I_{OH} = -1.0$ mA (Note 1)
	V_{OH2}	$V_{DD}-0.4$			V	$I_{OH} = -2.0$ mA (Note 2)
Output voltage low	V_{OL1}			+0.4	V	$I_{OL} = 3.2$ mA (Note 1)
	V_{OL2}			+0.4	V	$I_{OL} = 6.4$ mA (Note 2)
Input leakage current	I_{LI}			±10	μA	$0V \leq V_I \leq V_{DD}$
Output leakage current	I_{OL}			±10	μA	$0V \leq V_O \leq V_{DD}$
Supply current	I_{DD}		10	30	mA	

Note:
(1) All pins except DLCLK, DLDATA and R/W CLK.

(2) DLCLK, DLDATA, and R/W CLK pins only.

(3) 9306A only: all inputs except X1.

(4) 9306A only: X1 input.

Capacitance

$T_A = 25°C$, $f_C = 1MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	(Note 1)
Output capacitance	C_O			15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) All unmeasured pins returned to ground.

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
DLCLK, DLDATA rise time	t_{DLR}			20	ns	(Note 2)
DLCLK, DLDATA fall time	t_{DLF}			20	ns	(Note 2)
DLCLK cycle time	t_{CYDLK}		100		ns	
DLCLK high level width	t_{WDLKH}	40	50	60	ns	
DLCLK low level width	t_{WDLKL}	40	50	60	ns	
DLDATA high level width	t_{WDLH}	55	70	100	ns	
DC1–DC9, DD1–DD5 rise time	t_{DR}			30	ns	
DC1–DC9, DD1-DD5 fall time	t_{DF}			30	ns	
DC1–DC9 cycle time	t_{CYDC}		100		ns	
DC1–DC9 high level width	t_{WDCH}	40	50	60	ns	
DC1–DC9 low level width	t_{WDCL}	40	50	60	ns	
DD1–DD5 high level width	t_{WDH}	55	70	100	ns	
R/W CLK rise time	t_{RWR}			10	ns	
R/W CLK fall time	t_{RWF}			10	ns	
R/W CLK cycle time	t_{CYRW}	83	100		ns	
R/W CLK high level width	t_{WRWH}	30			ns	
R/W CLK low level width	t_{WRWL}	30			ns	
Crystal frequency	f_{XTAL}		10	10.5	MHz	
DLCLK ↑ to DC9 ↑ delay time	t_{DDC1}	85	90	95	ns	(Note 3)
DCn ↑ to DCn+1 ↑ delay time (n=1, 2, .., 8)	t_{DDC2}	8	10	12	ns	(Note 3)
DLDATA ↑ to DD5 ↑ delay time	t_{DDD1}	95	100	105	ns	(Note 3)
DDn ↑ to DDn+1 ↑ delay time (n=2, 3, 4)	t_{DDD2}	8	10	12	ns	(Note 3)
R/W CLK ↑ to R/W DATA delay time	t_{DRW}	10	20	45	ns	RGATE=1

Note:
(1) $C_{LOAD} = 30pF$

(2) When delay line is driven

(3) Delay line specs used:
Delay time step = 10 ± 2 ns; total delay time = 100 ± 5 ns

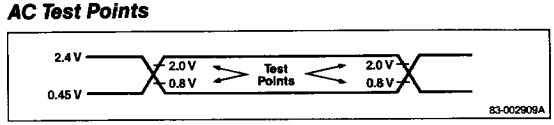
Table 1. μPD9306/A Performance

Connection (Note 1)	Bit Jitter Margin	Speed Variation Tolerance
DD1 to 40-ns delay line tap and DD2 to 60-ns delay line tap	±30 ns	±2% (Note 2)
DD1 to 30-ns delay line tap and DD2 to 70-ns delay line tap	±35 ns	±1.5% (Note 2)

Note:
(1) Performance depends on precision of externally connected delay line.

(2) Modern Winchester drives seldom exceed 0.5% speed variation.

AC Test Points



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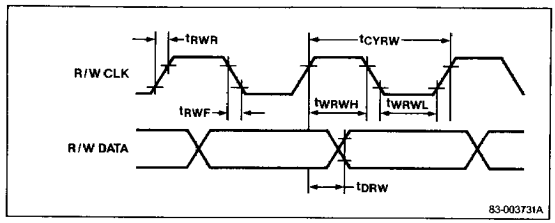
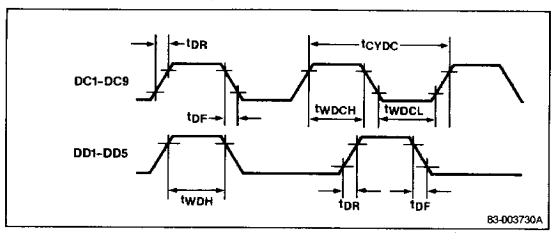
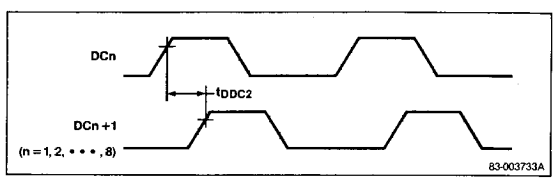
Timing Waveforms

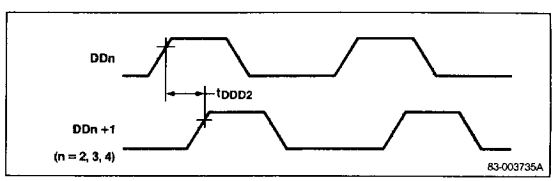
Controller Interface Timing (Read Operation Only)



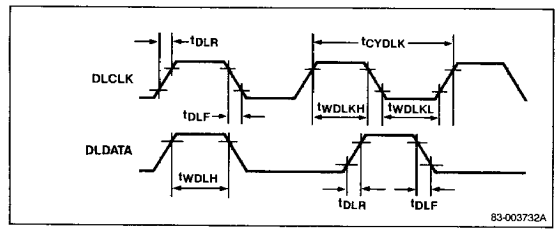
Delay Line Timing Requirements

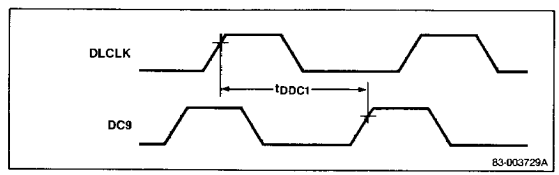


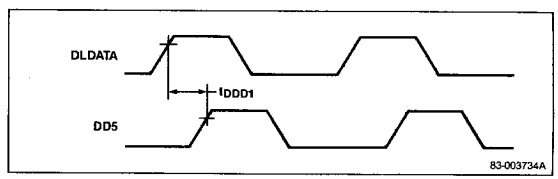




Delay Line Inputs





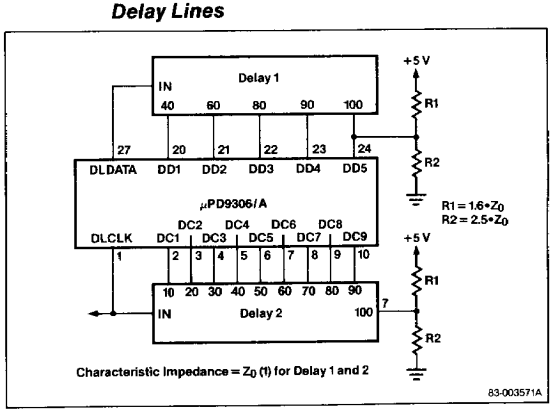


Functional Description

System Configuration

The schematic diagram in figure 1 illustrates the use of the μPD9306/A in conjunction with active delay lines. Active delay lines are the easiest to use in any application, but generally cost twice as much as the passive type. The μPD9306/A is capable of driving passive delay lines with 200 Ω or higher impedance. A circuit example is shown in figure 2. Passive delay lines will perform very well when provided with good grounds and proper termination.

Figure 1. System Configuration with Passive Delay Lines



Note:

(1) An internal terminating resistor provided with the delay line should not be used. The delay line should be terminated at the last stage output (100 ns) as shown.

Precompensation Circuit

Write precompensation is a technique that reduces the bit jitter present in read data, thereby increasing reliability. It is typically used only on the inner cylinders. When data is written to the disk, pulse crowding takes place on the higher-numbered inner cylinders where the same amount of data is compressed into less space than on the outer cylinders. A high percentage of the bit jitter present in the read data is due to magnetic effects causing flux transitions to occur displaced from their nominal position. These effects are predictable based on the pattern of data being recorded. Precompensation reduces bit jitter by writing the data slightly before or slightly after the nominal pulse transition time in a direction opposite to the expected jitter.

Various manufacturers of many ST-506 style Winchester disk drives use delay values of 10–12 ns. The μPD7261A generates the two precompensation control signals, precompensation early (PCE) and precompensation late (PCL), to direct the write data through one of three delay pathways. There is circuitry within the μPD9306/A allowing it to operate with PCE/L and R/W DATA skewed from each other by as much as 50 ns. This eliminates the need for synchronizing the precompensation and write data signals externally.

The μPD9306/A utilizes the data path delay line for both the precompensation and the phase-comparator circuit. When RGATE is low, data appearing on the R/W DATA line is written to the drive. The write data is passed through delay line 1, and the 80-, 90- and 100-ns taps are used for the early, nominal and late signals.

Digital Phase-Locked Loop

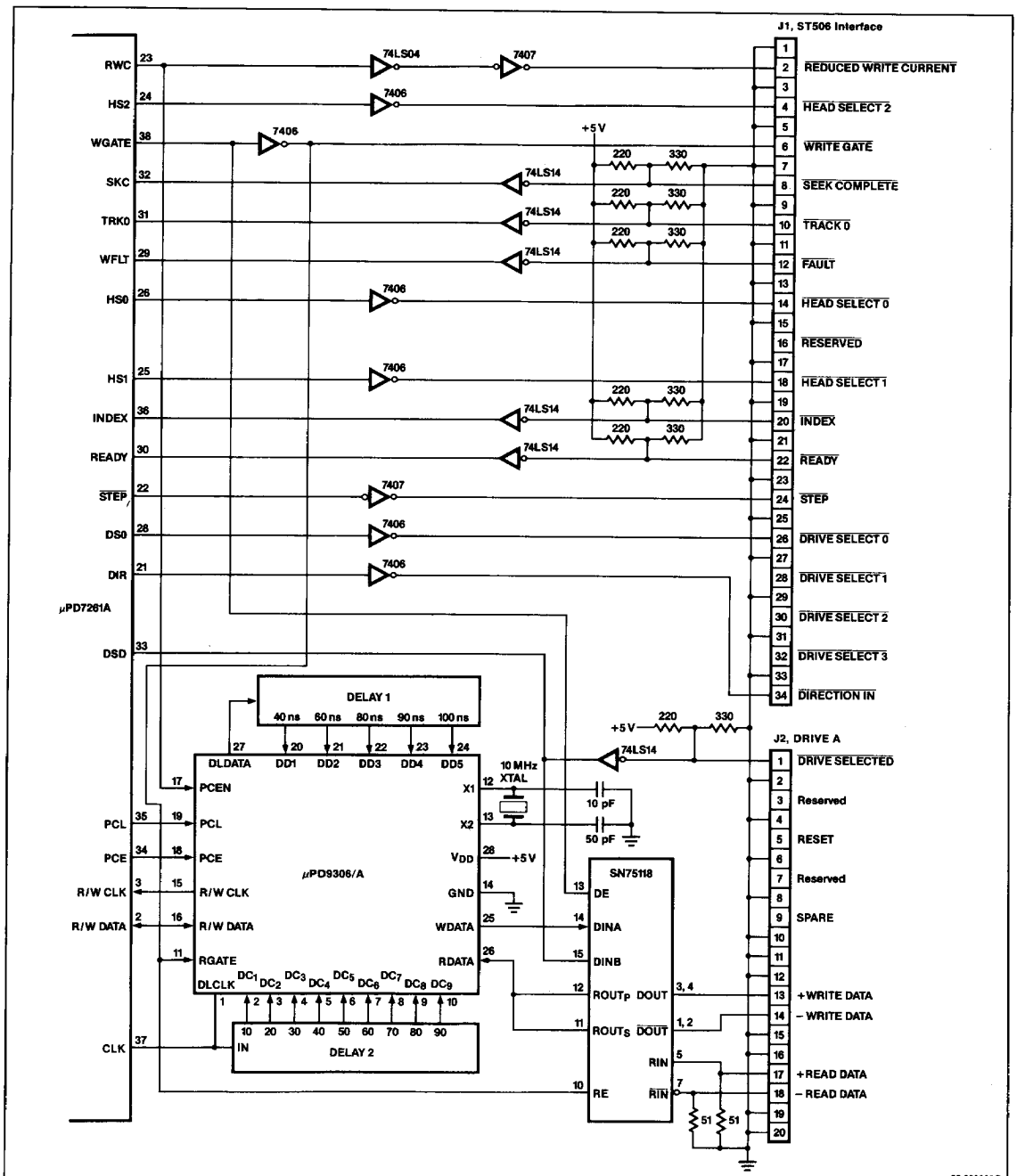
The μPD9306/A employs unique circuitry to accomplish the phase-locked loop (PLL) function, which simplifies the overall design and provides very low error rate data recovery.

The raw read data from the ST-506 Winchester is MFM encoded and consists of clock and data pulses. The data format on the disk is broken into sectors with each sector containing sync fields, address marks, ID fields, and data fields. The different fields each have specific functions. For an in-depth explanation of each of these, refer to the μPD7261A user's manual.

Typically, a Winchester controller will have a data separator that recovers data from the MFM data stream. Within the data separator are several functional blocks that include a sync field detector, phase-locked loop (consisting of a phase comparator, error amplifier, low-pass filter, voltage-controlled oscillator, and pulse synchronizing logic), reference oscillator, and address mark detector. The μPD9306/A eliminates the need for many of these functional blocks. It acquires "lock" within 4 bit times in a sync field, yet it is incapable of locking to a harmonic, as analog PLL circuits are prone to do. The μPD9306/A is also immune to the high-frequency bursts that may occur during the write splice areas of the disk.

6

Figure 2. μPD9306 with Passive Delay Line



The μPD9306/A simulates the function of an analog VCO by using a digital phase-shift network. One of the external delay lines is used to generate ten phase-shifted reference clocks. These clocks have a frequency of 10 MHz and are phase shifted in equal degree increments. The total delay line time is 100 ns, which is the same as the period of the clock, providing a complete 360° phase shift. The μPD9306/A synthesizes the VCO signal by internally selecting one of the phase-shifted clock signals. The rate at which the clock is phase-shifted in one direction or the other corresponds to an increase or decrease in the resulting frequency.

The internal phase comparator uses the data delay line (Delay 1) to divide the data window into ten slices. Depending on where the sampling edge of the recovery clock falls within the data window, a proprietary algorithm changes the phase of the recovery clock. The μPD9306/A has the same jitter rejection abilities that you would expect from a well-designed analog PLL. It can accept disk data with jitter in excess of plus or minus 30 ns. As an option, delay line 1 taps DD1 and DD2 may be connected to the 30-ns and the 70-ns tap respectively. Due to this option, the μPD9306/A performance is affected by its immunity to bit jitter and its tolerance to speed variation as shown in table 1.