TEA1501

GreenChip SMPS controller IC

Rev. 02 — 31 March 2006 | Product data sheet

1. General description

The TEA1501 is the low power member of the GreenChip family and is especially designed for standby Switched Mode Power Supply (SMPS) applications. The TEA1501 incorporates all the necessary functions for an efficient and low cost power supply for 90 V to 276 V AC universal input. The TEA1501 is a monolithic integrated circuit and is available in a SO8 package. The design is made in the BCD_PowerLogic750 process and includes the high voltage switching device. Using only seven functional pins, the TEA1501 contains extensive control functions to form a flexible and a reliable power supply with a minimum of external components. The TEA1501 operates in a flyback topology (see Figure 3) with a fixed switching frequency, constant primary peak current control and regulates the output voltage in Burst mode.

Applications include low power and standby power supplies as used in television, monitor, lighting electronics and domestic appliances with an output power from 0.1 W to 3 W.

2. Features

2.1 Distinctive features

- Direct off-line operation (90 V to 276 V AC)
- Low external component count
- Integrated high voltage start-up current source for a fast start-up within 0.25 s
- Integrated power switch: 650 V, 40 Ω, 0.25 A
- Programmable primary peak current
- Data transfer from isolated secondary side to non-isolated primary side via the transformer
- On/off function replaces expensive mains switch by a functional switch

2.2 Green features

- Low current consumption in Off mode, typical 40 μA
- Efficient Burst mode operation, for 0.1 W to 3 W output power

2.3 Protection features

- Cycle-by-cycle current control with programmable primary peak current
- Overvoltage protection
- Undervoltage lockout
- Overtemperature protection

PHILIPS

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{on/off}$	on/off level		0.4	0.7	0.9	V
$V_{data(off)}$	data off level	20 μA < I_{OOD} < 100 μA	0.9	1.3	1.6	V
$V_{data(on)}$	data on level	20 μA < I_{OOD} < 100 μA	3.5	4.0	4.5	V
I_{start}	start-up current, pin AUX	V_{AUX} = 8 V; V_{OOD} > 0.9 V	–2.4	–1.8	–1.2	mA
$I_{DRAIN(off)}$	pin DRAIN current in Off mode	V_{OOD} < 0.4 V; V_{DRAIN} = 300 V	-	40	100	μA
V_{BD}	breakdown voltage	$I_{DRAIN(off)}$ + 100 μA	650	-	-	V
R_{dson}	on resistance	T_j = 25 °C; I_{DRAIN} = 80 mA	25	40	55	Ω
V_{detect}	detection level		0.47	0.50	0.53	V

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA1501T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5. Block diagram

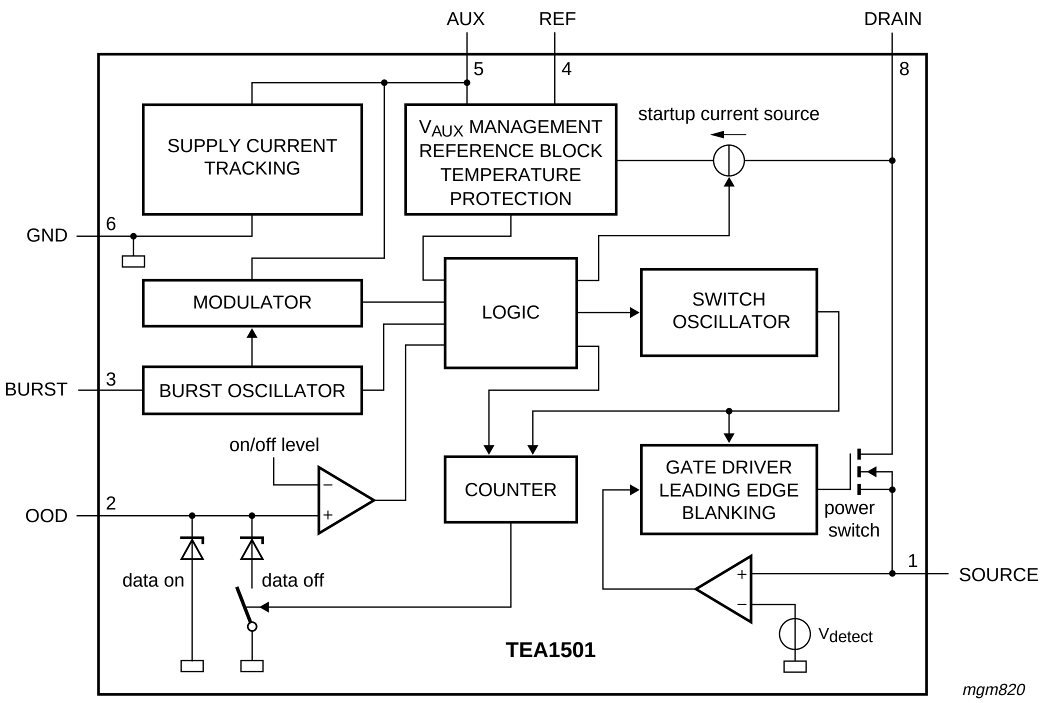


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

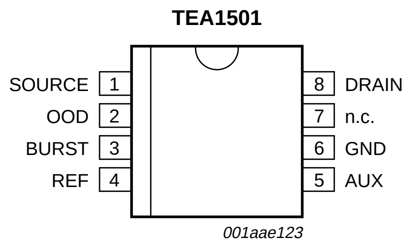


Fig 2. Pin configuration: TEA1501T (SOT176-1)

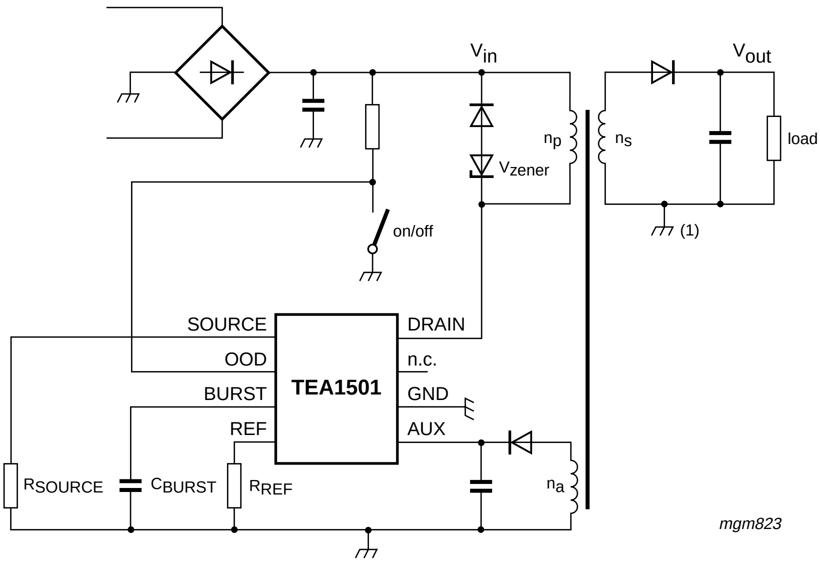
6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SOURCE	1	source of the power switch and input for primary current sensing
OOD	2	on/off input and data transfer output
BURST	3	input for burst capacitor
REF	4	input for reference resistor
AUX	5	supply input of the IC and input for voltage regulation
GND	6	ground
n.c.	7	not connected to comply with safety requirements
DRAIN	8	drain of the power switch and input for start-up current

7. Functional description

The TEA1501 contains a high voltage power switch, a high voltage start-up circuit and low voltage control circuitry on the same IC. Together with a transformer and a few external components a low power, isolated, flyback converter can be built, see Figure 3. The system of the TEA1501 operates in a Burst mode. During each burst period the output voltage is regulated to a desired voltage level.



(1) The secondary earthing point is isolated from the primary earthing points.

Fig 3. Basic flyback configuration

7.1 System operation

7.1.1 On/off

The system of the TEA1501 can be switched on and off by means of a low cost, low voltage switch. In the Off mode the start-up current source and power switch are disabled. In the On mode, the TEA1501 delivers the start-up current for the supply capacitor and after the supply voltage reaches the start-up level, the TEA1501 activates the power switch.

7.1.2 Start-up

The start-up is realized with a high voltage start-up current source instead of a dissipative bleeder resistor which is commonly used by low voltage control ICs. When the TEA1501 is switched on, the start-up current source is enabled and starts charging the AUX capacitor. The start-up current level is high and accurate (typical 1.8 mA) which results in a well-defined and short start-up time, within 0.25 s. After the supply voltage reaches the start-up level the current source is switched off and the AUX capacitor supplies the chip. Reducing the power dissipation in the current source to zero after start-up is one of the green features of the TEA1501.

7.1.3 Operation

After start-up the flyback converter starts delivering energy to the secondary and auxiliary winding. The system of the TEA1501 works with fixed switching frequency and fixed peak current.

As all the windings of the flyback transformer have the same flux variation, the secondary voltage and the auxiliary voltage are related via the turns-ratio (n_s : n_a). Therefore, the isolated secondary voltage is controlled by the non-isolated auxiliary voltage.

The Burst mode operates by switching at high frequency until V_{AUX} reaches its regulation level of 20 V. The TEA1501 stops switching until the time period set by the burst oscillator has expired. At the start of the next burst period the TEA1501 starts switching at high frequency and repeats the cycle again.

To guarantee a stable operation in a Burst mode controlled system a V_{AUX} slope compensation circuit is integrated in the TEA1501. The TEA1501 delivers a constant voltage to the secondary load until a burst duty cycle of 40 % is reached.

7.1.4 Data transfer

The TEA1501 has a data transfer function which makes communication from the isolated secondary side to the non-isolated primary side of the transformer possible, without using an opto-coupler. This communication function is activated by increasing the secondary load. With this data transfer function a main power supply can be switched on and off by the system of the TEA1501.

The power delivered to the secondary and auxiliary winding is proportional to the number of primary current pulses per burst period, provided that the converter operates in Discontinuous conduction mode. During each burst period the number of primary current pulses is counted. A threshold (N_{data}) of 56 pulses is integrated. The clamp level on the OOD pin is set to data-on level from data-off level in case the N_{data} threshold is passed. This data-on clamp level can be sensed by the on/off input of a main supply control IC of the GreenChip family. The data-on clamp level is maintained until a burst appears with a number of pulses below the N_{data} threshold.

7.2 Waveforms in the Off mode, Start-up mode and Operation mode

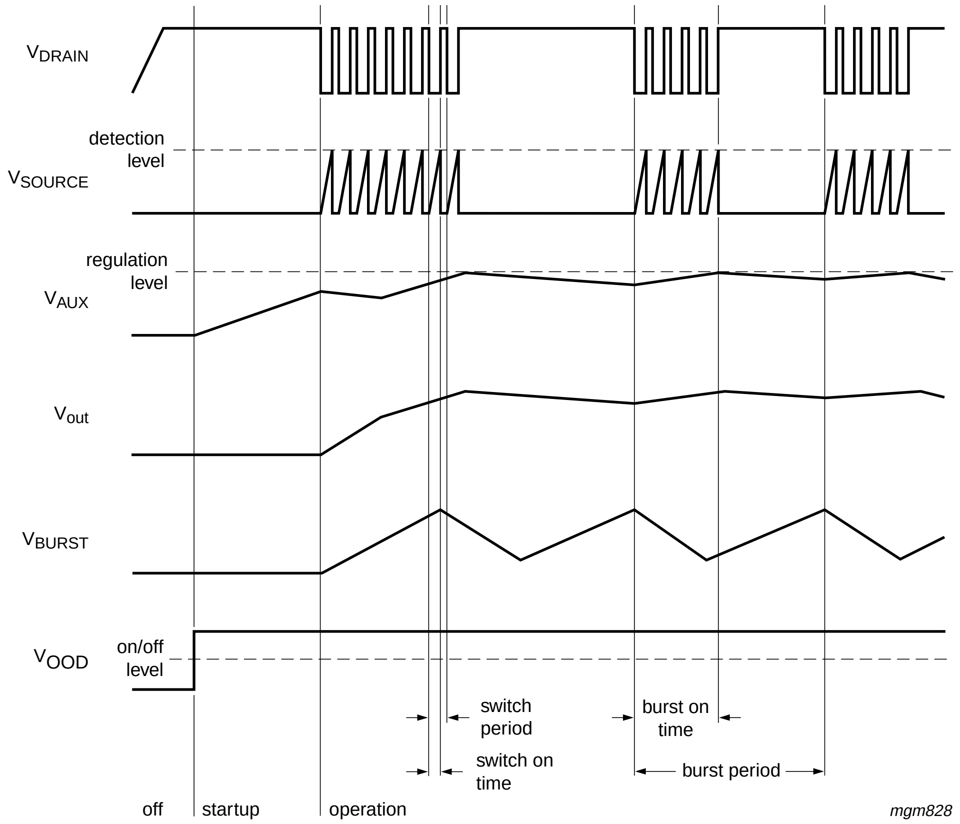


Fig 4. Waveforms of the TEA1501 in the Off mode, Start-up mode and Operation mode

7.3 Circuit block description

7.3.1 On/off/data section

The on/off/data block contains a comparator for the on/off level and is active if the drain voltage is above 50 V (DC). The typical current consumption in Off mode is 40 µA. The data signal changes the clamp level on the OOD pin to indicate data transfer: low clamp level for data-off and high clamp level for data-on.

7.3.2 V_{AUX} management

The V_{AUX} management block is active when the TEA1501 is in the On mode. This V_{AUX} management block senses the AUX voltage and determines the state of the TEA1501: start-up or normal operation. During start-up the following circuits are active: On/off/data section, reference block (partial), V_{AUX} management, temperature protection and the start-up current source.

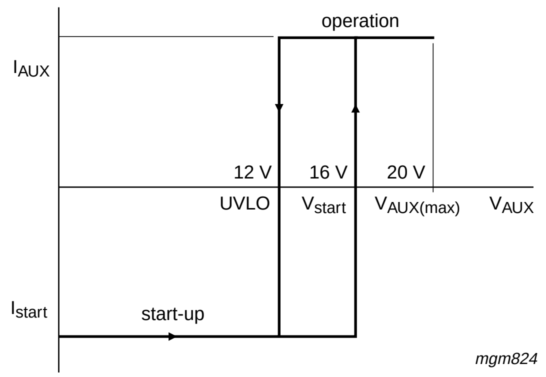


Fig 5. I_{AUX} **as a function of** V_{AUX}

7.3.3 Start-up current source

The start-up sequence is carried out using an accurate start-up current source. The start-up current flows from the DRAIN pin to the AUX pin via the start-up current source and charges the AUX capacitor. When AUX reaches the start-up threshold the start-up current is switched off and the flyback converter starts operating and the output voltage rises. The AUX capacitor must be capable of supplying the entire supply current ($I_{AUX(low)}$) until the output voltage is in regulation. From that moment the AUX capacitor is charged by the flyback converter via the auxiliary winding.

7.3.4 Reference block

The reference block contains a band gap circuit which determines all the accurate and temperature independent reference voltages and currents. It defines the voltage detection level for the primary current comparator and it defines the voltage at the REF pin. The value of the reference resistor determines the burst frequency, the switching frequency and the leading edge blanking time.

7.3.5 Temperature protection

The temperature protection circuit senses the chip temperature using a proportional to absolute temperature voltage (V_{ptat}) generated in the reference block. If the chip temperature exceeds 140 °C the power switch and the start-up current source are disabled. When the chip cools down below 100 °C, the start-up circuit is enabled again.

7.3.6 Switch oscillator

The switch oscillator determines the switching frequency and the maximum on-time of the power switch. The maximum on-time is set at 66 % of the switching period. The switching frequency is determined by the reference resistor at the REF pin and an internal capacitor. The switching frequency can be adjusted in a range from 20 kHz to 50 kHz, thus above the audible spectrum.

7.3.7 Burst oscillator

The burst oscillator generates a triangular wave signal for determination of the burst frequency. The burst frequency is determined accurately and temperature independent by the externally connected reference resistor R_{REF} and burst capacitor C_{BURST}.

7.3.8 Gate driver

The gate driver switches the power switch. The power switch is turned on at the beginning of every oscillator cycle and is turned off by the primary current comparator or by the maximum on-time. The power switch is also prevented from turning on if V_{AUX} has reached its regulation level or in the case of active overtemperature protection or active undervoltage lockout protection.

7.3.9 Power switch

The power switch is an integrated high voltage Lateral Diffused Metal Oxide Semiconductor Transistor (LDMOST) with a R_{dson} of 40 Ω, a maximum peak drain voltage of 650 V, a maximum continuous drain voltage of 500 V and a maximum drain current of 0.25 A.

7.3.10 Primary current comparator

The primary current comparator senses the voltage across the external sense resistor R_{SOURCE} which reflects the primary current. The detection level of the comparator is 0.5 V. The power switch is switched off quickly when the source voltage exceeds this detection level. The comparator has a typical propagation delay of 80 ns. If the dV/dt of the drain voltage has to be limited for ElectroMagnetic Interference (EMI) reasons, a capacitor can be connected between the DRAIN and SOURCE pins of the TEA1501. The discharge current of this EMI capacitor does not flow through the sense resistor R_{SOURCE} and does not activate the comparator.

7.3.11 Leading edge blanking

To prevent the power switch from switching off due to the discharge current of the capacitance on the DRAIN pin a Leading Edge Blanking (LEB) circuit has been implemented. The leading edge blanking time is defined as the maximum duration time needed to discharge the capacitance at the drain of the power switch. The leading edge blanking time is determined by the reference resistor to obtain an accurate and temperature independent time. The LEB time tracks with the period time of the switch oscillator.

7.3.12 Modulator

The modulator determines the regulation level of V_{AUX}. For a burst duty cycle from 0 % to 40 % the AUX voltage is regulated to 20 V. For stable operation in Burst mode a decrease in regulation voltage is integrated for a burst duty cycle above 40 %. At 100 % burst duty cycle the regulation voltage is 17.5 V.

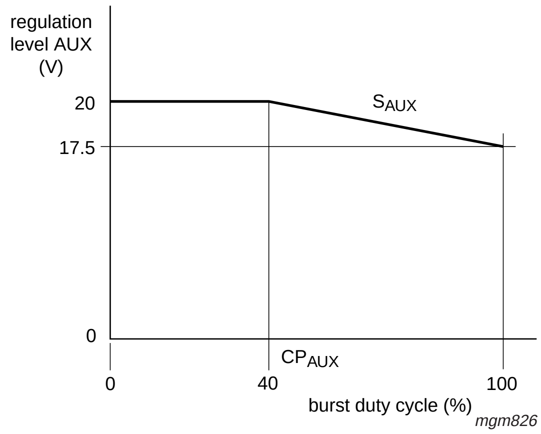


Fig 6. Regulation level AUX as a function of burst duty cycle

7.3.13 Counter

The power delivered to the load (auxiliary and secondary) is a function of the number of energy pulses per burst, according to the following formula

$$P_{load} = \eta \times \frac{1}{2} \times L_p \times I_{prim}{}^2 \times f_{burst} \times N$$

Where η is the efficiency, L_p is the primary inductance, I_{prim} is the primary peak current, f_{burst} is the burst frequency and N is the number of pulses in one burst period.

The counter counts the number of pulses in each burst period and detects if the N_{data} threshold is passed. The counter state is used for the data transfer function and for the supply current tracking.

7.3.14 Supply current tracking

For obtaining good load regulation, especially with low cost transformers, a tracking circuit is included. The tracking circuit makes the supply current of the TEA1501 a function of the secondary load. This makes the voltage drop across the series resistance of the auxiliary winding proportional to the voltage drop across the series resistance of the secondary winding. Therefore, the secondary output voltage tracks with the AUX regulation voltage.

The tracking starts at a counter state of 28. For a counter state from 28 up to 112 (typical values) the supply current of the TEA1501 rises linearly with the counter state according to the following formula, see Figure 7.

$$I_{AUX} = k_{tracking} \times N$$

For counter states of 112 and higher the supply current remains on its maximum value.

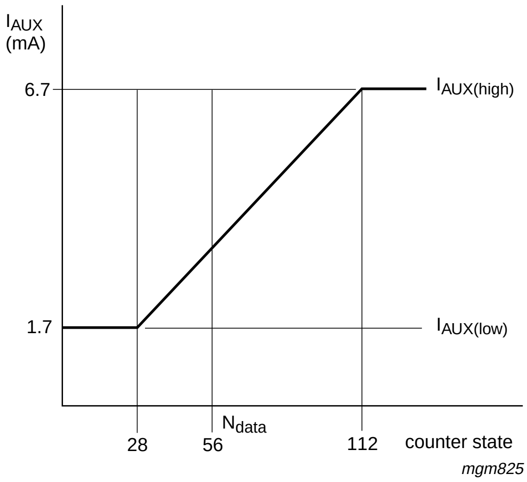


Fig 7. AUX current as a function of counter state

7.4 Design Equations

7.4.1 Primary peak current

The primary peak current is determined by the sense resistor R_{SOURCE} and may be calculated as shown below:

$$R_{SOURCE} = \frac{V_{detect}}{I_{prim}}$$

7.4.1.1 Minimum value of R_{SOURCE}

The maximum drain current is 0.25 A, this results in a minimum value for resistor R_{SOURCE} of 2.0 Ω.

7.4.2 Switch oscillator

The maximum output power of the converter is a function of the switching frequency, provided that the converter operates in discontinuous conduction mode.

$$P_{out(max)} = \eta \times \frac{1}{2} \times L_p \times I_{prim}{}^2 \times f_{switch}$$

Where η is the efficiency, Lp is the primary inductance, I_{prim} is the primary peak current and f_{switch} is the switching frequency.

The switching frequency can be adjusted between 20 kHz and 50 kHz by the reference resistor R_{REF}:

$$f_{switch} = \frac{1}{k_{switch} \times R_{REF}}$$

7.4.2.1 Range of R_{REF} values

The minimum value for resistor R_{REF} is 24 kΩ, the maximum value is 62 kΩ.

7.4.3 Leading edge blanking

The leading edge blanking time is determined by the reference resistor R_{REF} as shown below:

$$t_{LEB} = t_{constant} + (k_{LEB} \times R_{REF})$$

The leading edge blanking time consists of a constant time and a time which tracks with the period time of the switch oscillator.

7.4.4 Burst oscillator

The power threshold for data transfer is determined by the burst frequency, according to the following formula:

$$P_{data} = \eta \times \frac{1}{2} \times L_p \times I_{prim}{}^2 \times f_{burst} \times N_{data}$$

The power ratio P_{data} : $P_{out(max)}$ is therefore:

$$\frac{P_{data}}{P_{out(max)}} = \frac{f_{burst} \times N_{data}}{f_{switch}}$$

The desired P_{data} : $P_{out(max)}$ ratio determines the burst frequency. For example, when the desired P_{data} : $P_{out(max)}$ ratio is 0.5 then the burst frequency has to be 450 Hz at 50 kHz switching frequency. The burst frequency can be adjusted by the reference resistor R_{REF} and the burst capacitor C_{BURST} as shown below:

$$f_{burst} = \frac{1}{k_{burst} \times R_{REF} \times C_{BURST}}$$

7.4.4.1 Minimum value of C_{BURST}

The minimum value for capacitor C_{BURST} is 3.3 nF.

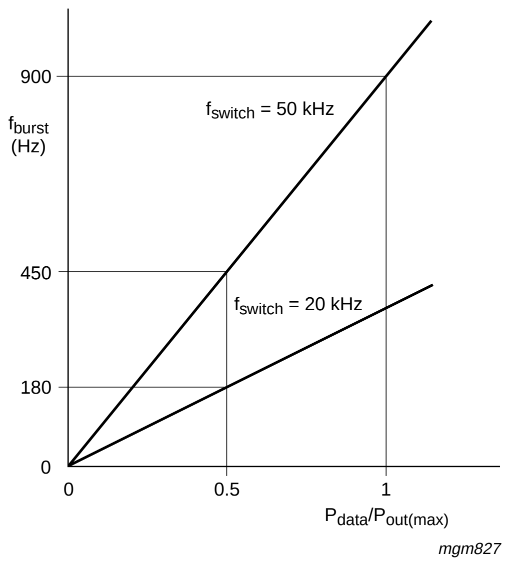


Fig 8. Burst frequency as a function of power ratio

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referred to ground. Positive currents flow into the IC. All pins not mentioned in the voltage list are not allowed to be voltage driven.

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{DRAIN}	pin DRAIN voltage	commutation voltage peak: $V_{in} + V_{zener}$	[1]	–0.4	+650	V
V_{SOURCE}	pin SOURCE voltage			–0.4	+12	V
V_{AUX}	pin AUX voltage			–0.4	+24	V
V_{BURST}	pin BURST voltage			–0.4	+5	V
Currents						
I_{DRAIN}	pin DRAIN current			0	0.25	A
I_{SOURCE}	pin SOURCE current			0	0.25	A
I_{OOD}	pin OOD current			–1	+5	mA
I_{REF}	pin REF current			–1	+0	mA
I_{BURST}	pin BURST current			–1	+0.05	mA
Power and temperature						
P_{tot}	total power dissipation	T_{amb} < 70 °C		-	0.7	W
T_j	junction temperature			–10	+140	°C
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			–10	+70	°C

[1] The ElectroStatic Discharge (ESD) voltage according to the Human Body Model is limited to 1200 V for pin 8 (DRAIN).

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	96	K/W

10. Characteristics

Table 6. Characteristics

Conditions unless otherwise specified: –10 °C < T_j < 80 °C, R_{REF} = 24 kΩ – 0.1 %; 12 V < V_{AUX} < 20 V. All voltages are referred to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/off/data section						
$V_{on/off}$	on/off level		0.4	0.7	0.9	V
$V_{data(off)}$	data off level	20 µA < I_{OOD} < 100 µA	0.9	1.3	1.6	V
		I_{OOD} = 2.5 mA	1.4	1.7	2.0	V
$V_{data(on)}$	data on level	20 µA < I_{OOD} < 100 µA	3.5	4.0	4.5	V

Table 6. Characteristics *...continued*

Conditions unless otherwise specified: –10 °C < T_j < 80 °C, R_{REF} = 24 kΩ – 0.1 %; 12 V < V_{AUX} < 20 V. All voltages are referred to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AUX} management						
V_{start}	start voltage		15	16	17	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		11.3	12	12.7	V
Start-up current source						
I_{start}	start-up current, pin AUX	V_{OOD} > 0.9 V				
		V_{AUX} = 0 V	–3.0	–2.2	–1.5	mA
		V_{AUX} = 8 V	–2.4	–1.8	–1.2	mA
		V_{AUX} = 15 V	–1.9	–1.3	–0.8	mA
$I_{DRAIN(on)}$	pin DRAIN current during start-up	V_{AUX} = 0 V; V_{OOD} > 0.9 V	1.8	2.6	3.4	mA
$I_{DRAIN(off)}$	pin DRAIN current in Off mode	V_{OOD} < 0.4 V; V_{DRAIN} = 300 V	-	40	100	µA
Reference block						
V_{REF}	reference voltage		1.18	1.23	1.28	V
Temperature protection						
T_{prot}	thermal shutdown		130	140	150	°C
T_{hys}	thermal hysteresis		35	40	45	°C
Switch oscillator						
k_{switch}	switch oscillation constant		0.67	0.82	1.00	µs/kΩ
$\delta_{cy(max)}$	maximum switch duty cycle		60	66	72	%
Burst oscillator						
k_{burst}	burst oscillation factor		7.0	7.5	8.1	
Counter						
N_{data}	number of current pulses for data transfer		50	56	62	
Power switch						
V_{BD}	breakdown voltage	$I_{DRAIN(off)}$ + 100 µA	650	-	-	V
R_{dson}	on resistance	T_j = 25 °C; I_{DRAIN} = 80 mA	25	40	55	Ω
t_f	fall time	V_{DRAIN} = 300 V; R_{DRAIN} = 2 kΩ	-	50	-	ns
t_r	rise time	V_{DRAIN} = 300 V; R_{DRAIN} = 2 kΩ	-	100	-	ns
Comparator						
V_{detect}	primary peak detection level		0.47	0.50	0.53	V
t_{PD}	propagation delay	dV_{source}/dt = 0.5 V/µs	-	80	-	ns
Leading edge blanking						
$t_{constant}$	constant part of the LEB time, independent of R_{REF}		100	250	400	ns
k_{LEB}	LEB time constant		4	5	6	ns/kΩ

Table 6. Characteristics *...continued*

Conditions unless otherwise specified: –10 °C < T_j < 80 °C, R_{REF} = 24 kΩ – 0.1 %; 12 V < V_{AUX} < 20 V. All voltages are referred to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Modulator						
$V_{AUX(max)}$	maximum V_{AUX} non-compensation	δ_{burst} < CP_{AUX}	19	20	21	V
CP_{AUX}	compensation point		37	40	43	%
S_{AUX}	slope of $V_{AUX(max)}$, $\Delta V_{AUX(max)}$ / (100 % – CP_{AUX})	δ_{burst} < CP_{AUX}	34	42	50	mV/%
V_{offset}	offset voltage on $V_{AUX(max)}$	$V_{AUX(max)}$ at compensation point	-	–0.1	-	V
Supply current tracking						
$I_{AUX(low)}$	low supply current	N < $0.5N_{data}$; non-tracking	1.2	1.7	2.5	mA
$k_{tracking}$	tracking constant		48	60	72	μA
$I_{AUX(high)}$	high supply current	N > $2N_{data}$; non-tracking	5.4	6.7	8.0	mA

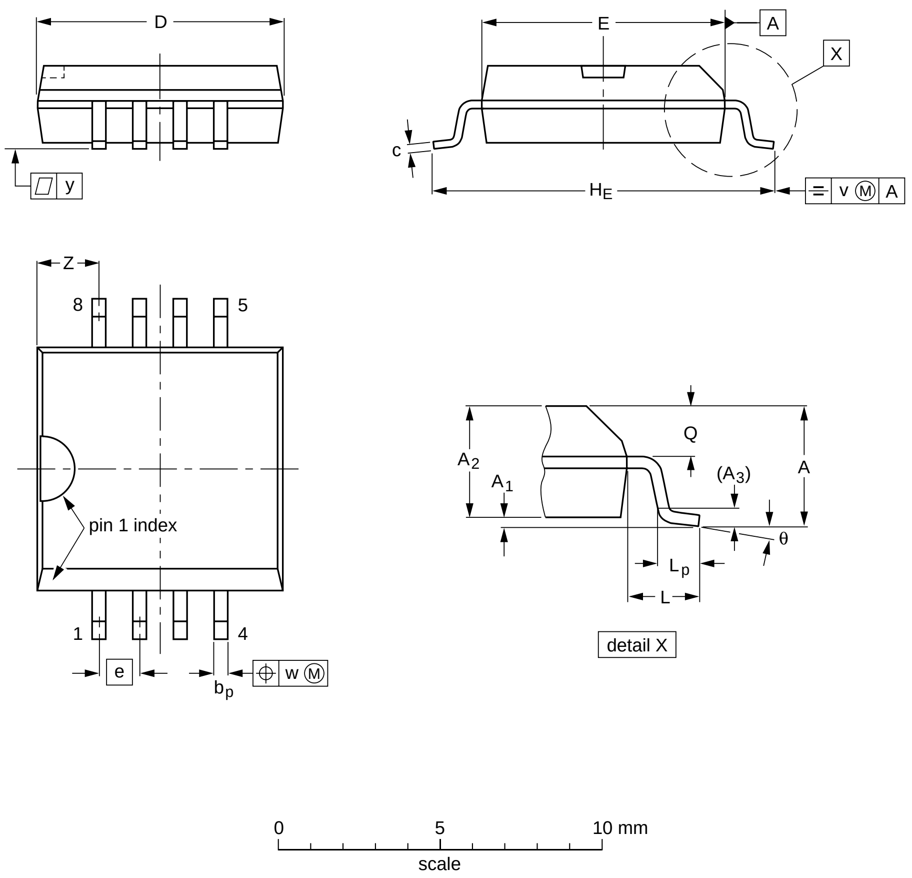
11. Test information

11.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.05	0.419 0.394	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT176-1						~~97-05-22~~ 03-02-19

Fig 9. Package outline SOT176-1 (SO8)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 260 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 7. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1501_2	20060331	Product data sheet	-	TEA1501_N_1 (9397 750 03371)
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Added package SO8, removed package DIP8. See Table 2 “Ordering information”, Section 6.1 “Pinning” and Section 12 “Package outline” • Removed TEA1504 application (section “Low power standby application”).			
TEA1501_N_1 (9397 750 03371)	19980819	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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17. Contents

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