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SSI 32P549
Pulse Detector

December 1991

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DESCRIPTION

The SSI 32P549 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

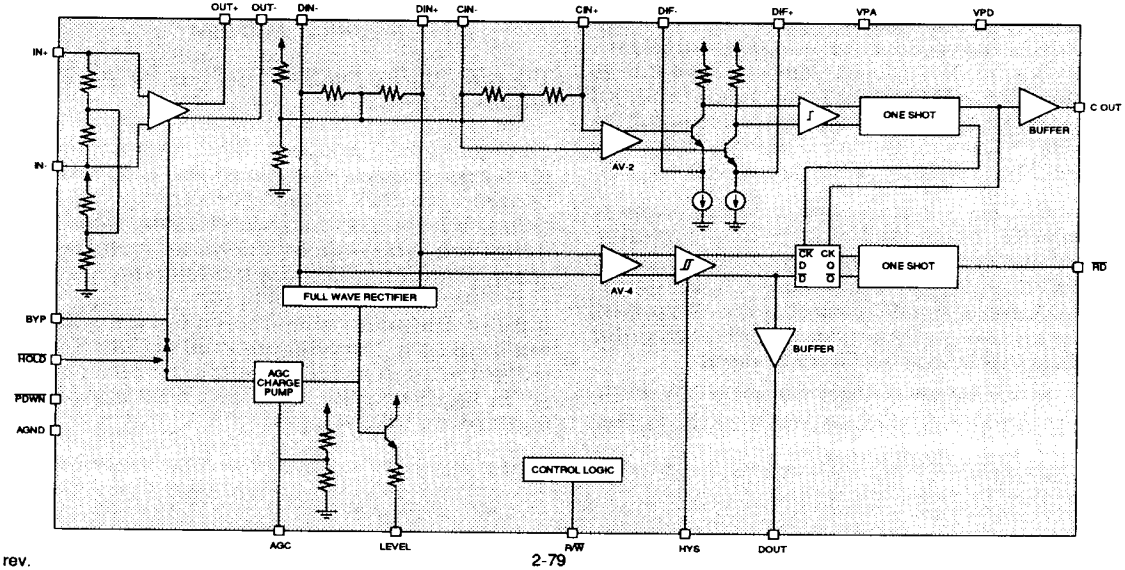
In read mode the SSI 32P549 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the read data pulse circuitry is disabled, the AGC gain is held constant, and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P549 requires a +5V power supply and is available in a 28-pin PLCC, 24-pin DIP and 24-pin SOL.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ± 10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤ ±1.0 ns pulse pairing**
- **16 Mbit/s operation**

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P549 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.3V, nom)

Rint = AGC pin input impedance (2.5 kΩ, typ)

Rext = External resistor

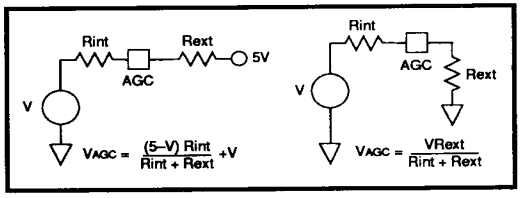


FIGURE 1: AGC Voltage

The new DIN ± input target level is nominally (V_{AGC} - 0.75) • 0.64 Vpp.

The maximum AGC amplifier output swing is 2.6 Vpp at OUT±, which allows for up to 6dB loss, with margin, in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

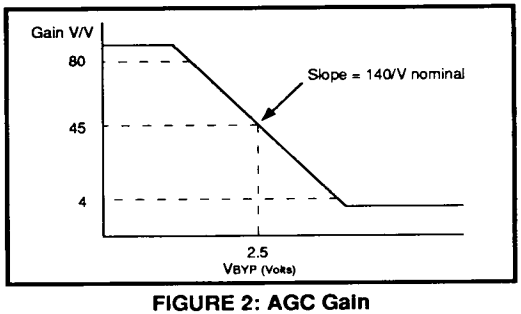


FIGURE 2: AGC Gain

The AGC amplifier has emitter follower outputs and can sink 3.5 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built-in 0.05V threshold (10% of 1Vpp) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull down resistor. If no testing is necessary, the DOUT pin can be pulled up to VPD (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 150\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

WRITE MODE

In Write Mode the SSI 32P549 Pulse Detector is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P549 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown. When $\overline{PDWN}$ returns high, the device executes the normal Write to Read recovery sequence.

MODE CONTROL

The SSI 32P549 circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

R/$\overline{W}$	$\overline{HOLD}$	$\overline{PDWN}$	
1	1	1	Read Mode, AGC Active
1	0	1	Read Mode AGC gain held constant*
0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	0	Power Down - low current disabled mode

* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

TABLE 1: Mode Control

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	I	Analog (+5V) power supply for pulse detector
AGND	I	Analog ground pin for pulse detector block
VPD	I	Digital (+5V) power supply pin
DGND	I	Digital ground pin
IN+, IN–	I	Analog signal input pins
OUT+, OUT–	O	Read path AGC Amplifier output pins
DIN+, DIN–	I	Analog input to the hysteresis comparator
CIN+, CIN–	I	Analog input to the differentiator
DIF+, DIF–	I/O	Pins for external differentiating network
COUT	O	Test point for monitoring the flip-flop clock input
DOUT	O	Test point for monitoring the flip-flop D-input
$\overline{RD}$	O	TTL compatible read output
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1
AGC	I	Reference input voltage for the read data AGC loop
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
$\overline{PDWN}$	I	Low state on this pin puts the device in a low power "off" state
R/$\overline{W}$	I	Selects Read or Write mode

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ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA & VPD)		4.5	5.0	5.5	V
Junction Temperature, Tj		25		135	°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IVPA IVPD	Supply Current	Outputs unloaded; $\overline{PDWN}$ = high or open		58	80	mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded; $\overline{PDWN}$ = high		290	440	mW
		Outputs unloaded; $\overline{PDWN}$ = low		100	150	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VPA+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

ELECTRICAL SPECIFICATIONS (Continued)

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable to/from $\overline{PDWN}$ Transition Time	Settling time of external capacitors not included, pin high to/from low			20	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC settling not included	0.4	0.9	1.6	µs
$\overline{HOLD}$ On to/from $\overline{HOLD}$ Off Transition Time	$\overline{HOLD}$ pin high to/from low			1.0	µs

READ MODE (R/$\overline{W}$ is high)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >800Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Minimum Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 2.6 Vpp	4		80	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP pin THD ≤ 5%	2.6			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		4	10	pF
Single Ended Input Impedance (Each Side)	R/$\overline{W}$ = high, IN+ or IN- pin	2	2.7	3.8	kΩ
	R/$\overline{W}$ = low, IN+ or IN- pin		160	250	Ω
Input Noise Voltage	Gain set to maximum		5	15	nV$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	30			MHz
OUT+ & OUT- Pin Current	No DC path to AGND	±2.5	±3.5		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40	65		dB
PSRR (Input Referred)	VPA, VPD = 100 mVpp @ 5 MHz, gain set to max	30			dB

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
(DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = (V_{AGC} - K1) • K2	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp				
	K1	0.5	0.75	1.00	V
	K2	0.54	0.64	0.74	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			5	%
AGC Voltage	AGC open	1.8	2.3	2.7	V
AGC Pin Input Impedance		1.8	2.5	3.8	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V, AGC pin open	2.8	4.5	6.5	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high		0.12		mA
AGC Leakage Current	$\overline{HOLD}$ = low, 10 ≤ AGC gain ≤80	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.563 VDC, AGC pin open	-0.11	-0.18	-0.27	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, AGC pin open	-0.9	-1.4	-2.1	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value	12	20	36	µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp @ 2.5 MHz (OUT+) - (OUT-) to 90% final value	38	60	110	µs
Gain Attack Time	R/$\overline{W}$ = low to high (IN+) - (IN-) = 250 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value	0.8	2	3.6	µs

WRITE MODE (R/$\overline{W}$ is low)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Single-ended Input Impedance (each side)	IN+ or IN-		160	250	Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Single Ended Input Voltage at DIN± Impedance (Each Side)	DIN+ or DIN-	4	5	7	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND		1		V/Vpp
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Threshold Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V	0.32	0.36	0.44	V/V
HYS Pin Current	0.3 V < HYS < 1.0V	0.0		-10	µA
DOUT Pin Output Low Voltage	5 kΩ from DOUT to DGND		VPD -2		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to DGND		VPD -1.6		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz			5.0	pF
Single Ended Input Impedance	CIN+ or CIN-	4	5	7	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA

ACTIVE DIFFERENTIATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
COUT Pin Output Low Voltage	5 kΩ from COUT to DGND		VPD -2		V
COUT Pin Output High Voltage	5 kΩ from COUT to DGND		VPD -1.6		V
COUT Pin Output Pulse Width		22	35	55	ns

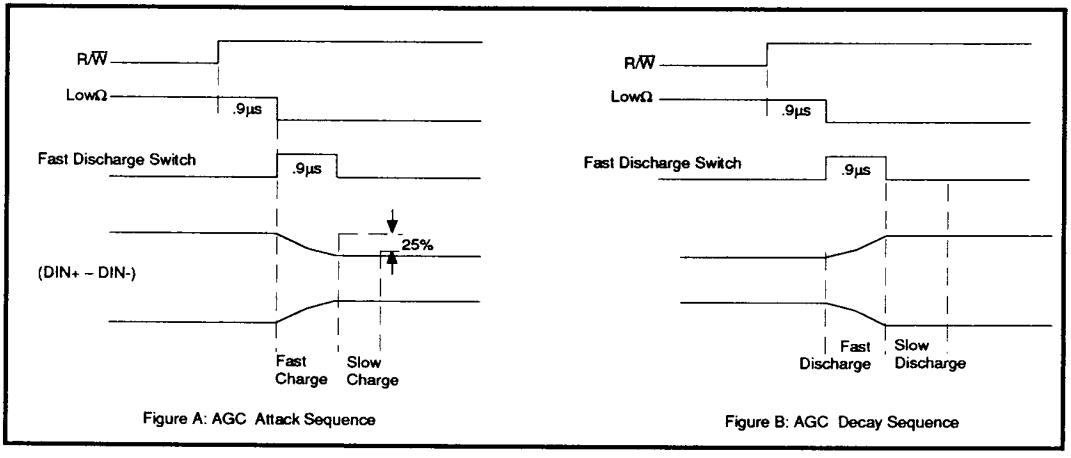

FIGURE 7: AGC Timing Diagram

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay			15		ns
Td3-Td4	Pulse Pairing	1.0 Vpp, 2.5 MHz sinewave			2	ns
Td3-Td4	Pulse Pairing	1.0 Vpp, 5 MHz sinewave			1	ns
Td5	$\overline{RD}$ Output Pulse Width		22	35	55	ns

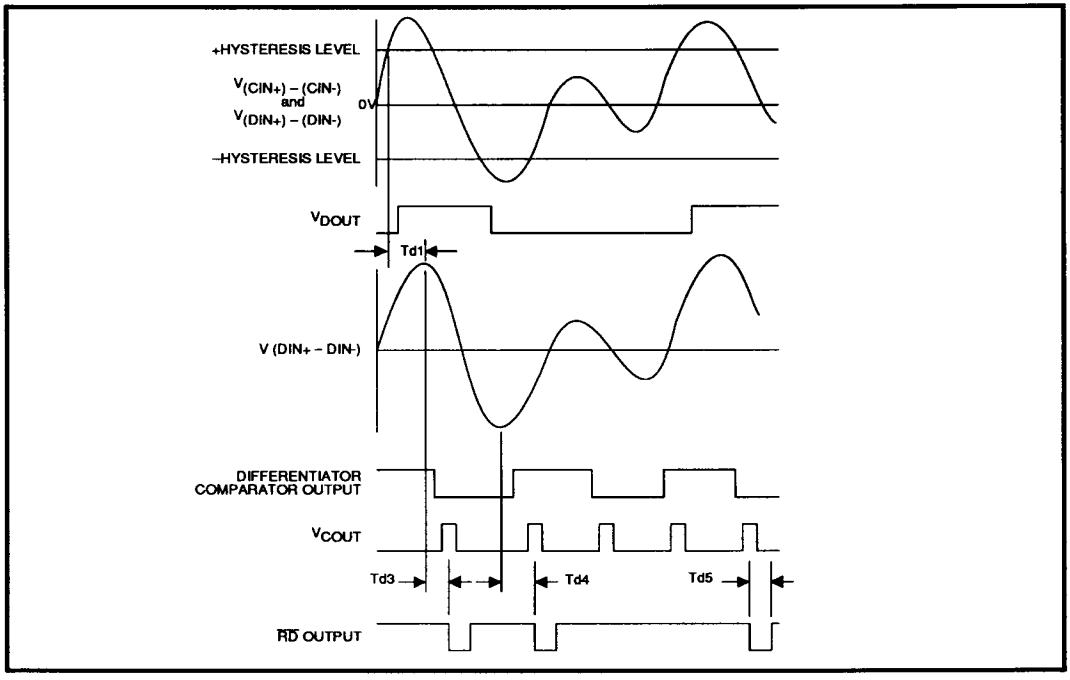

FIGURE 8: Read Mode Digital Section Timing Diagram

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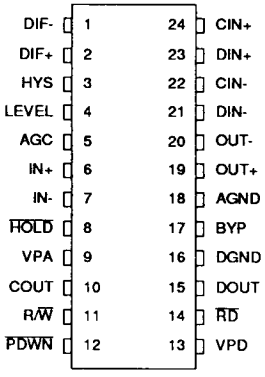
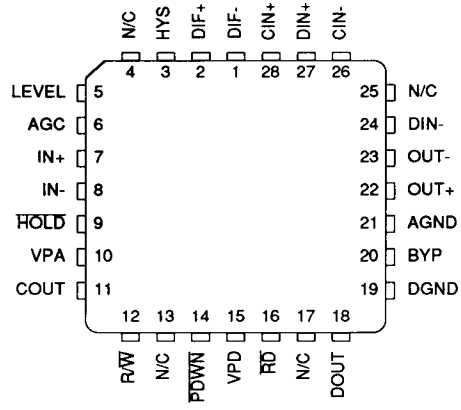
PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: θja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P549 Pulse Detector		
24-Pin PDIP	32P549-CP	32P549-CP
24-Pin SOL	32P549-CL	32P549-CL
28-Pin PLCC	32P549-CH	32P549-CH

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