DS04–21325–1aE

FUJITSU

DATA SHEET

MB1517A *ASSP*

2.0 GHz High–Speed Tuning PLL Frequency Synthesizer

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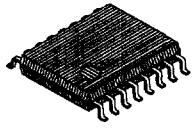
The Fujitsu MB1517A is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. MB1517A achieves the low noise performance as well as the high–speed lock-up which is required for digital mobile communications.
The MB1517A can operate from a single +3 V supply. Fujitsu's advanced technology achieves an Icc of 12 mA (typical) as well as 100 µA (typical) at power down mode.

Plastic SSOP, 16 pin



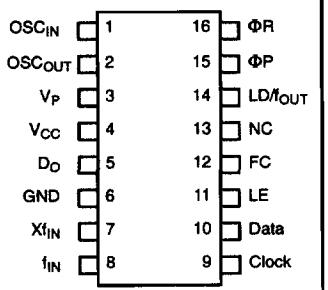
(FPT–16P–M05)

FEATURES

- High operating frequency : f_{IN} = 2.0 GHz (P_{IN} = –10 dBm)
- Pulse-swallow function : High-speed two-modulus prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 12 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit switch counter sets prescaler divide ratio
  1-bit power saving function control
  1-bit LD/font switch
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin SSOP (shrink small outline) package

PIN ASSIGNMENT

(TOP VIEW)



(FPT–16P–M05)

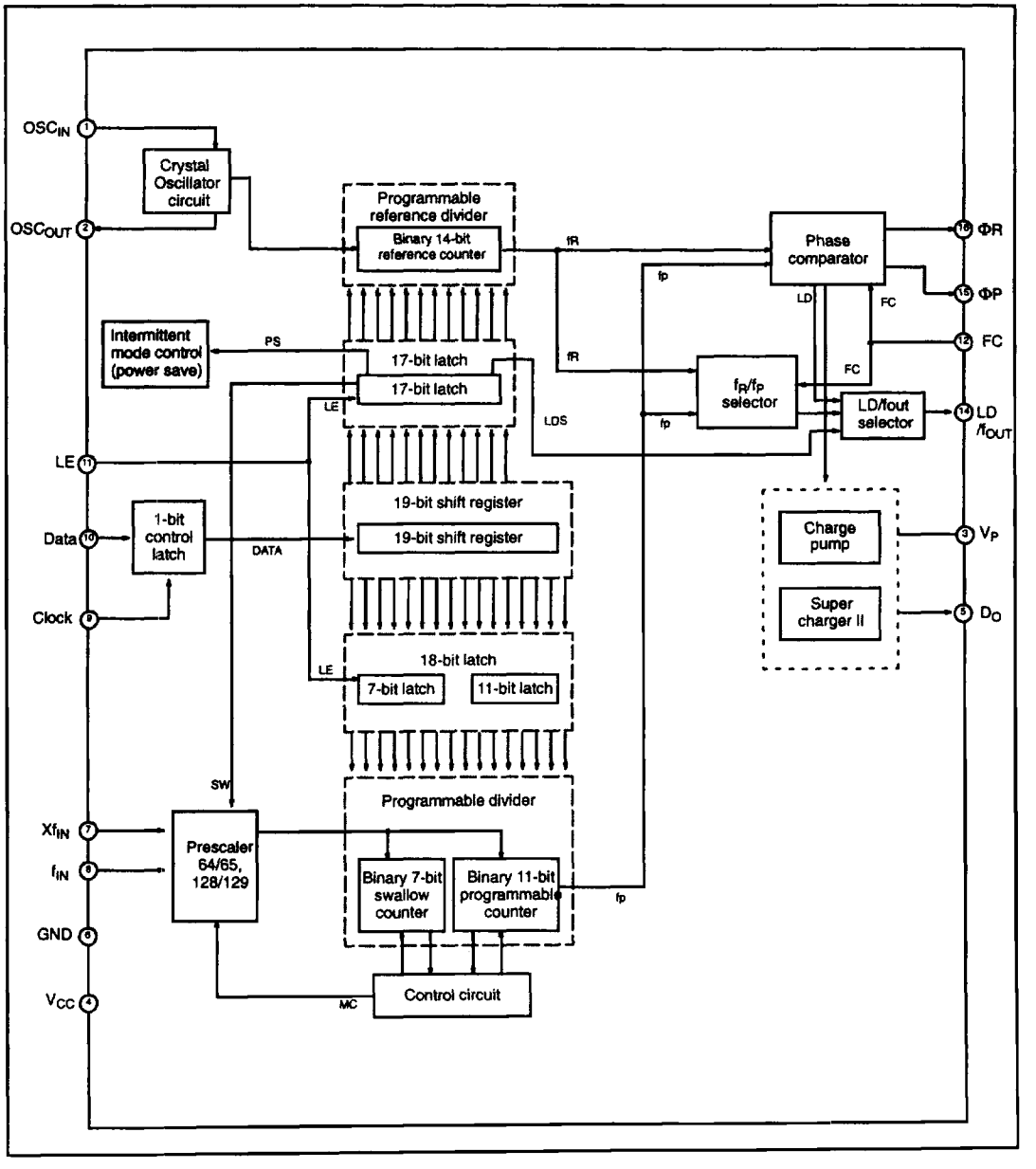
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Rating	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP, LD/fout
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output Connection for external crystal.
3	V_P	–	Power supply input for the internal charge pump
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output Phase characteristics of the charge pump can be reversed by FC input.
6	GND	–	Ground
7	Xfin	I	Complementary input of the prescaler Xfin pin should be grounded via a capacitor.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 17-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	FC	I	Phase switch input for phase comparator When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f_{OUT} pin (test pin) output (f_R or f_P).
13	NC	–	No connection
14	LD/f_{OUT}	O	Lock detector output / Phase comparator monitoring output This is a N-ch open drain output. Either of the outputs is selected by LDS bit of the serial data. a)Lock detector output : at lock state .... LD = "H" at unlock stae .. LD = "L" b)Monitoring output : Phase comparator input signals (f_P, f_R) can be monitored.
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R \quad (A < N)$

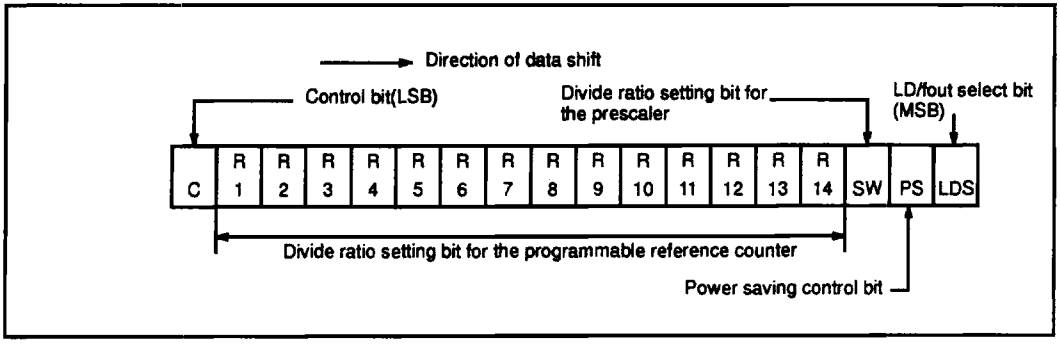
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- P : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 17-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 18-bit shift register, a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

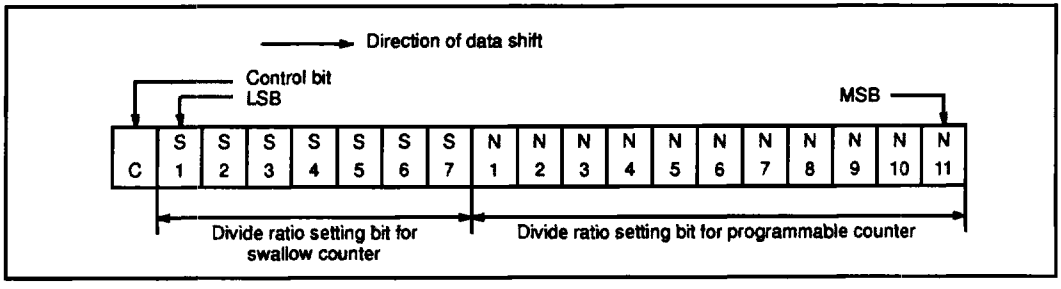
Divide ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. R1 to R14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
4. C: Control bit: Set high.
5. PS: This bit controls power saving mode.
   High : Nomal operation
   Low : Power saving mode
6. LDS: This bit controls LD/fout output signal
   High : fout signal (f_R or f_P) is selected and output via LD/fout pin.
   Low : Lock detect signal is selected and output via LD/fout pin.
7. Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

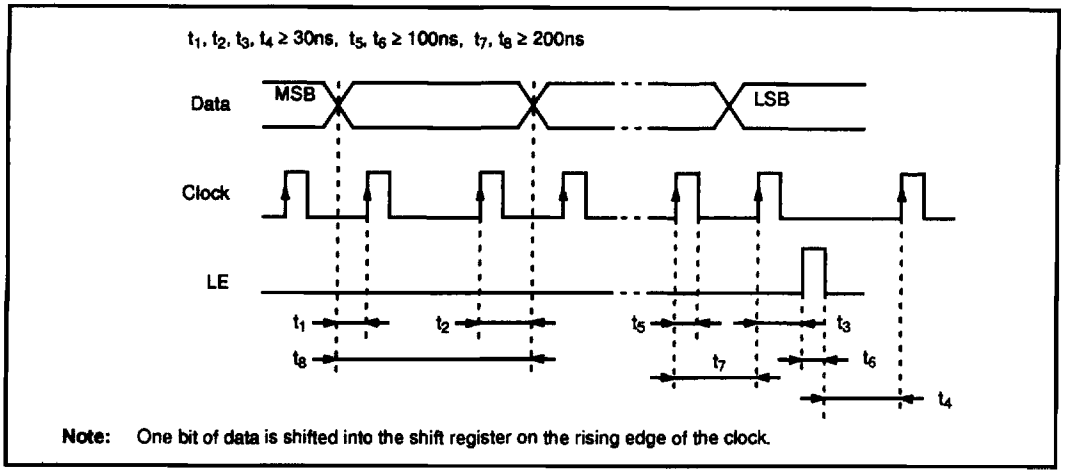
- 11-bit programmable counter divide ratio

Divide ratio N	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for the 11-bit programmable counter.
2. S1 to S7: These bits select the divide ratio of the swallow counter (0 to 127).
3. N1 to N11: These bits select the divide ratio of the programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power saving mode (intermittent operation control circuit)

Setting PS bit to Low, MB1517A enters into power saving mode resultatly current sonsumption can be limited to 100µA (typ.). Setting PS bit to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from power saving mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_R) and comparison frequency (f_P) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

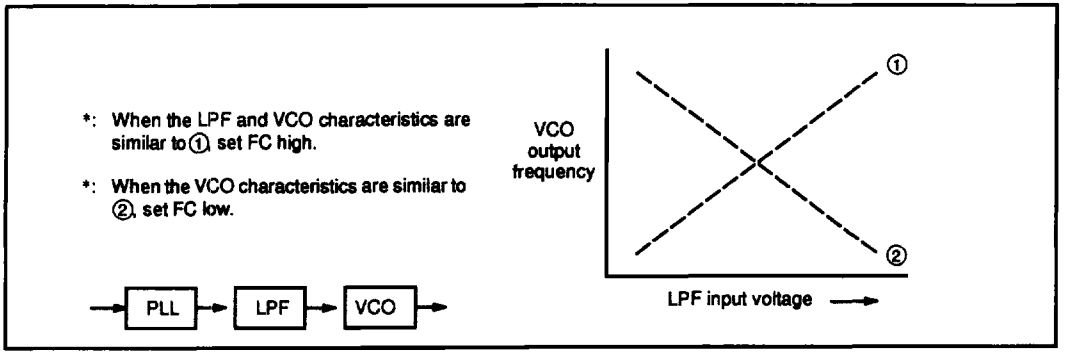
Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed depending on the FC pin input level. Also, the monitor pin (f_{OUT}) output is controlled by the FC pin. The relationship between the FC input level and each of D_O, ΦR, and ΦP is shown below:

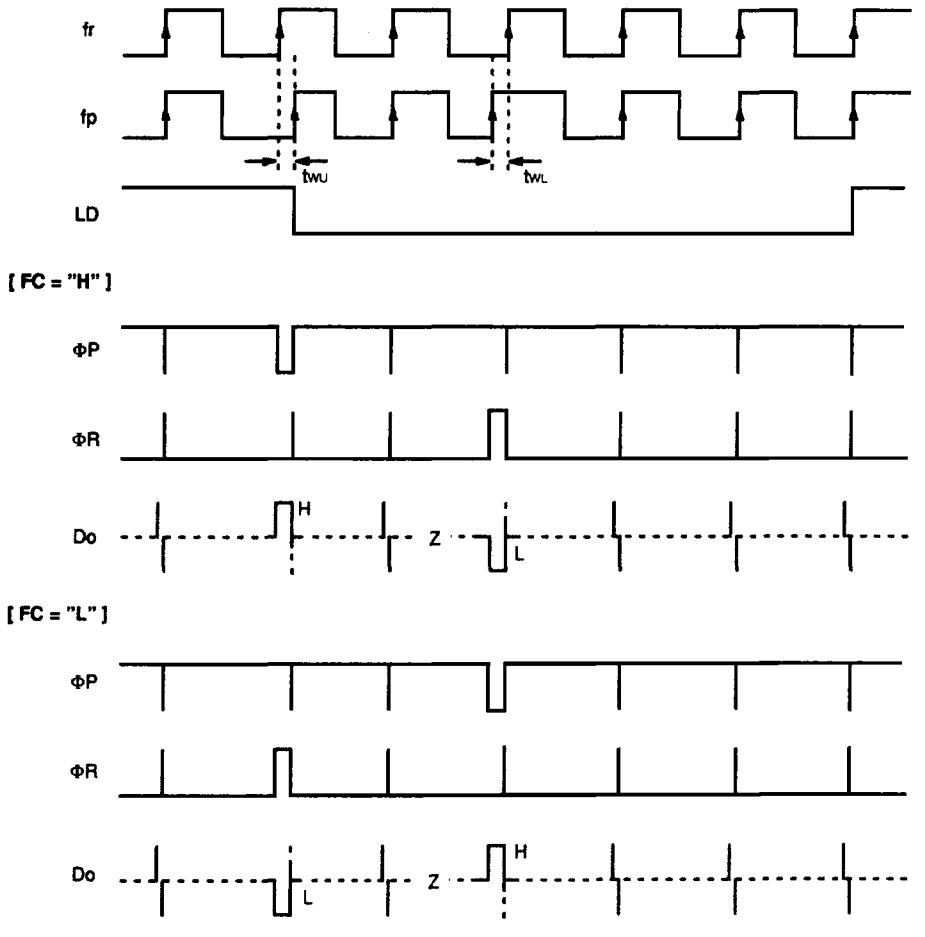
	FC = High				FC = Low			
	D_O	ΦR	ΦP	f_{OUT}	D_O	ΦR	ΦP	f_{OUT}
$f_R > f_P$	H	L	L	(f_R)	L	H	Z(*1)	(f_P)
$f_R < f_P$	L	H	Z(*1)	(f_R)	H	L	L	(f_P)
$f_R = f_P$	Z(*1)	L	Z (*1)	(f_R)	Z(*1)	L	Z(*1)	(f_P)

*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



Phase comparator output waveforms



Notes: 1. Phase difference detection range: -2π to $+2\pi$

2. LD output becomes low when phase error is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
3. twu and twL depend on OSCin input frequency.

   twu ≥ 8/fosc (e. g. twu ≥ 825ns, foscin = 12.8 MHz)

   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	-	5.0	V	
Input voltage	V_I	GND	-	V_{CC}	V	
Operating temperature	Ta	-40	-	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

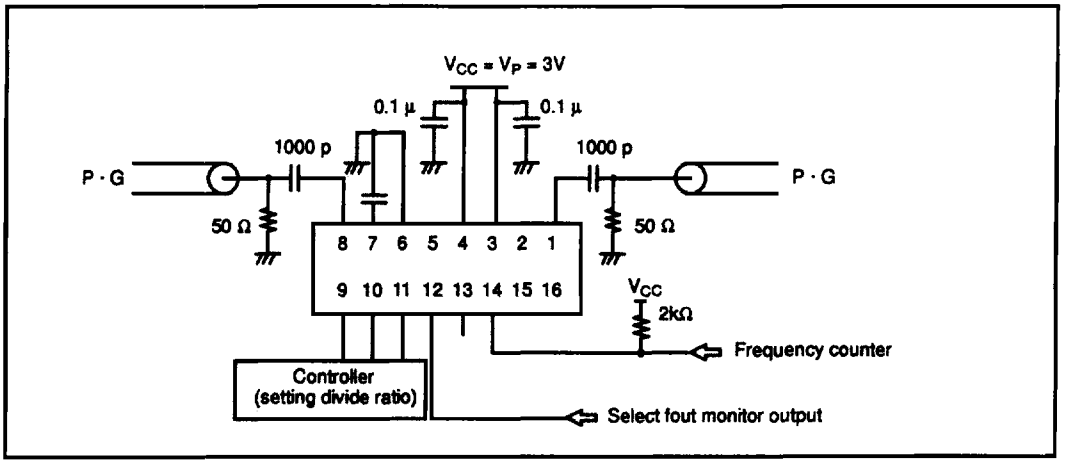
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

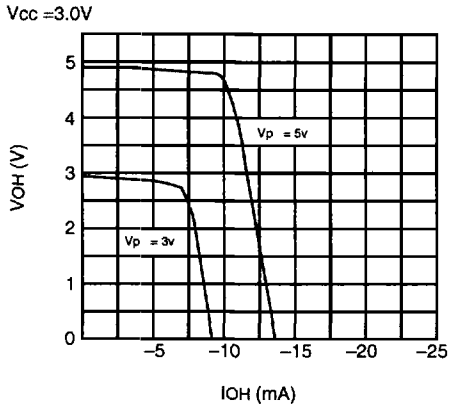
Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	12	–	mA	With f_{IN} = 2.0 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Stand by current		I_{PS}	–	100	–	µA	PS bit = "L"
Operating frequency	f_{IN}	f_{IN}	1000	–	2000	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	50Ω System
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, FC	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100		+100	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0mA
Low-level output voltage		V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_O, LD/fout, ΦP	I_{OFF}	–	–	1.1	µA	V_{CC} = 3.6V, V_P = 5 .0V V_{OOP} = GND to 6 .0V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	Vcc = 3V
		I_{OL}	–	–	1.0	mA	Vcc = 3V

TEST CIRCUIT
(for Measuring Input Sensitivity fin/OSCin)

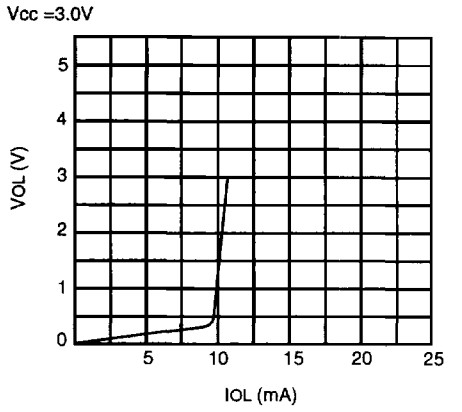


TYPICAL CHARACTERISTIC CURVES

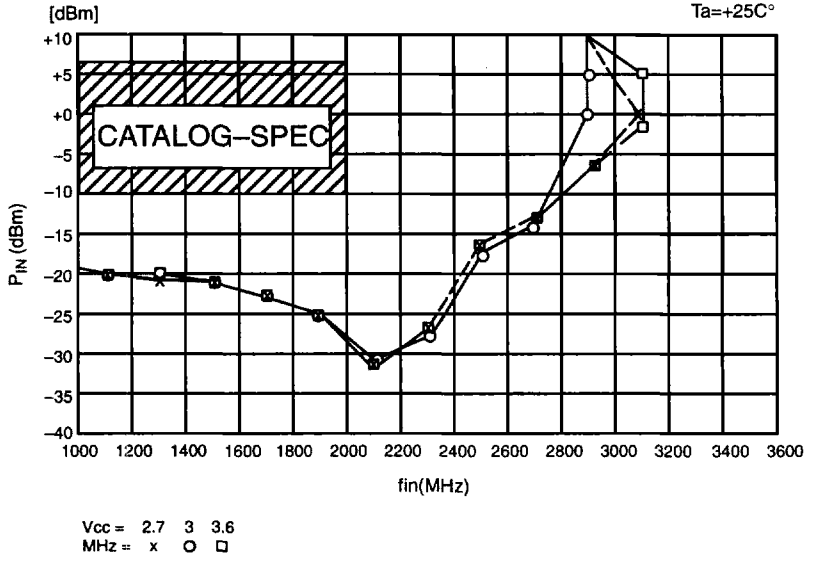
Charge pump current vs. Do voltage



Charge pump current vs. Do voltage



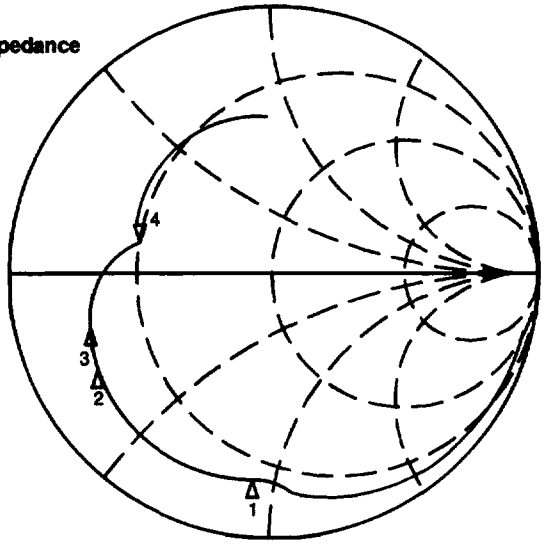
Input sensitivity vs. Input frequency



Vcc = 2.7 3 3.6
MHz = x O □

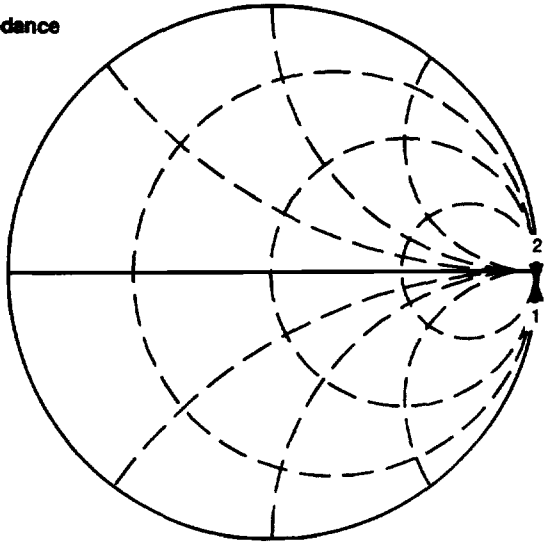
TYPICAL CHARACTERISTIC CURVES (Continued)

Prescaler Input Impedance



1: 11.115 Ω
-45.209 Ω
1 GHz
2: 8.3428 Ω
-12.503 Ω
1.5 GHz
3: 9.2764 Ω
-7.1001 Ω
1.6 GHz
4: 17.173 Ω
5.8379 Ω
2 GHz

Crystal Input Impedance



1: 2.1155 Ω
-4.4665 Ω
10 MHz
2: 426.63 Ω
-2.201 kΩ
25 MHz

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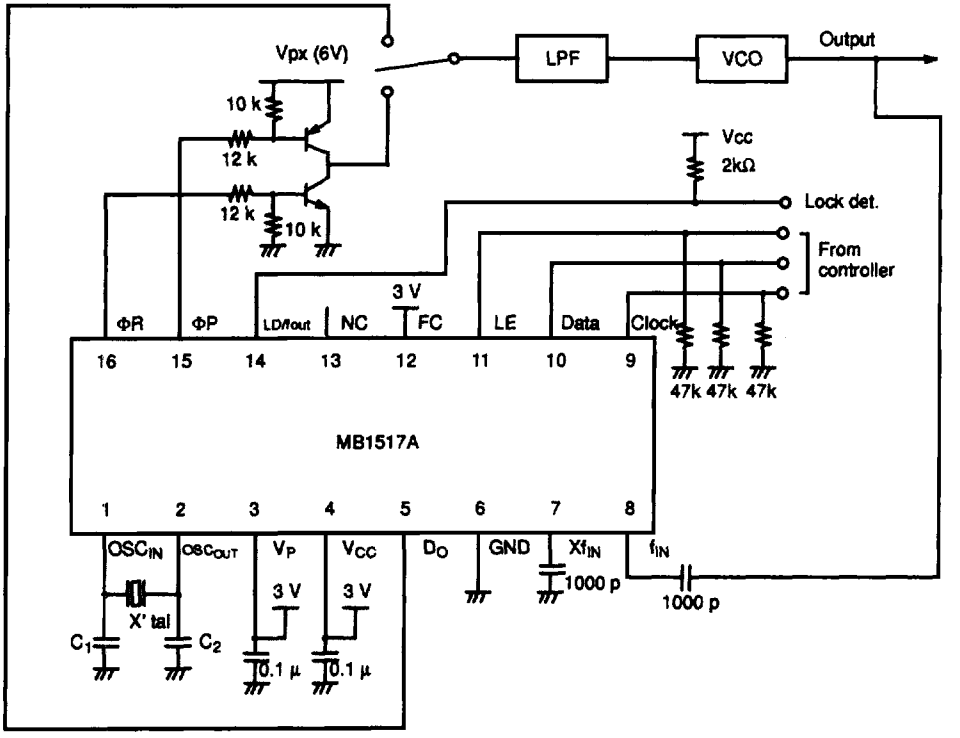
TYPICAL APPLICATION EXAMPLE

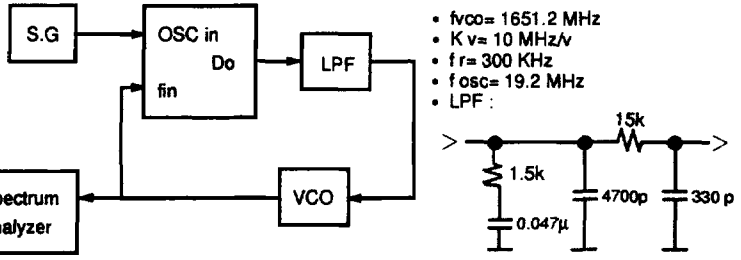


V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal oscillatar
ΦP, LD/fout : N-ch open drain output
ΦR : C-MOS output

REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below.
Each plot shows lock up time, phase noise, and reference leakage.

Test Circuit



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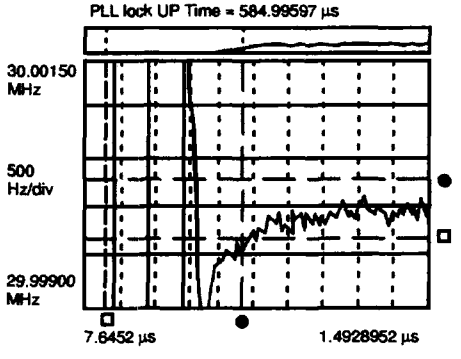
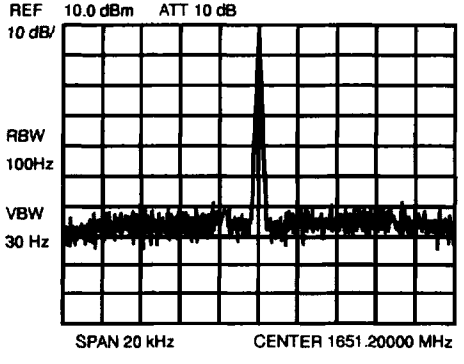
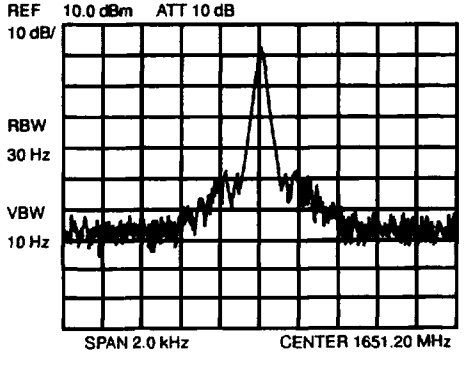
PLL Lock Up Time



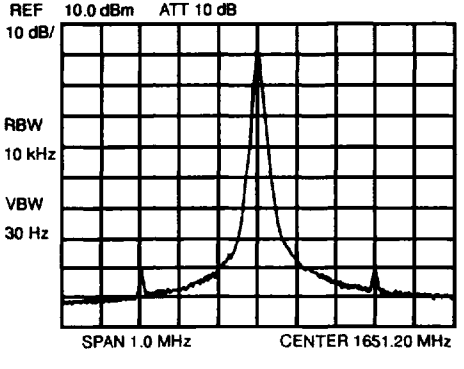
PLL Phase Noise



PLL Phase Noise



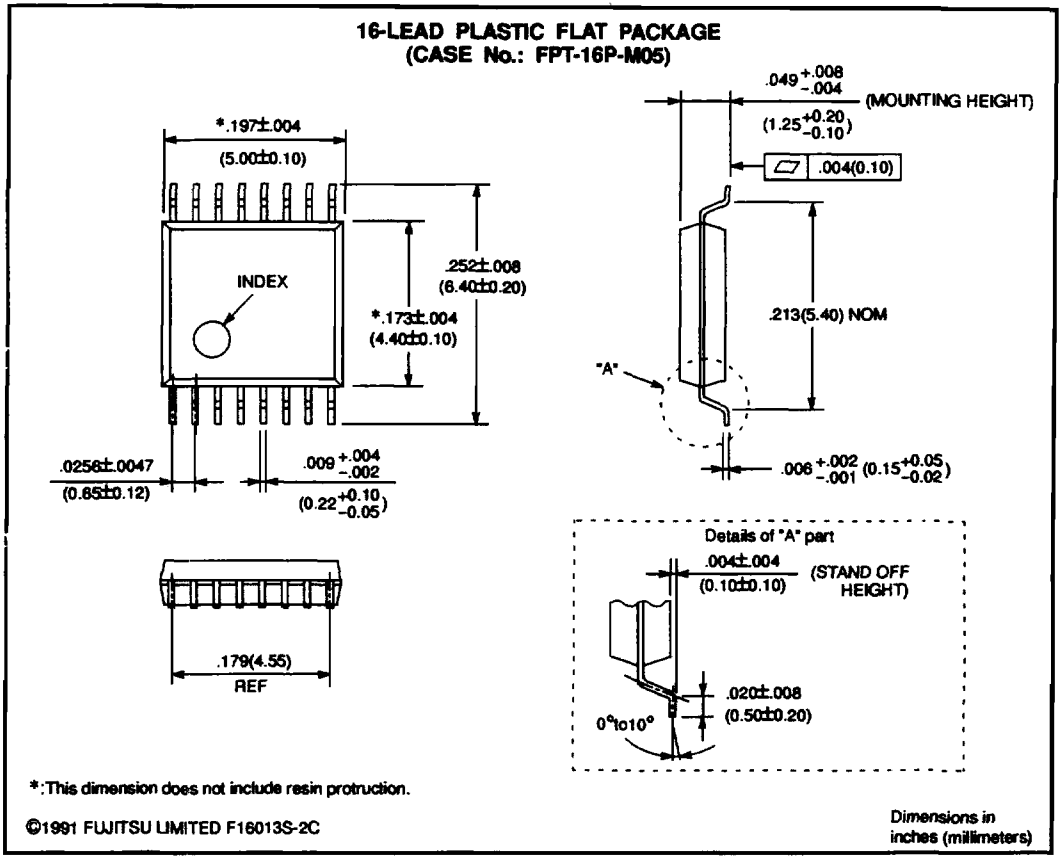
PLL Reference Leakage



ORDERING INFORMATION

Part number	Package	Remarks
MB1517APFV1	Plastic · SSOP, 16-pin (FPT-16P-M05)	

PACKAGE DIMENSION

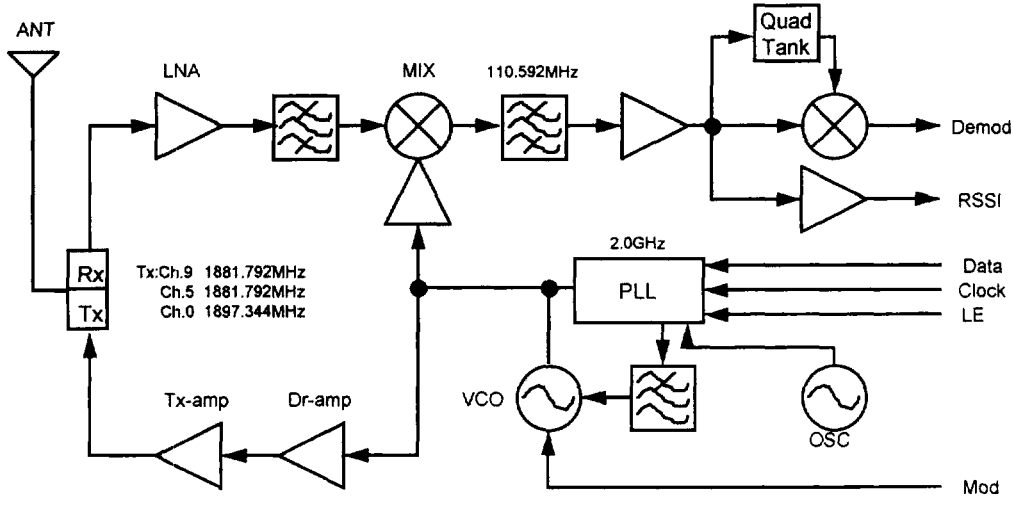


MB1517A Test Data

February 1995

ANALOG LSI DESIGN DEPARTMENT

Block Diagram of DECT RF part



PLL Serial Data Setting (fr=1.728MHz)

	Frequency	PLL Divide Ratio Prescaler(M)	N-Counter(N)	A-Counter(A)
Rx	Ch.9 1771.200MHz	64	16	1
	- 15.552MHz -	-	-	-
	Ch.0 1786.752MHz	64	16	10
	126.144MHz			
Tx	Ch.9 1881.792MHz	64	17	1
	- 15.552MHz -	-	-	-
	Ch.0 1897.344MHz	64	17	10

Pulse Swallow Function : fvco = { (M x N) + A } x fr A < N

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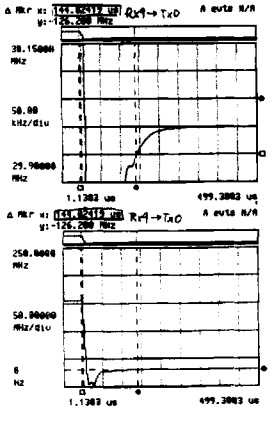
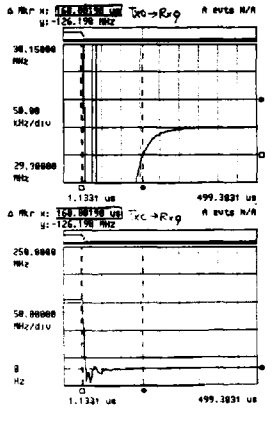
PLL Hopping Time

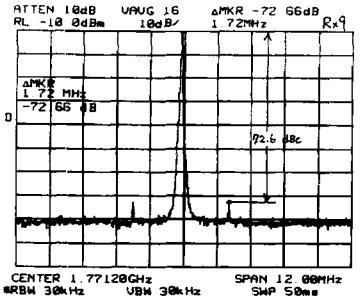
1771.200MHz -> 1897.344MHz,within ± 50KHz
Rx9 ->Tx0 144 μs



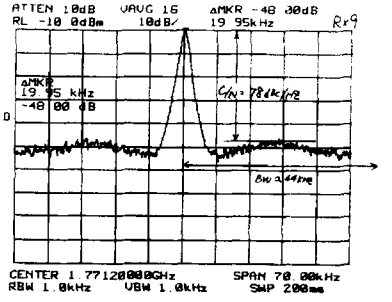
1897.344MHz -> 1771.200MHz,within ± 50KHz
Tx0 ->Rx9 160 μs



■ Spurious Level



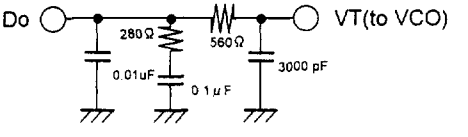
■ Phase Noise / Loop Band Width



■ PLL Characteristics of DECT Application fr=1.728MHz/Vcc=3.0V,Vp=Vvco=3.0V

Parameter		Measured Value	Conditions
Hopping Time	Rx9->Tx0	144 μs	1771.200MHz -> 1897.344MHz,within ± 50KHz
	Tx0->Rx9	160 μs	1897.344MHz -> 1771.200MHz,within ± 50KHz
Spurious Level		72dBc	±1.728MHz offset at 1771.200MHz
Phase Noise		78dBc/Hz	within Loop Bandwidth at 1771.200MHz

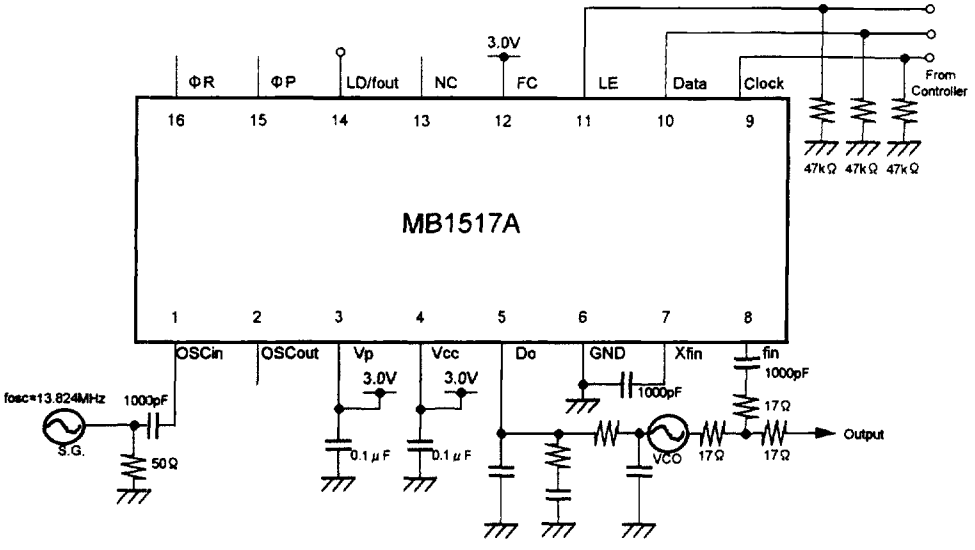
■ Loop filter scamatics



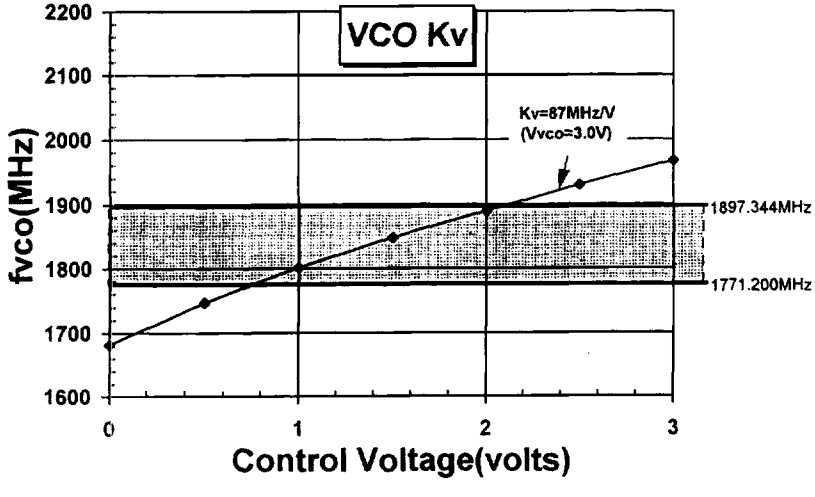
■ VCO; Kv=87MHz/V

(muRata MQE030 - 1835)

APPLICATION EXAMPLE



■ VCO Operating Range



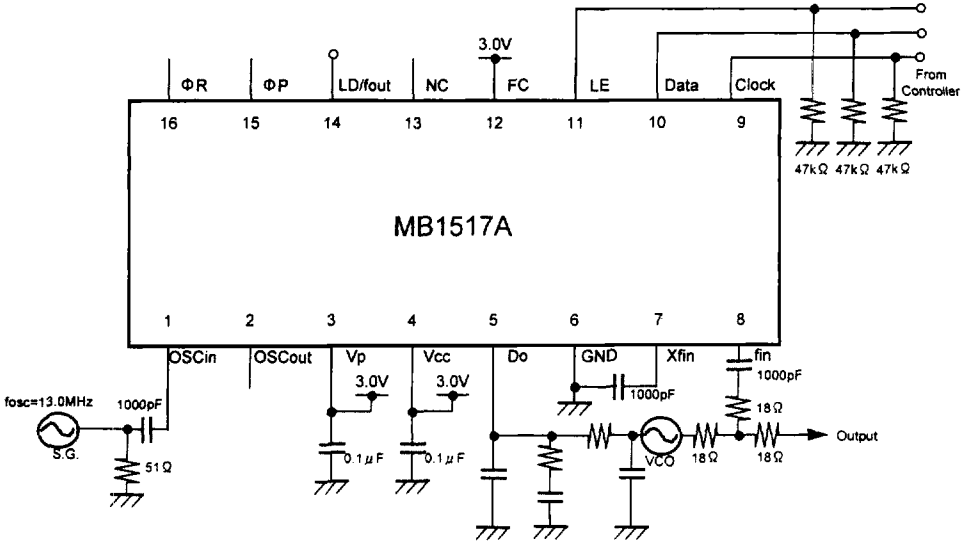
MB1517A Test Data

(PCN Application)

April 1995

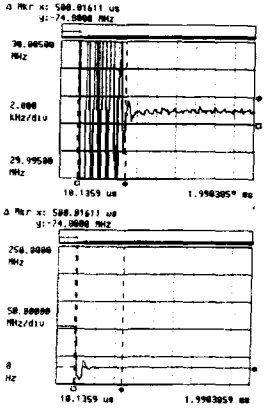
ANALOG LSI DESIGN DEPARTMENT

APPLICATION EXAMPLE

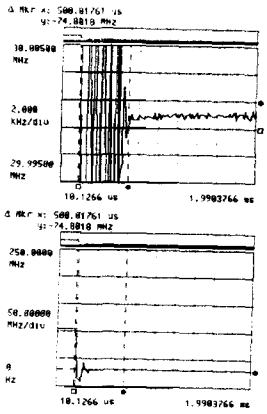


PLL Hopping Time

1797.600MHz -> 1872.400MHz,within ± 1KHz
Lch ->Hch 500 μs



1872.400MHz -> 1797.600MHz,within ± 1KHz
Hch ->Lch 500 μs



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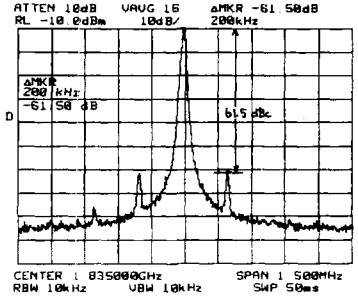
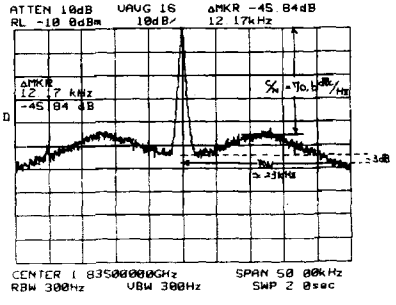
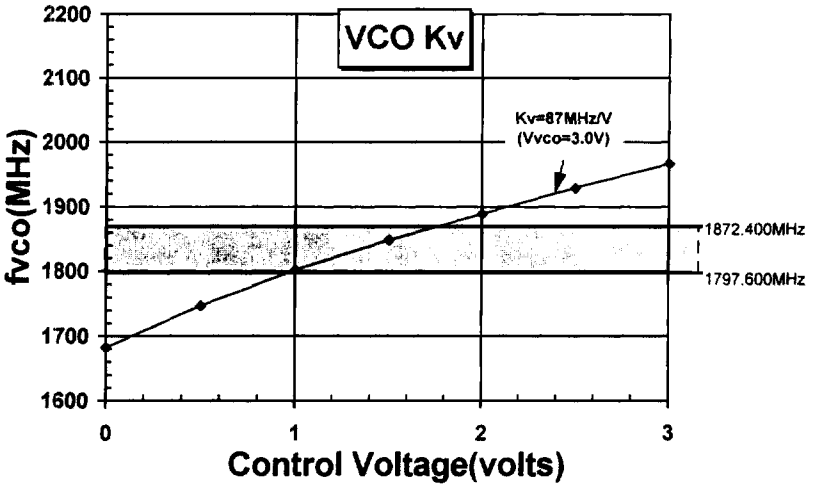
Spurious Level



Phase Noise / Loop Band Width



VCO Operating Range(muRata MQE030-1835)



PLL Serial Data Setting (fr=200kHz)

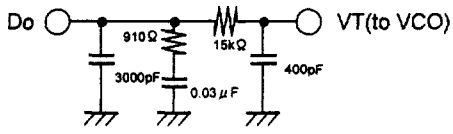
	Frequency		PLL Divide Ratio Prescaler(M)	N-Counter(N)	A-Counter(A)
Rx/Tx	Lo ch 1797.600MHz	74.8MHz	64	140	28
	37.4MHz				
	Mi ch 1835.000MHz		64	143	23
	37.4MHz				
	Hi ch 1872.400MHz		64	146	18

Pulse Swallow Function : fvco = { (M x N) + A } x fr A < N

PLL Characteristics of PCN Application fr=200kHz/Vcc=3.0V,Vp=Vvco=3.0V

Parameter		Measured Value	Conditions
Hopping Time	Lch->Hch	500 μ s	1797.600MHz -> 1872.400MHz,within ± 1KHz
	Hch ->Lch	500 μ s	1872.400MHz -> 1797.600MHz,within ± 1KHz
Spurious Level		61dBc	±200kHz offset at 1835.000MHz
Phase Noise		70dBc/Hz	within Loop Bandwidth at 1835.000MHz

Loop filter scamatics



VCO; Kv=87MHz/V

(muRata MQE030 - 1835)